High-Performance RSD Poly-Si TFTs With a New ONO Gate Dielectric

Kow-Ming Chang, *Member, IEEE*, Wen-Chih Yang, and Bing-Fang Hung

***Abstract*—This paper developed a novel polycrystalline silicon (poly-Si) thin-film transistor (TFT) structure with the following special features: 1) a new oxide–nitride–oxynitride (ONO) multilayer gate dielectric to reduce leakage current, improved breakdown characteristics, and enhanced reliability; and 2) raised source/drain (RSD) structure to reduce series resistance. These features were used to fabricate high-performance RSD-TFTs with ONO gate dielectric. The ONO gate dielectric on poly-Si films shows a very high breakdown field of 9.4 MV/cm, a longer time dependent dielectric breakdown, larger $Q_{\rm BD}$, and a lower charge-trapping rate than single-layer plasma-enhanced chemical vapor deposition tetraethooxysilane oxide or nitride. The fabricated RSD-TFTs with ONO gate dielectric exhibited excellent transfer characteristics, high field-effect mobility of 320 $\rm cm^2/V\cdot s$, and an on/off current ratio exceeding 10^8.**

***Index Terms*—Gate dielectric, N_2O-plasma oxynitride, oxide–nitride–oxide (ONO), raised source/drain (RSD), thin-film transistors (TFTs).**

I. Introduction

LOW-TEMPERATURE poly-Si thin-film transistors (LTPS TFTs) offer potential for fabricating flat panel display (FPD) with integrated system on glass [1]. In realizing large-area active matrix liquid crystal displays with integrated peripheral poly-Si TFT driving circuits on the glass substrate, gate insulator quality, and field-effect mobility are two of the most important determinants of LTPS TFTs performance and reliability [2]. However, traditional TFTs use single-layer, plasma-enhanced chemical vapor deposition (PECVD), SiO_2 or Si_3N_4 as the gate insulator and so suffer from the high interface trap density, low breakdown strength, and high gate leakage current [3], [4]. In 1984, Watanabe *et al.* first reported silicon oxide–nitride–oxide (ONO) films as alternative dielectrics for DRAM cell capacitors [5]. In 1995, C. K. Yang *et al.* used ONO film as a gate insulator in high-temperature TFTs [6]. In ONO multilayer structures, the bottom oxide provides a device-quality electrical SiO_2/Si interface. The nitride layer increases the effective dielectric constant of the ONO sandwich in such a way that a film twice as thick as SiO_2-based dielectric shows equal capacitance, and therefore decreased threshold voltage, decreased subthreshold swing, and increased drive current of the poly-Si TFTs. Finally, the top oxide provides the electrical contact to the poly-Si gate electrode [7]. Although ONO structures exploit concomitantly the advantages of oxide and nitride films, ONO films are prepared by thermal growth in an low-pressure chemical vapor deposition (LPCVD) reactor at high temperature (> 750 °C); this method is not appropriate for fabricating LTPS TFTs at a temperature much higher than a strain point of the glass substrate. Hence, this study presents a new low-temperature ($<= 300$ °C) PECVD oxide–nitride–N_2O-plasma-oxynitride multilayer gate dielectric for fabricating high performance LTPS TFTs. PECVD SiO_2/Si_3N_4 stack dielectric has been found to have lower leakage current and much longer (by 2–3 orders of magnitude) time dependent dielectric breakdown (TDDB) life time than single-layer PECVD tetraethooxysilane (TEOS) oxide or Si_3N_4 dielectrics [8], [9]. Furthermore, our previous works reported that N_2O-plasma oxide shows strong Si $\equiv$N bonds, excellent breakdown characteristic, and a smooth surface at the oxynitride/poly-Si interface [10]. Therefore, the proposed new PECVD ONO gate dielectric was expected to provide high quality interface properties, increased electric breakdown voltage, and improved reliability for LTPS TFTs.

Besides being a high-quality gate insulator, high field-effect mobility also significantly influences device performance. The excimer laser annealing (ELA) method has been widely used to obtained high field effect mobility of low temperature polycrystalline TFTs [11]. However, large off-state leakage current, poor poly-Si uniformity, and poor electrical stability of ELA poly-Si TFTs due to trap states in poly-Si grain boundaries and at the SiO_2/poly-Si interface are still serious problems. One method of alleviating these problems is to adopt a recessed channel structure [12], [13]. However, the polysilicon gate in recessed channel structure is not self-aligned to the recessed region, and the devices may have asymmetric characteristics. Therefore, it has been experimentally demonstrated that self-aligned raised source/drain (RSD) structure can provide a significantly improvement in current drive, low series resistance, and a steeper subthreshold slope [14]–[16]. The thick source/drain (S/D) region is the most promising method of decreasing the series resistance effectively and further improving the device performance. Previously, some researchers described RSD structures using local oxidation of silicon (LOCOS), selective epitaxy growth (SEG), *in situ*-doped LPCVD polycrystalline silicon, or poly deposition [12], [17]–[21]. LOCOS introduces large bird's beak, furthermore, the S/D is not self-aligned to the gate in that structure. Selective epitaxy in the source and drain regions is an attractive solution to solve this problem. However, the concerns of SEG are poor selectivity between silicon and oxide, facet formation at the gate edge, and defects caused by *in situ* dopant. The

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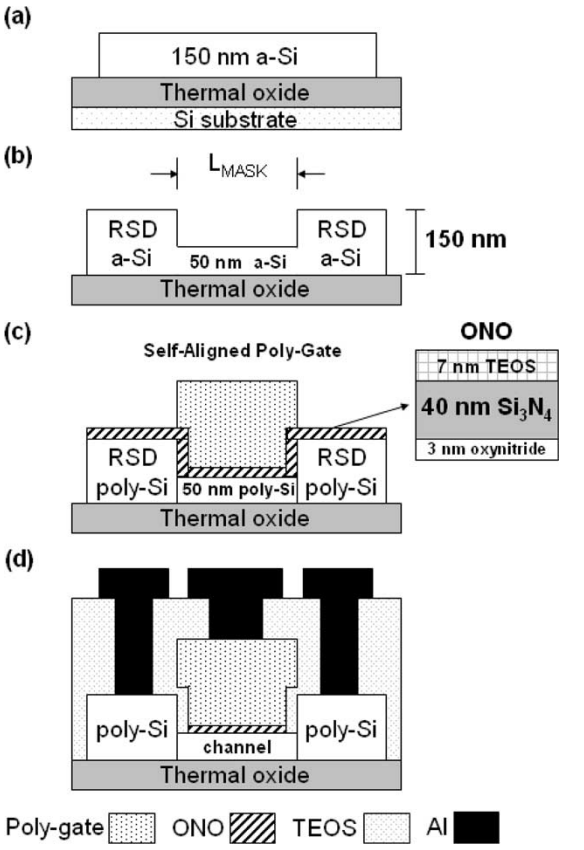

Fig. 1. Schematic cross-sectional view of key process steps for self-aligned RSD poly-Si TFT device with ONO stack gate dielectric.

advantage of *in situ* doped poly-Si and poly RSD is their independence of the original poly-Si layer, which makes it more flexible in the process integration. Therefore, this investigation uses a different process to form poly-Si RSD structure that was achieved by using RIE to etch poly-Si to form thick S/D regions without additional polysilicon deposition or selective epitaxial growth process. The experimental data show that the LTPS TFT with RSD structure has a higher on current and larger on/off current ratio than conventional TFT. Therefore, the motivation of this work has two aims. First, this paper developed a new low-temperature Oxide/Nitride/N_2O-plasma Oxynitride (ONO) gate dielectric for LTPS TFT to promote breakdown voltage, reduce leakage current, and enhance reliability. Second, the drive current and on/off current ratio of LTPS TFTs could be further promoted by using RSD structure.

II. Device Fabrication

The schematics of key processes for fabricating the RSD-TFT devices with ONO gate dielectric are illustrated in Fig. 1. At first, amorphous silicon (a-Si) films with a thickness of 150 nm were deposited on thermally oxidized Si wafers by LPCVD at 550 °C with SiH_4 as the gaseous source. The experimental conditions are given in [22]–[24]. The amorphous silicon layer then was defined as the active islands. After active islands formation, the S/D region of amorphous silicon active islands were patterned and then anisotropically etched using reactive ion etching (RIE) to form a thin 50-nm active channel region and a thick 150-nm RSD region. Because the amorphous silicon active islands had no stopper layer, the active channel region thickness was controlled by etching rate (8.33 $\text{Å}/\text{sec}$). Additionally, the a-Si film thickness was determined by Ellipsometer, and the thickness of the active channel region was accurately controlled, with an error of within $\pm 3\%$ (50 ± 1.5 nm). Laser crystallization process then was performed using KrF excimer laser (wavelength of 248 nm). During the irradiation, the energy density, pulse, and substrate temperature were 300 mJ/cm^2, ten shots, and 300 °C, respectively. The physical thickness 50-nm-thick ONO multilayer gate dielectric of the bottom-oxynitride (3 nm)/Si_3N_4 (40 nm) /top-oxide (7 nm) films then was successively deposited by PECVD. First, PECVD N_2O-plasma oxidation was performed at 300 °C substrate heating, plasma pressure 100 mtorr, and 200 W of RF power for 1 min to grow a 3-nm-thick oxynitride. Thereafter, a 40-nm-thick PECVD Si_3N_4 and 7-nm-thick TEOS oxide was continuously deposited *in situ* on the thin oxynitride film. Then, polysilicon gate was formed on the thin active channel region. Subsequently, a 200-nm-thick poly-Si was deposited and patterned to form the gate electrode. Also, the gate electrode and S/D regions were implanted by phosphorous ions at a dose of $5 \times 10^{15}/\text{cm}^2$, and energy of 40 keV. In order to reduce the extra parasitic capacitance between gate and S/D, the sidewall ONO gate dielectric in Fig. 1(c) was removed by wet etching. Post-implantation ELA then was applied to activate the dopant and anneal the amorphized S/D region silicon layer. After depositing a 400-nm PECVD TEOS interlayer oxide, contact holes were defined and opened by photolithography and wet etching. Finally, 500 nm Al was deposited and patterned to provide an electrode pad. Al sintering was then carried out at 400 °C for 30 min. The RSD-TFT with ONO gate dielectrics devices were fabricated without any hydrogenation plasma passivation treatment.

III. Results and Discussion

A. Electrical Characteristics of ONO Gate Dielectric

First, stacked type n^+ poly/dielectric/poly-Si capacitors were prepared to examine the electrical characteristics of ONO, TEOS oxide, and Si_3N_4 dielectrics. For comparing ONO gate dielectric quality, the control samples were comprised of physical thickness 50-nm-thick PECVD TEOS oxide or Si_3N_4 were not treated with N_2O-plasma [3], [8]. Fig. 2. shows the current density versus electric field (J–E) characteristics of TEOS oxide, Si_3N_4, and ONO gate dielectric films. The J–E characteristics of TEOS, Si_3N_4, and ONO dielectrics were measured by grounding the source and drain of the TFTs and applying a gate bias that swept from 0 to +50 V. Obviously, The breakdown field of ONO stack gate dielectric is larger than that of PECVD TEOS oxide to the value of about 3 MV/cm. The ONO dielectric film had a very high electric breakdown field of 9.4 MV/cm and a much lower leakage current than PECVD TEOS oxide and Si_3N_4 films. This phenomenon is attributed to two reasons: First, the thin bottom-layer of N_2O-plasma oxynitride with high interface quality resulting in a smooth surface and strong Si $\equiv$ N bonds at the oxynitride/poly-Si interface [25], [26]. Second, in the nitride film, electrons are trapped and drift toward the top oxide by the Poole–Frenkel conduction

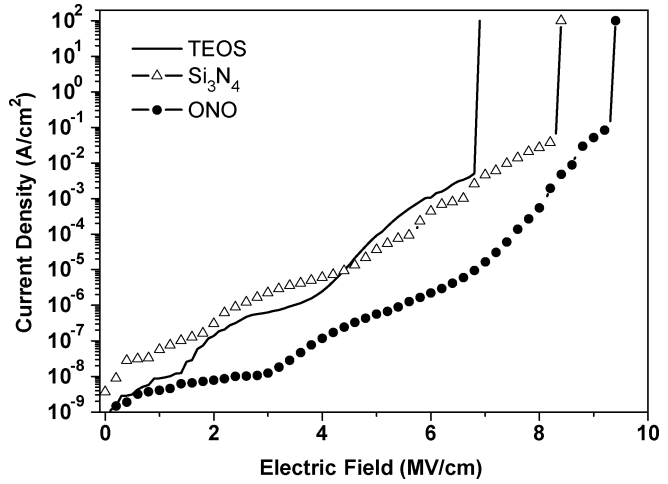

Fig. 2. Current density versus electric field (J–E) characteristics of the gate dielectric films for the conventional TEOS oxide, PECVD Si_3N_4 and proposed ONO stack gate dielectric.

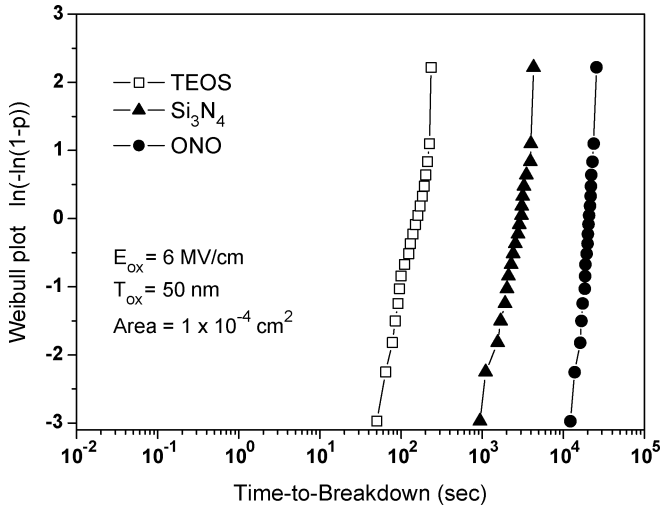

Fig. 3. Weibull plot of time-to-breakdown distribution obtained from constant voltage stress test for MOS devices with 500-nm gate dielectric thickness. Dielectric breakdown characteristics of the ONO film is dramatically improved, compared with those of PECVD TEOS and Si_3N_4 films.

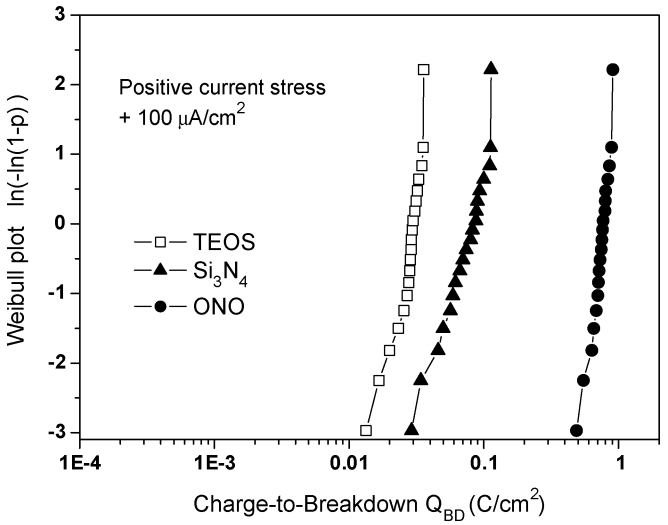

Fig. 4. Weibull plots of charge-to-breakdown for TEOS, Si_3N_4, and ONO stack gate dielectric under positive constant current stress of 100 μA/cm^2. The capacitor area was 1×10^{-4} cm^2.

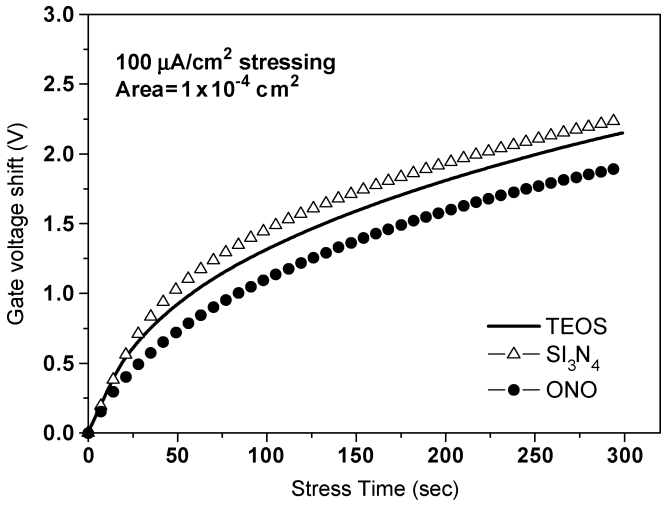

Fig. 5. Measured gate–voltage shift, ΔV_g, of MOS capacitors for the TEOS, Si_3N_4, and ONO films under the constant-current stress condition with current density of 100 μA/cm^2. ΔV_g for the ONO film by carrier-trapping is smaller compared with that for TEOS oxide or Si_3N_4 film.

[27]. The electrons reaching the top oxide may tunnel though it to be collected by the gate. Tunneling though the oxide depends on the oxide thickness and the applied electric field or voltage. The as-fabricated top-layer 7-nm-thick TEOS oxide has a sufficient barrier height to suppress the Poole–Frenkel leakage current. Therefore, the top and bottom oxides of the ONO gate dielectric play very important roles in the reduction of a leakage current. Fig. 3. presents the Weibull plot of TDDB distribution of the TEOS, Si_3N_4, and ONO films under constant voltage stress test. It is worth mentioning that the TDDB lifetime of the ONO film is about 1–2 orders of magnitude remarkably improved compared with those of the TEOS oxide and the Si_3N_4 dielectrics. The improvement of the electrical reliability of the ONO film is believed to be related to the PECVD N_2O-plasma effectively repairs defects in the oxynitride and poly-Si film, such as Si dangling bonds. Moreover, it is also considered that the accumulation of nitrogen at the oxynitride/poly-Si interface is one reason for the high electrical reliability [10], [26]. Fig. 4. shows charge-to-breakdown $(Q_{\rm BD})$ cumulative distributions of TEOS, Si_3N_4, and ONO films under positive constant current stress of $+100$ μA/cm^2. The physical thickness 50-nm-thick ONO stack gate dielectric has $Q_{\rm BD}$ up to 0.91 C/cm^2. The $Q_{\rm BD}$ value is much larger than that of PECVD TEOS and Si_3N_4 to the values of 0.021 and 0.068 C/cm^2. Fig. 5. shows the charge-trapping characteristics of TEOS, Si_3N_4, and ONO films under a constant current stress. The gate voltage shifts, ΔV_g, is smaller for the ONO film than for TEOS and Si_3N_4. The lower electron-trapping rate of ONO dielectric implies that the N_2O-plasma formed a smooth surface at oxynitride/poly-Si interface, which provides fewer trap sites and a lower current density with a lower electron-trapping rate [28].

To examine the roughness of the interface between N_2O-plasma oxynitride and poly-Si layer, the surface rough-

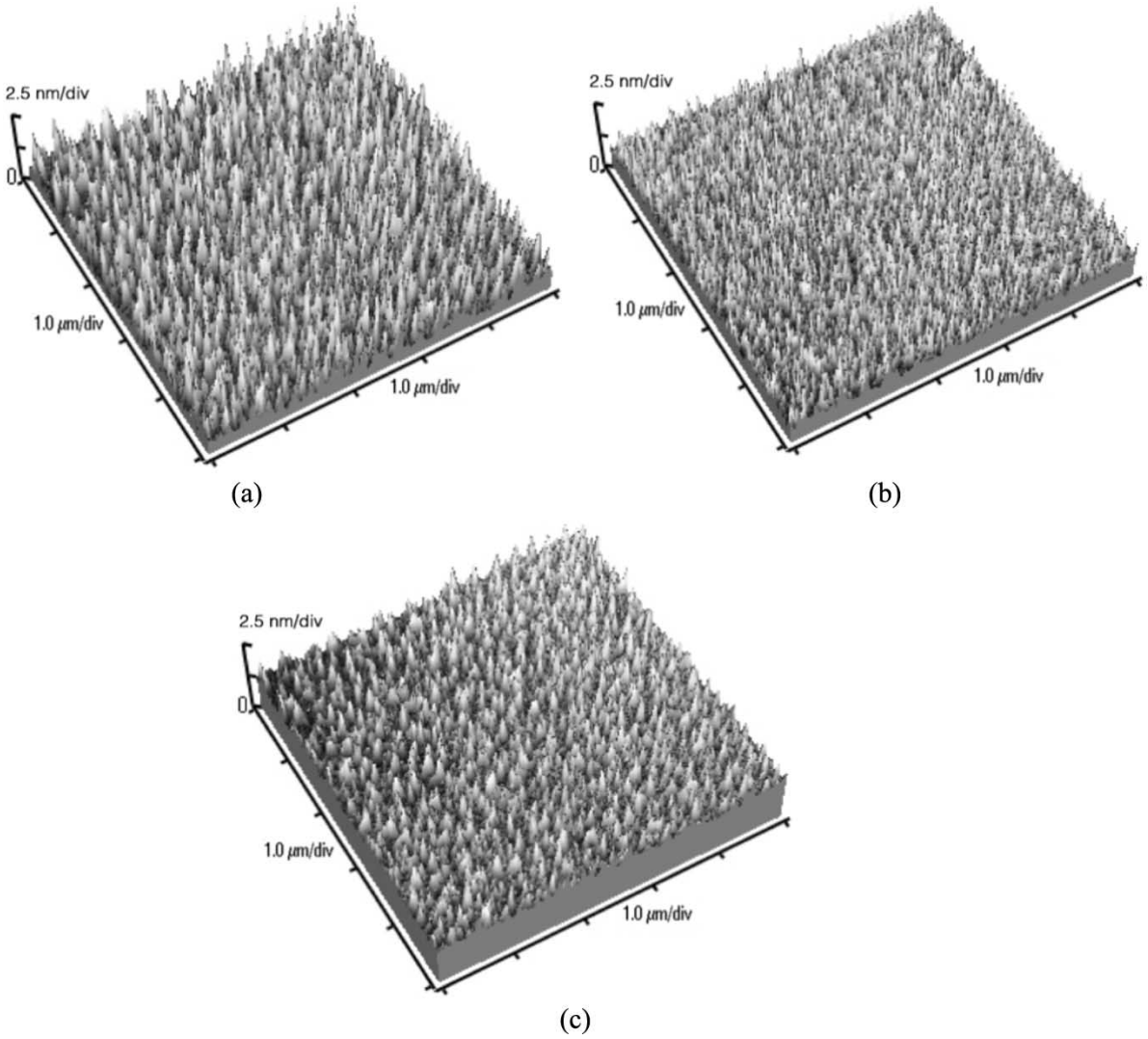

Fig. 6. AFM images of KrF laser annealed poly-Si films. (a) Poly-Si surface before oxidation. The rms roughness of the surface was measured to 4.53 nm. (b) Poly-Si surface after ONO dielectric deposition. The rms roughness was measured to 3.69 nm. (c) Poly-Si surface after PECVD TEOS oxide and Si_3N_4 deposition. The rms roughness was measured to 4.47 and 4.51 nm, respectively.

ness was measured using atomic force microscopy (AFM). Fig. 6. shows the AFM images of the KrF laser annealed poly-Si films. Before AFM measurements, grown dielectrics were completely removed in 50:1 HF solution. The root mean square (rms) roughness of poly-Si surface before oxidation was measured as being 4.53 nm. The rms roughness of poly-Si surface after ONO dielectric deposition then was reduced to 3.69 nm and the rms roughness of poly-Si surface after PECVD TEOS or Si_3N_4 deposition were almost the same as the original poly-Si surface, namely 4.47 and 4.51 nm, respectively. The poly-Si surface of ONO gate dielectric was significantly smoother than that of PECVD TEOS oxide and Si_3N_4. Apparently, the roughness existing at TEOS or Si_3N_4-poly-Si interface thus provides various trap sites and lead to a higher current density with higher electron-trapping rate, thus causing smaller $Q_{\rm BD}$ values. These analytical results confirm that larger electron conduction and electron trapping characteristics of PECVD TEOS oxide and Si_3N_4 compared to ONO gate dielectric are due to larger polysilicon surface roughness and poor quality dielectric film.

B. Electrical Characteristics of RSD-TFT With ONO Gate Dielectric

Conventional poly-Si TFTs with channel thickness of 50-nm-thick and TEOS, Si_3N_4 or ONO gate dielectrics were fabricated for comparing device performance. Typical transfer characteristics of conventional poly-Si TFTs with TEOS, Si_3N_4 or ONO gate dielectrics are shown in Fig. 7. Conventional poly-Si TFTs with TEOS oxide have maximum field effect mobility of 84.5 $\rm cm^2/V\cdot s$, a minimal leakage current of 5.1 pA, and an on/off current ratio of 7.7×10^6. The poly-Si TFTs with new ONO gate dielectric (ONO-TFT) have greatly improved field-effect mobility and on/off current ratio: the electron mobility increased from 84.5 to 213.8 $\rm cm^2/V\cdot s$, minimal leakage current decreased from 5.1 pA to 1.7 pA, and the current ratio increased from 7.7×10^6 to 1.1×10^8. The improvement of ONO-TFT was attributed to the reduction of interface traps and the formation of a smooth surface at the oxynitride/poly-Si interface by N_2O-plasma oxide. Therefore, the combination of PECVD N_2O-plasma oxynitride, Si_3N_4 and TEOS oxide successfully promoted the breakdown field of gate dielectric

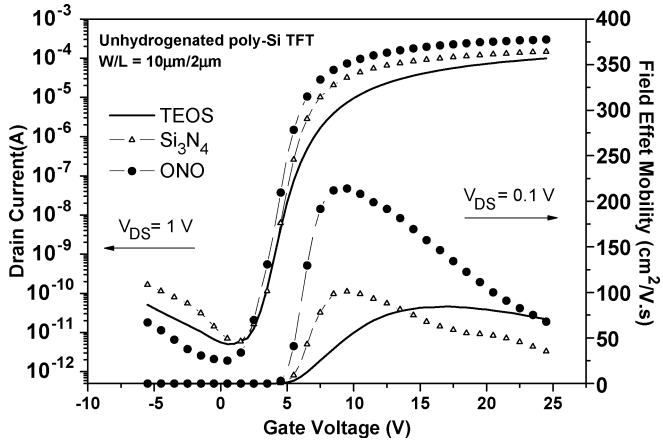

Fig. 7. Transfer characteristics of conventional poly-Si TFTs with ONO multilayer gate dielectrics were measured at $V_{\rm DS} = 1$ V for drain current I_d and $V_{\rm DS} = 0.1$ V for field-effect mobility $\mu_{\rm FE}$.

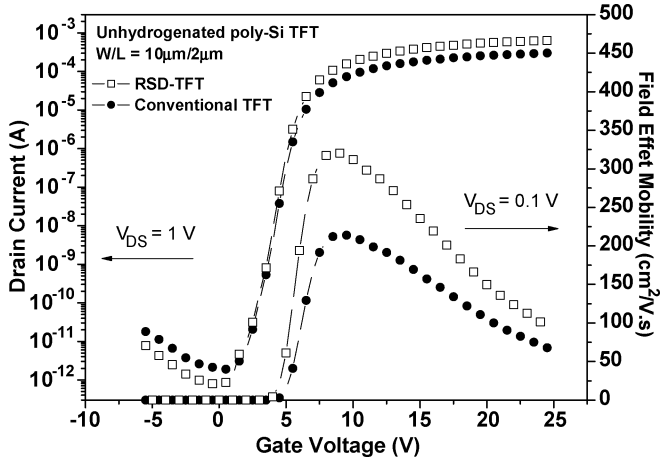

Fig. 8. Transfer characteristic of RSD-TFT and conventional TFT with ONO gate dielectric.

and improved the electrical characteristics of LTPS TFTs, because N_2O-plasma oxidation incorporates nitrogen atoms at the SiO_2/poly-Si interface, forming a nitrogen-rich layer with Si $\equiv$N bonds. Additionally, high dielectric constant Si_3N_4 film in the middle layer offers high capacitance to increase drive current, and the top-oxide constitutes an electrical contact to the poly-Si gate electrode and suppresses the Poole–Frenkel leakage current from the Si_3N_4 film.

Fig. 8 shows the transfer characteristics of RSD-TFT and conventional TFT (ONO-TFT) with ONO stack gate dielectric. The RSD-TFT with ONO stack gate dielectric with channel thickness of 50 nm, and an RSD region thickness of 150 nm, showed a 120% increase in on-current, a 50% increase in peak mobility (320 $\rm cm^2/V \cdot s$), and a 62% decrease in off-current at $V_{\rm GS} = -5$ V, compared with conventional TFT devices with the same channel thickness and ONO gate dielectric. Table I summarizes the performance parameters of fabricated RSD-TFT and ONO-TFT devices. The RSD-TFT exhibited better electrical characteristics than the conventional ONO-TFT. Because lateral thermal gradient could arise because of the heat generated

TABLE I
SUMMARY OF THE ELECTRICAL CHARACTERISTICS PARAMETERS OF FABRICATED RSD-TFTS AND ONO-TFTS WITH HIGH-QUALITY ONO GATE DIELECTRIC

W/L = 10μm/2μm	channel thickness (nm)	S/D Thickness (nm)	Vth (V)	subthreshold swing (mV/dec)	mobility ($\rm cm^2$/V-s)	on/off current ratio
RSD-TFT	50	150	3.1	445	320	6.2×10^8
ONO-TFT	50	50	3.6	496	213	1.1×10^8

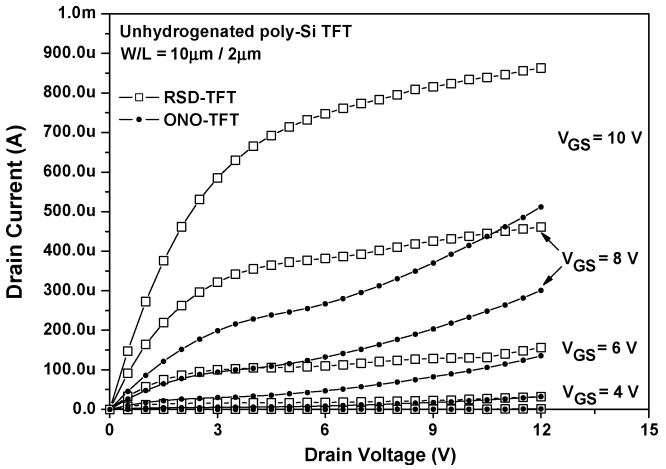

Fig. 9. I_d–V_d output characteristics of RSD-TFT and conventional TFT with ONO gate dielectric.

at the moving solid-melt interface during ELA crystallization process, resulting large longitudinal grains could be grown in the thin channel regions accompanied with thick S/D region for reducing series resistance [29]. Fig. 9 shows the I_d–V_d output characteristics for both RSD-TFT and conventional TFT with ONO stack gate dielectric. Better drive current and steeper linear region revealed that the RSD-TFT had less S/D series resistance than conventional TFT. The current drivability is improved due to the formation of low-resistivity RSD structure in RSD-TFT. The RSD-TFT device had a measured low S/D sheet resistance of 620 Ωsq was smaller than that of 1.6 kΩsq of conventional TFT with same channel thickness and without RSD structure. It also can be seen that for the conventional ONO-TFT, the current–voltage curves behave more like resistance with increasing gate voltage. This phenomenon occurs because for larger gate bias, the channel resistance becomes smaller, hence, the dominant resistance comes from the source and drain region. The output current is subject to be limited by the source and drain resistance. Therefore, the output current of RSD-TFT is much larger than that of the conventional ONO-TFT because of its thick S/D region.

Finally, the drive current of TFT devices is known to be affected by:

1) presence of grain boundaries in the channel region;
2) series resistance in the S/D regions;
3) thick gate dielectric;
4) defect states in the channel and at the SiO_2/Si interface [30], [31].

Therefore, current drivability can be improved by excimer layer crystallization techniques to eliminate grain boundaries in the channel region, scaling the body thickness, low series resistance in RSD region, and using a thinner and better gate dielectric. The proposed poly-Si RSD-TFT with high-quality ONO gate dielectric has achieved all of the advantages mentioned above. Consequently, the proposed RSD-TFT with high-quality ONO gate dielectric has promise for realizing the FPD with peripheral drive integrated circuits on glass panel.

IV. Conclusion

This paper has proposed a high-performance RSD-TFT with a self-aligned RSD structure and high-quality ONO gate dielectric. The proposed ONO gate dielectric has superior dielectric properties to the conventional PECVD oxide and nitride films. Furthermore, this study applied this ONO gate dielectric to RSD-TFT to promote device performance. The RSD-TFT with ONO gate dielectric exhibits excellent electrical characteristics, with a field effect mobility of up to 320 $cm^2/V{\cdot}s$, and high current drivability. These improvements are related to the high interface quality of the bottom N_2O-plasma oxynitride film, the leakage current reduction by the combined effect of the TEOS oxide/Si_3N_4 films, and the low-resistivity thick source/drain region.

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