The Effect of Thermal Treatment on Device Characteristic and Reliability for Sub-100-nm CMOSFETs

Wen-Kuan Yeh, *Member, IEEE*, Yean-Kuen Fang, and Mao-Chieh Chen

***Abstract*—The effect of post-thermal annealing after halo implantation on device characteristic and reliability of sub-100-nm CMOSFETs was investigated. We found that the control of annealing time is more efficient than that of annealing temperature with respect to improving the hot-carrier-induced degradation. The best result of device performance and reliability was obtained by a post-thermal annealing treatment performed at medium temperatures (e.g., 900 °C) for a longer time (>1 min).**

***Index Terms*—Halo, hot-carrier-induced degradation, indium, post-thermal annealing.**

I. Introduction

FOR MOSFET, the reduction in threshold voltage $(V_{\rm th})$ with decreasing channel length is widely used as an indicator of short-channel effect (SCE) [1], [2]. As MOSFET scaled down to 100 nm and below, this adverse $V_{\rm th}$ roll-off effect may become a major limitation on the deep-submicron-device performance. In order to control the SCE in the sub-100-nm regime, it is necessary to reduce the gate oxide thickness and source/drain extension-junction depths. However, the possibility of direct tunneling limits the extent to which the gate oxide thickness can be thinned [3], and the reduction of source/drain extension-junction depths through lowering thermal budget gives rise to the dopant activation problem, which leads to degradation of device driving capability. In this context, lateral channel engineering provides an extra degree of freedom for the effect of limiting the adverse SCE effects [4]. Recently, local high doping concentration in the channel near source/drain junctions was employed via lateral channel engineering, e.g., halo [5], pocket [6], TCI (tilted-channel implantation) [2], and TIPS (tilted implantation punchthrough stopper) [7]. These implantations introduce the same type of impurity as in the channel region following the gate-etching, which can be symmetrical [6], [7] or asymmetrical [8] with respect to the deep source/drain implants. Engineering channel dopant profile for the localized halo implant has been used extensively in deep-submicron CMOS work and has become indispensable to achieving sub-100-nm CMOSFETs [9]. Indium (In) has been successfully used to obtain abrupt profiles in nMOSFETs because of its low diffusion constant [10], which leads to shallower deep-submicron nMOSFET source–drain extension/halo profiles. Unfortunately, interstitial Si is also produced during the In ion implantation, resulting in an increase in leakage current and degradation of device performance [11], [12]. Moreover, the hot-carrier-induced device's degradation is also enhanced. Thus, a post-thermal annealing (PA) treatment following the In-halo implantation is proposed to solve these problems. However, pMOSFET device characteristics are easily degraded by post-thermal treatment because of the out-diffusion of channel doping. On the other hand, with the continuous shrinking of device dimensions and gate oxide thickness, generation of interface traps during negative bias temperature instability (NBTI) stress in pMOSFET has become the most critical reliability issue that would ultimately determine the lifetime of devices. [13], [14]. In this work, we investigate the device characteristics and hot-carrier-induced device degradation of B-halo nMOSFETs, In-halo nMOSFETs, and As-halo pMOSFETs. The effect of PA on NBTI is also investigated for pMOSFETs. We propose an appropriate PA for In-implanted halo nMOSFETs and As-implanted halo pMOSFETs to achieve a high-performance and well-reliability sub-100-nm CMOSFETs.

II. Experiments

Devices were fabricated on p-type, (110)-oriented 8-inch Si wafers of 15–25 $\Omega \cdot$ cm resistivity using the conventional CMOSFET twin-well process. Following the shallow-trench isolation process, n/p-wells were formed using phosphorus (P) and boron (B) MeV implantation. Dual-gate CMOSFETs were fabricated with a 2-nm-thick nitrided gate oxide, grown by rapid thermal oxidation in NO ambient followed by poly-Si layer deposition. After poly-Si gate patterning with poly gate lengths $(L_{\rm G})$ in the range from 100 to 250 nm, n/p source/drain extensions were formed using, respectively, As^+ and B^+ ion implantations. Then, tilted-angle halo implantation was applied at 20∼30 degrees using B^+ (at 10∼30 KeV, $2 \sim 5\times10^{13}$ cm^{-2}) and In^+ (at 120∼180 KeV, $1 \sim 3 \times 10^{13}$ cm^{-2}) for nMOSFETs, and As^+ (at 110∼130 KeV, $2 \sim 4 \times 10^{13}$ cm^{-2}) for pMOSFETs. After the halo implantation, the device samples were annealed with rapid thermal processing (RTP) at various temperatures ranging from 900 °C to 1050 °C. A thin liner

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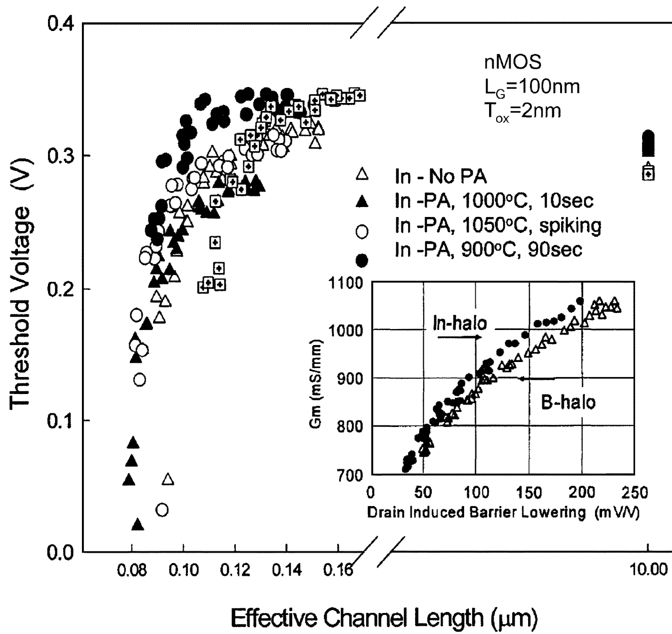

Fig. 1. Threshold voltage roll-off as a function of effective channel length. The inset in the figure shows intrinsic transconductance of nMOSFETs with In-halo and B-halo structures as a function of DIBL.

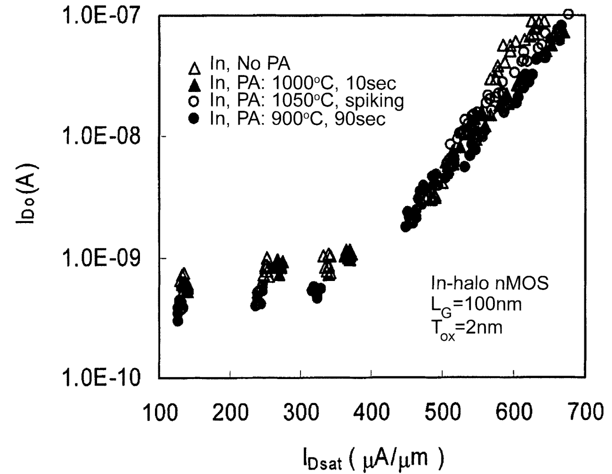

Fig. 2. I_{Do} versus I_{Dsat} for B-implanted and In-implanted halo nMOSFETs with various post-thermal annealing (PA).

oxide was deposited at 500 °C to 900 °C, followed by a SiN-spacer deposition at 400 °C to 800 °C. After formation of a 100-nm-thick composite liner oxide/SiN spacer, n^+/p^+ deep source/drain junctions were formed using As (at 40∼60 KeV) and B (at 6∼10 KeV) ion implantation. Finally, the wafers were annealed using RTP at 1000 °C followed by $CoSi_2$ salicidation processing. Then the sample preparation was completed after a standard backend flow processing. In this work, the drain current I_{D} was determined at $V_{\mathrm{G}} = V_{\mathrm{D}} = 1.2$ V and trancon-ductance G_m was determined with derivation of $dI_{\mathrm{D}}/dV_{\mathrm{G}}$. To investigate the hot-carrier effect, device stress and measurements were made on a probe station at various drain voltages ($|V_{\mathrm{D}}| = 1.2 \sim 2.0$ V) and gate voltages ($|V_{\mathrm{G}}| = 0 \sim 1.8$ V) for various durations. For pMOSFETs, NBTI stress was applied at a gate voltage of -1.8 V with the drain/source and substrate terminals connected to ground for a stress time of 100 min at an elevated temperature of 25 °C to 125 °C.

III. Results and Discussion

A. Indium-Halo Versus Boron-Halo nMOSFETs and Thermal Treatment for In-Halo nMOSFETs

Threshold voltages, as determined by the $G_{m\max}$ method, are illustrated in Fig. 1 as a function of effective channel length (L_{eff}). The L_{eff} was derived using a modified Shift and Ratio algorithm [15], which extracts parameters between two neighboring short-channel devices ($L_{\mathrm{gate}} = 100$–250 nm) without concerning the mobility difference. Compared to the B-halo-structure devices, the In-halo samples have a formed localized high-dose halo structure because of the low diffusion constant of indium, thus improving the punch-through margin of the devices. The inset in Fig. 1 shows the G_m versus drain-induced barrier lowering (DIBL: measured deviation of gate voltage at $V_{\mathrm{D}} = 0.1$ and $V_{\mathrm{D}} = 1.2$ V); it is worth noting that the mobility of the In-halo nMOSFETs is higher than that of the B-halo nMOSFETs, particularly for the devices with L_{eff} less than 100 nm. In this work, the In-halo samples are free from apparent reverse short-channel effects (RSCEs), while the conventional B-halo samples exhibit such effects. Transient enhanced diffusion (TED), which is believed to be the cause of RSCEs, was effectively suppressed in the In-halo devices [16] due to indium deactivation [17]. Thus, In-halos lead to reducing V_{th} and increasing device resistance to SCEs. However, a large amount of Si interstitials will be generated by the As-extension implantation and further enhanced by the In-halo implantation. These Si interstitials can react with the In dopant more efficiently, resulting in a more pronounced deactivation, and causing accelerated V_{th} roll-off in short-channel devices [18]. Thus, PA is proposed to remove these Si interstitials and suppress the TED phenomenon. Although Si interstitials can be removed with higher temperature with shorter time (e.g., 1000 °C, 10 s), junction depth was also increased following the PA with an RTP at 1000 °C, resulting in a higher device V_{th} roll-off. Thus, a lower temperature was possible better post-treatment without device performance degradation. However, longer time is necessary for medium-temperature treatment to give enough energy for Si interstitials removing. In this study, we found that the device SCEs can be improved by RTP at 900 °C for a longer period of time (e.g., longer than one minute). It is believed that the Si interstitials can be removed by a medium-temperature annealing for an appropriately longer time without degrading the device SCEs. We found that higher saturated values of V_{th} and RSCEs apparently occur in the In-halo nMOSFETs annealed at 900 °C for a longer period of time. Medium-temperature annealing can improve SCEs in the In-halo devices, even in the sub-100-nm channel-length range, thus reducing the device's off-state drain current (I_{Do}). Fig. 2 illustrates that the device's I_{Do} can be reduced with the 900 °C long-time annealing. Although the localized In-halo dopant is located only around the extension junction and does not degrade the device's driving capacity, the hot-carrier effect of the In-halo device is still a troublesome problem, which becomes more serious with decreasing dimension. In comparison with the B-halo nMOSFET, the In-halo nMOSFET

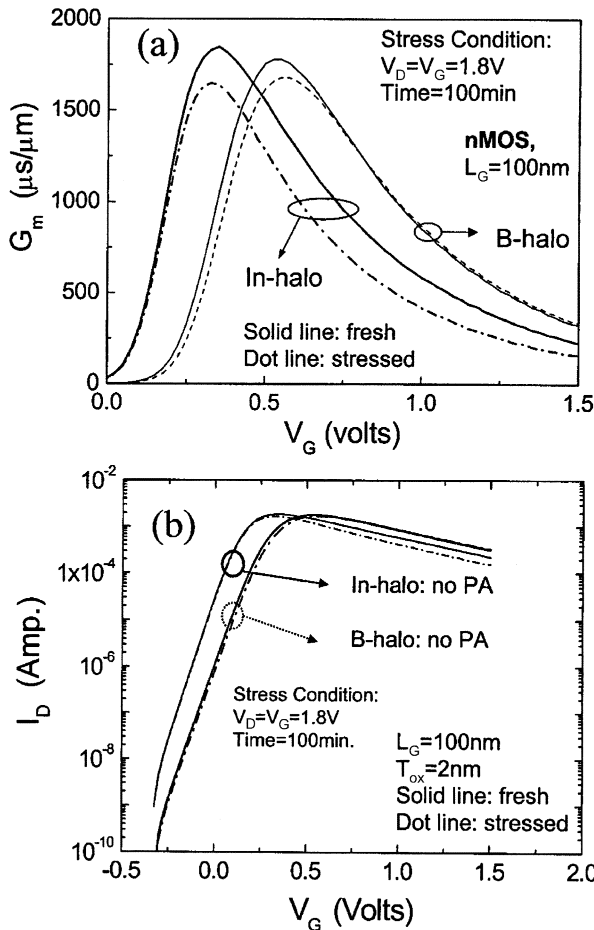

Fig. 3. (a) Transconductance (G_m) and (b) drain current (I_{D}) as a function of gate voltage (V_{G}) for B-implanted halo and In-implanted halo nMOSFETs before and after hot-carrier stress.

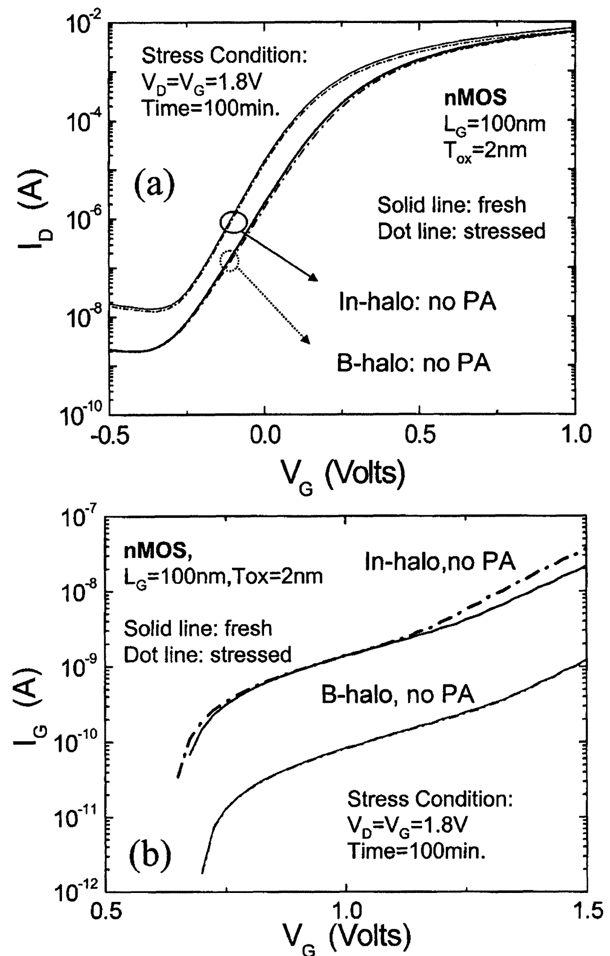

Fig. 4. (a) Subthreshold characteristic and (b) gate leakage (I_{G}) as a function of gate voltage (V_{G}) for nMOSFET with B-implanted and In-implanted halo structures before and after hot-carrier stress.

shows a larger hot-carrier-induced G_m degradation, particularly at higher gate voltage, as well as a worse subthreshold characteristic, as shown in Fig. 3. For the In-halo nMOSFET, the abrupt and shallow junction profile increases the drain electric field and enhances the high impact-ionization rate of channel carrier, thus aggravating the hot-carrier effect. It is apparent that the B-halo device has a smaller junction leakage than the In-halo device, as shown in Fig. 4(a). According to the results of Yu *et al.* [1], the B-halo nMOSFET exhibits a normal recombination-generation junction leakage, while the highly localized dose of the In-halo nMOSFET shows the presence of a drain-to-halo (body) band-to-band tunneling current. This tunneling leakage can be a considerable contributor to the device's I_{Do}, resulting in higher I_{Do} in the device with an In-halo structure. The swing degradation indicates the creation of interface traps, resulting in a threshold voltage shift [19]. The gate-induced drain leakage (GIDL) in B-halo and In-halo nMOSFETs at a negative gate bias of $V_{\mathrm{G}} = -0.5$ V was increased. It has been reported that GIDL is a direct result of the generation of interface states; thus, the largest degradation in I_{Dsat} coincides with the largest increase in interface state density. Compared to the B-halo nMOSFET, the subthreshold characteristic of the In-halo nMOSFET shows a larger I_{Do} and GIDL. Moreover, the gate leakage of the In-halo device is larger than that of the B-halo device, and is increased after the hot-carrier stress, particularly at a higher gate voltage, as shown in Fig. 4(b). It is believed that the In-halo nMOSFET contains a larger number of interface states, which lead to the degraded device characteristic and reliability, in particular after hot-carrier stress. Fig. 5 shows that the gate leakage of the In-halo device increases with the implantation dose of In-halo, and that the leakage is further increased after the hot-carrier stress, particularly at a higher gate voltage. We believe that the higher implant dose of In-halo resulted in increase of interface state generation, thus aggravating the gate leakage of nMOSFETs. In this study, the In-halo device's subthreshold swing and I_{Do} can be most efficiently improved with a long-time PA at 900 °C, as shown in Fig. 6. The hot-carrier-induced degradation of saturated drain current (I_{Dsat}) is illustrated in Fig. 7 as a function of stress time; it clearly indicates that the In-halo device degrades more seriously than the B-halo device. However, significant improvement with respect to the stress-induced I_{Dsat} degradation was achieved for the In-halo device by applying appropriate PA. A long-time PA at 900 °C, for example, was able to make the In-halo nMOSFET show a very low drain degradation of less 3%. In this work, the interstitial defect caused by the In-halo implantation and

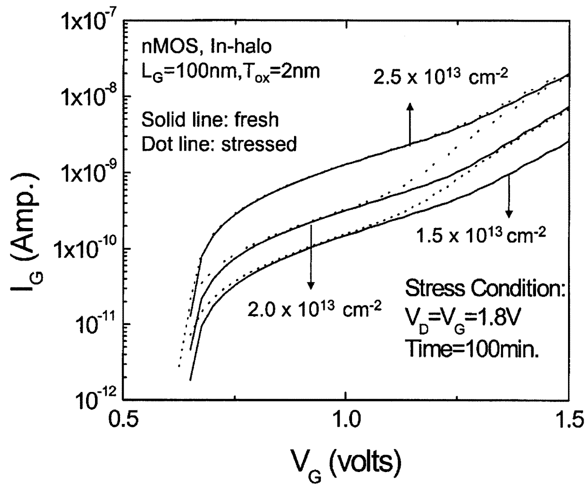

Fig. 5. Gate leakage (I_{G}) as a function of gate voltage (V_{G}) for In-halo nMOSFETs with various indium implantation doses before and after hot-carrier stress.

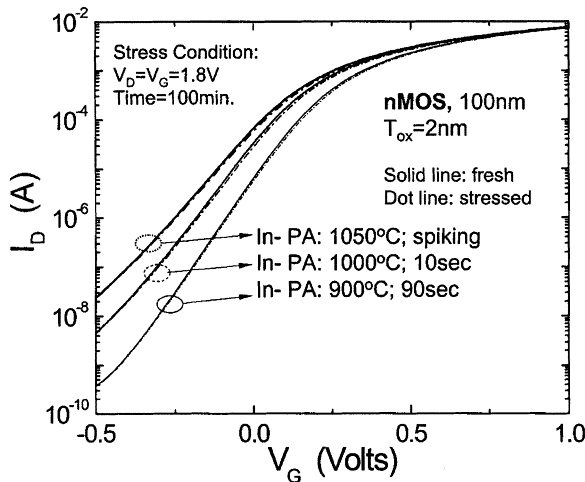

Fig. 6. Subthreshold characteristic for nMOSFETs with In-implanted halo structure with various post-thermal annealing before and after hot-carrier stress.

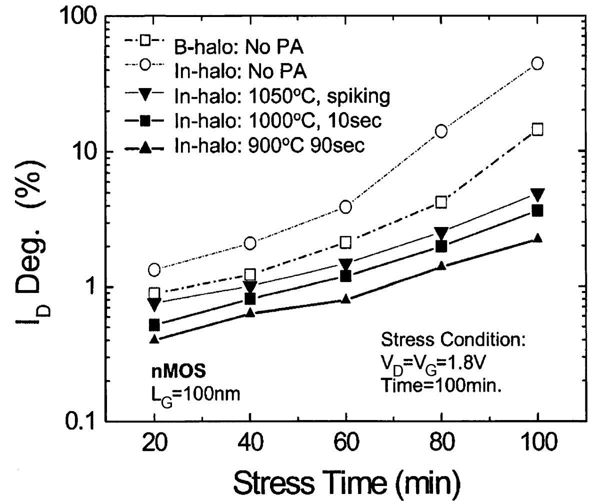

Fig. 7. Hot-carrier-induced degradation of saturated drain current (I_{Dsat}) versus stress time for nMOSFETs with B-implanted and In-implanted halo structures with and without post-thermal annealing.

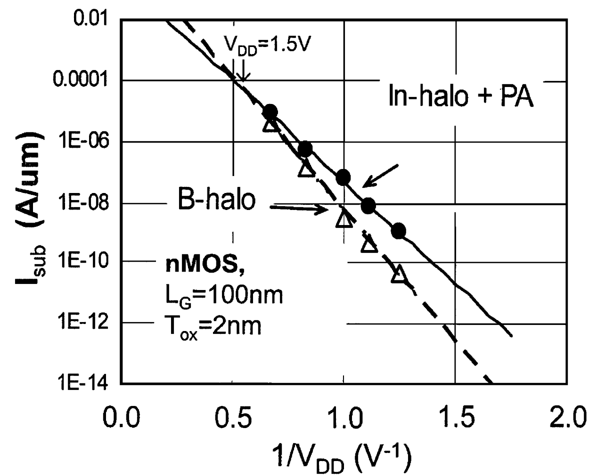

Fig. 8. Substrate current as a function of drain voltage (V_{D}) for B-halo nMOSFET and In-halo nMOSFET with PA.

the channel impact ionization caused by the electron can be suppressed with appropriate PA. Thus, an appropriately PA annealed In-halo nMOSFET shows longer lifetime and lower substrate current (I_{sub}) than the B-halo nMOSFET, particularly at stress voltage larger than 1.5 V, as shown in Fig. 8. It is apparently that an appropriate PA is necessary to improve the device's reliability especially for high-performance products (operating voltage $>$1.2 V).

B. Thermal Treatment for As-Halo pMOSFETs

As-halos implantation is used to modify the pMOSFET drain structure for efficiently blocking the B-extension. However, Si interstitials are also generated by the As-halo implantation. These Si interstitials will degrade the device performance and enhance the hot-carrier effect. Fig. 9 shows the G_m versus gate voltage and the subthreshold characteristic for the As-halo pMOSFETs with various As-halo concentrations before and after hot-carrier stress. Since higher dose of As-halo implantation would result in more abrupt junction, higher carrier mobility and thus higher G_m can be obtained. However, higher dose implantation would also generate more Si interstitial, leading to degradation of the device characteristic, particularly at higher gate voltage. Moreover, the subthreshold characteristic is also degraded with increasing dose of As-halo implantation. Thus, the hot-carrier-induced I_{Dsat} degradation of the As-halo pMOSFETs becomes more serious as the As-halo implantation dose is increased, as shown in Fig. 10. Apparently, an appropriate PA is necessary to improve the pMOSFETs characteristic. However, the PA may affect the B-extension/As-halo structure due to the change in boron doping profile in the channel region, leading the device's V_{th} shift, particularly for the device annealed with a short-time PA at 1000 °C. Fig. 11 shows the G_m versus gate voltage for three differently post-annealed As-halo pMOSFETs before and after the hot-carrier stress. It can be seen that a serious V_{th} shift occurred after the device was annealed with a short-time PA at 1000 °C, and that the device degradation remained after a hot-carrier stress. In this work, we found that the hot-carrier-induced G_m degradation can be efficiently recovered

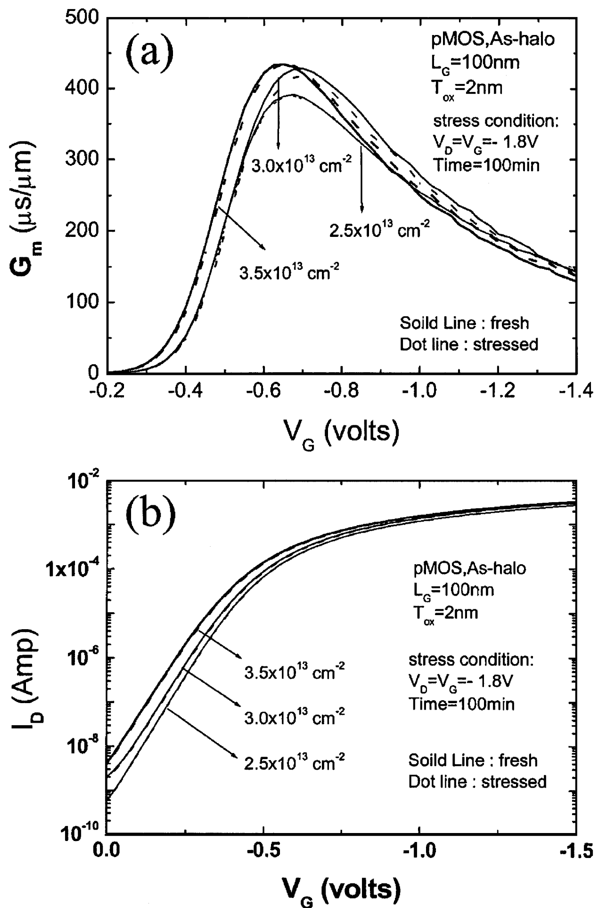

Fig. 9. (a) Transconductance (G_m) versus gate voltage and (b) subthreshold characteristic for As-implanted halo pMOSFET with various As-halo implantation doses before and after hot-carrier stress.

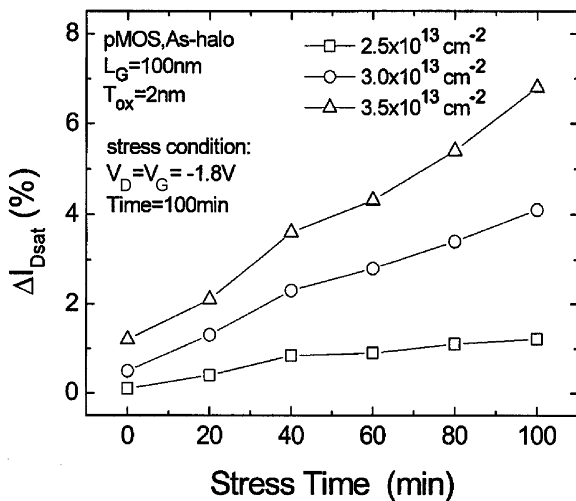

Fig. 10. Hot-carrier-induced degradation of saturated drain current ($I_{\rm Dsat}$) versus stress time for As-halo pMOSFETs with various As-halo implantation doses.

with a long-time PA at 900 °C without causing the device's threshold voltage shift. With this PA, the As-halo pMOSFETs subthreshold characteristic was also improved, as shown in Fig. 12. This is because the pA efficiently removed interface defects and thus the device's gate leakage was improved, in particular the long-time PA at 900 °C, as shown in Fig. 13.

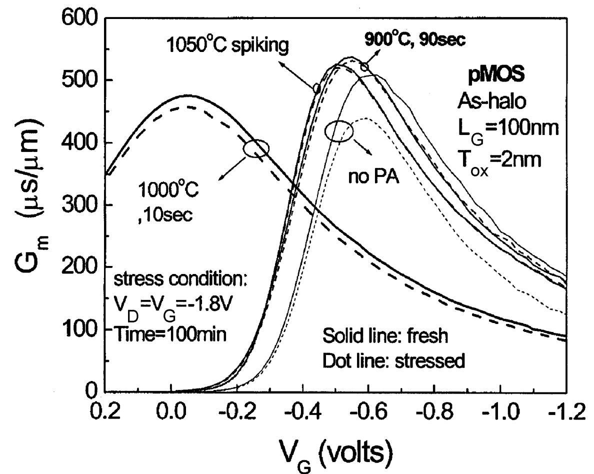

Fig. 11. Transconductance (G_m) versus gate voltage for differently post-annealed As-halo pMOSFET before and after hot-carrier stress.

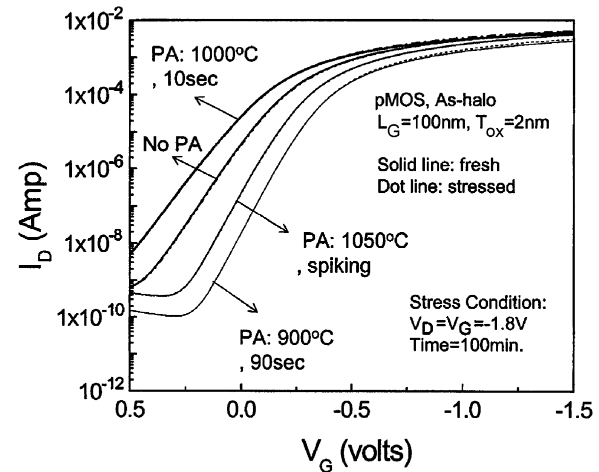

Fig. 12. Subthreshold characteristic for differently post-annealed As-halo pMOSFETs before and after hot-carrier stress.

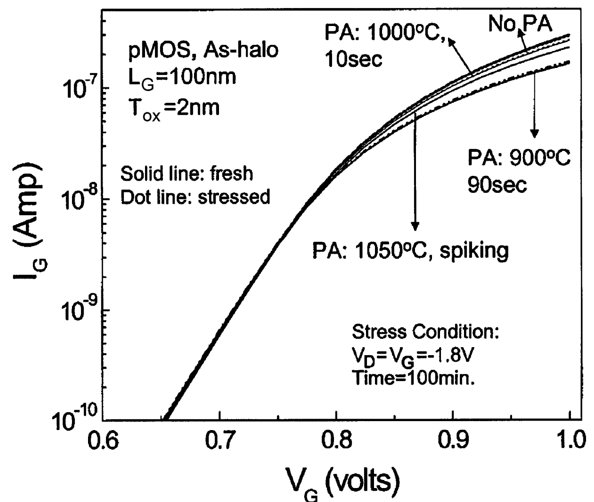

Fig. 13. Gate leakage ($I_{\rm G}$) as a function of gate voltage for differently post-annealed As-halo pMOSFETs before and after hot-carrier stress.

The hot-carrier-induced $I_{\rm Dsat}$ degradation versus stress time for three differently post-annealed As-halo pMOSFETs is

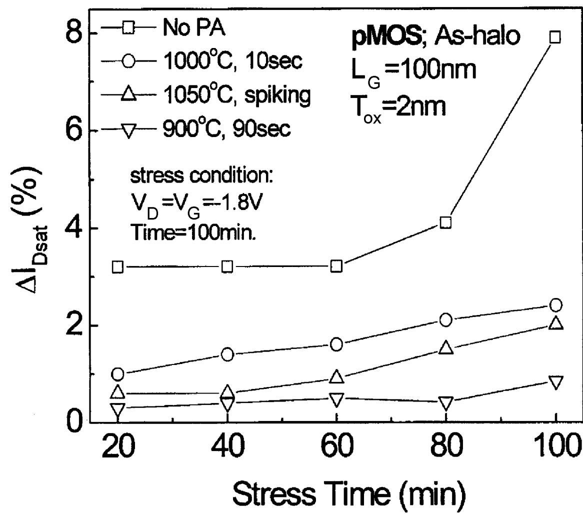

Fig. 14. Hot-carrier-induced degradation of saturated drain current ($I_{\rm Dsat}$) versus stress time for differently post-annealed As-halo pMOSFETs.

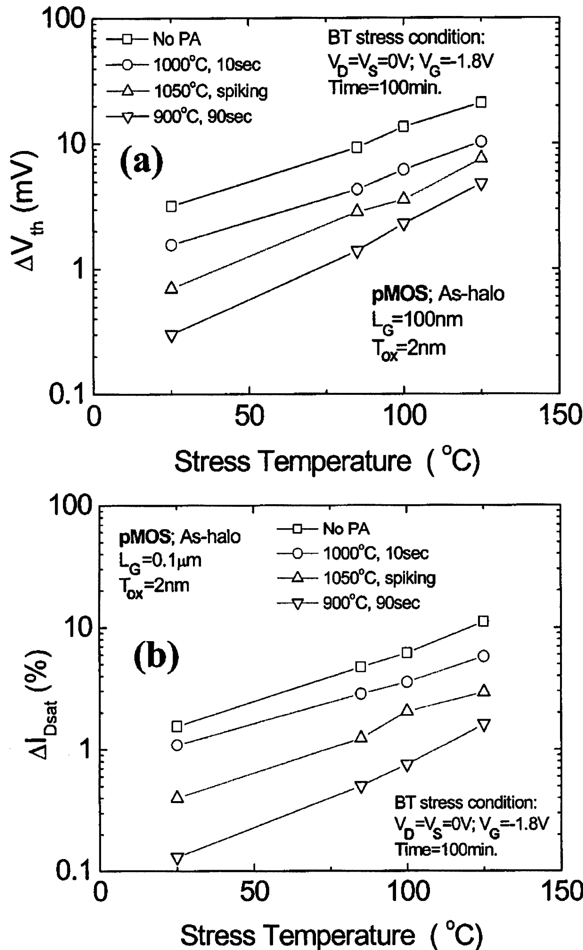

Fig. 15. Stress temperature dependence of (a) $V_{\rm th}$ shifts and (b) $I_{\rm Dsat}$ degradation for differently post-annealed As-halo pMOSFETs.

illustrated in Fig. 14. Apparently, the entire three PA are beneficial to the device's resistance against the hot-carrier stress. Fig. 15(a) and (15b) show, respectively, the $V_{\rm th}$ shift and $I_{\rm Dsat}$ degradation as a function of NBTI stress temperature for the differently post-annealed As-halo pMOSFETs. All PA devices show a higher resistance to NBTI-induced $V_{\rm th}$ shift and NBTI-induced $I_{\rm Dsat}$ degradation as compared to the device without any PA. We may conclude that a PA, in particular the long-time PA at 900 °C, can reduce the interface traps, thus improving the device's characteristic and reliability.

IV. Conclusion

In this work, the effect of post-thermal annealing treatment on the device characteristics and hot-carrier-induced reliability was investigated for the sub-100-nm CMOSFETs. For both In-halo nMOSFETs and As-halo pMOSFETs, the device characteristics and hot-carrier-induced device degradation can be improved by the post-thermal treatment, particularly the long-time post-annealing at medium temperature (e.g., 90-s RTP at 900 °C).

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