A Novel Four-Mask-Processed Poly-Si TFT Fabricated Using Excimer Laser Crystallization of an Edge-Thickened α-Si Active Island

Tien-Fu Chen, Ching-Fa Yeh, Chun-Yen Liu, and Jen-Chung Lou

***Abstract*—A novel four-mask-processed polycrystalline silicon thin-film transistor (poly-Si TFT) is fabricated using 50-pulse KrF excimer laser to crystallize an edge-thickened amorphous silicon (α-Si) active island without any shrinkage. This method introduces a temperature gradient in the island to enlarge grains from the edge, especially when the channel width is narrow. The grain boundaries across the width of the channel suppress the leakage current and the drain-induced barrier lowering. Moreover, the proposed poly-Si TFT with a channel length of $L = 2\ \mu$m and a channel width of $W = 1.2\ \mu$m possesses a high field-effect mobility of 260 cm^2/Vs and an on/off current ratio of 2.31×10^8.**

***Index Terms*—Anisotropic plasma etching, drain-induced barrier lowering (DIBL), excimer laser-annealed poly-Si, grain boundaries, leakage current, α-Si spacer.**

I. Introduction

LASER-ANNEALED polycrystalline silicon thin film transistors (poly-Si TFTs) have become the most promising candidates for use in active-matrix displays because they potentially enable peripheral drive circuits to be integrated into a panel [1]. The fabrication of high-mobility poly-Si TFTs by a lateral temperature modulation usually involves complex processes, such as the use of additional masks to enlarge channel grains [2], [3], and the application of homogenizing and shaping laser beam profiles to make the device performance uniform [4], [5]. Simplifying the processes involving in fabricating high-performance poly-Si TFTs is very important in replacing amorphous silicon (α-Si) TFT-based active-matrix displays [6]. Notably, the performance of conventional four-mask-processed poly-Si TFTs can be improved by the excimer laser crystallization of pre-patterned α-Si films [7], but surface tension shrinks the active islands [8], reducing the uniformity of the device performances. Hence, conventional poly-Si TFTs are fabricated by patterning precrystallized poly-Si films as active islands. However, unpatterned α-Si films cannot be directly irradiated using a continuous wave (CW) laser because the CW laser irradiation strips the film and thermally damages the glass substrate. An additional mask is used to pattern the α-Si films before the CW laser crystallization is performed [9]. In this letter, KrF excimer laser is used to crystallize α-Si islands whose edges are thickened by α-Si spacers formed by anisotropic plasma etching, and then the thickened edges are completely removed by anisotropic plasma etching with the top oxide as a protective layer, needing no additional mask. This method not only prevents α-Si islands from shrinking during crystallization, but also improves the device performance. The authors believe that this method can be applied to fabricate a high-performance poly-Si TFT with a neck to grow a single crystal of Si by appropriately modulating CW laser scanning in the source-drain direction [10], [11], since the edge-thickened α-Si active islands are very robust against laser-induced distortion.

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II. Device Fabrication

First, a 93-nm-thick α-Si layer was deposited on thermally oxidized (1.5 μm-thick) Si wafers by decomposing SiH_4 in a low-pressure chemical vapor deposition (LPCVD) system at 550 °C. Next, a 160-nm-thick low-temperature tetraethooxysilane (TEOS) oxide layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350 °C. A mask of active region was used to pattern the TEOS oxide layer. The under α-Si layer was directly etched by plasma following a slight lateral wet etching of the TEOS oxide, as shown in Fig. 1(a). After removing the top photoresists, a 93-nm-thick α-Si layer was deposited by LPCVD at 550 °C. Subsequently, edge-thickened α-Si islands were formed by anisotropic plasma etching with oxide as a stop layer, and then were crystallized by 50-pulse KrF excimer laser with energy density of around 335 mJ/cm^2 at a substrate temperature of 400 °C. Plasma etching was then used, first to reduce the thickness of the TEOS oxide using a low silicon-to-oxide selectivity, and last to remove completely the thickened edges of α-Si islands using a high silicon-to-oxide selectivity, as illustrated in Fig. 1(b). The proposed active islands were uniquely formed after the residual TEOS oxide was removed using a dilute hydrogen fluoride solution. In addition, the excimer laser-crystallized poly-Si films were patterned as the active islands of conventional poly-Si TFTs. Finally, the same steps were simultaneously implemented to finish the proposed and conventional poly-Si TFTs, such as a 110-nm-thick TEOS oxide layer as the gate insulator deposited by PECVD at 350 °C, a 170-nm-thick α-Si layer as the gate electrode deposited by LPCVD at 550 °C, a self-aligned ion implantation of phosphorous with a dosage of 5×10^{15} cm^{-2} at 35 keV, activation at 600 °C for 16 h

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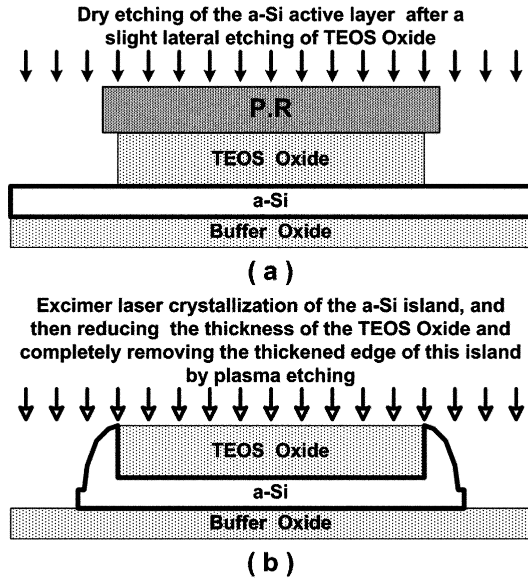


Fig. 1. Key processes for fabricating the laser-crystallized poly-Si island.

in a furnace with a nitrogen ambient, a 300-nm-thick TEOS passivation oxide layer deposited by PECVD at 350 °C, and sintering at 400 °C for 30 min. No further hydrogenation step was carried out.

III. Results and Discussion

Fig. 2 shows the SEM micrograph of excimer laser-crystallized poly-Si grains obtained after Secco etching of the proposed poly-Si island. The channel region was completely melted and the edge-thickened region was partially melted during 50-pulse excimer laser irradiation. The both regions have two different heights of the molten silicon, building a temperature gradient perpendicular to the source-drain direction and then facilitating the grain growth by the unmelted α-Si of the edge-thickened region as seeds. The top TEOS oxide not only releases the surface tension of the molten silicon [12], effectively suppressing the shrinkage of the island, but also acts as a heat source to reduce the quenching rate of the molten silicon [13]. Therefore, in addition to meeting each other at the center, some of the grains laterally elongated from the unmelted edge are merged while the channel width is narrow. Differences among sizes of grains in the conventional laser-crystallized poly-Si film cannot be prevented because of the applied laser with a Gaussian beam profile and a deviation of energy density of pulse-to-pulse. Therefore, the channels in the proposed poly-Si TFTs exhibit a more regular arrangement of grains as compared with the channels in the conventional poly-Si TFTs. After defining pre-crystallized poly-Si films as active islands, the conventional poly-Si TFTs have grain boundaries randomly distributed within the channel regions, resulting in a poor uniformity of device performance.

Fig. 3(a) shows the transfer characteristics of the proposed and conventional poly-Si TFTs with a channel length of 2 μm and a channel width of about 1 μm. Notably, the on/off current ratios at $V_{\rm DS} = 5$ V are 2.31×10^8 for the proposed poly-Si TFT and 2.15×10^7 for the conventional TFT. This difference of one order of magnitude is mainly attributable to the difference in leakage current. Besides, the shift of threshold voltage $\Delta V_{\rm th}$ is

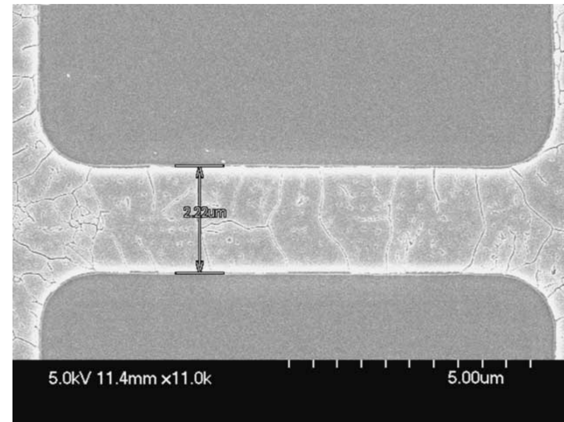
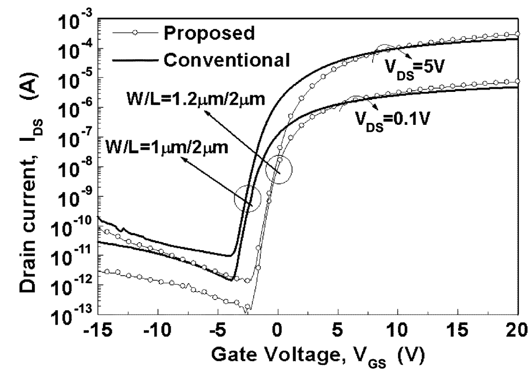
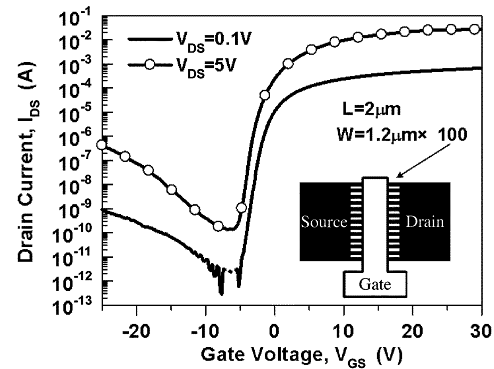


Fig. 2. SEM photograph of excimer laser-crystallized poly-Si island after secco etching.



(a)



(b)

Fig. 3. Transfer characteristics of (a) the proposed and conventional poly-Si TFTs with channel widths of about 1 μm and (b) the proposed poly-Si TFT with 100 channel units.

defined as $V_{\rm th,1}$–$V_{\rm th,2}$ where $V_{\rm th,1}$ denotes $V_{\rm GS}$ of drain current of $(W/L) \times 10^{-8}$ A at $V_{\rm DS} = 0.1$ V and $V_{\rm th,2}$ represents $V_{\rm GS}$ of the drain current of $(W/L) \times 10^{-7}$ A at $V_{\rm DS} = 5$ V. The $\Delta V_{\rm th}$ of 0.23 V in the proposed poly-Si TFT is smaller than that of 0.80 V in the conventional poly-Si TFT. Those results imply that the grain boundaries perpendicular to the direction of current flow suppress the leakage current [14] and the drain-induced barrier lowering (DIBL) in the proposed poly-Si TFTs. However, preventing grain boundaries from lying across from the source to drain is difficult in the conventional poly-Si TFTs, and such grain boundaries provide extra paths for current and cause punchthrough effects as the channel length is shortened.

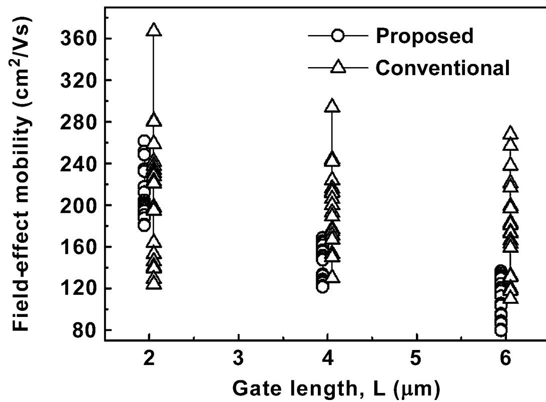


Fig. 4. Dependence of field-effect mobility on the channel length given channel widths from 1 to 4 μm for the proposed and conventional poly-Si TFTs. The field-effect mobility was evaluated at $V_{\rm DS} = 0.1$ V.

Therefore, the proposed poly-Si TFTs simultaneously benefit more from device scaling than the conventional poly-Si TFTs. By dividing the channel width into narrow units, an on/off current ratio of eight orders of magnitude at $V_{\rm DS} = 5$ V is also obtained from the proposed poly-Si TFT with $L = 2$ μm and $W = 1.2$ μm $\times$ 100 as shown in Fig. 3(b). The self-heating reliability of a TFT with divided channel units can be further improved due to the rapid heat diffusion when the TFT is operated in a high drain current [15], [16].

Fig. 4 shows the dependence of field-effect mobility on the channel length for the proposed and conventional poly-Si TFTs. The twenty TFTs with channel widths from 1 μm to 4 μm for each channel length are included. The maximum mobility of the proposed poly-Si TFTs decreases as the channel length increases, indicating that grain boundaries perpendicular to the direction of current flow act as strong scattering centers that limit the transport of carriers. However, mobility of some conventional TFTs larger than that of the proposed TFTs is obtained due to the instability of the applied laser, resulting in a large variation of field-effect mobility of the conventional poly-Si TFTs. This result suggests that the proposed method can partially compensate for the nonuniform beam profile and the unstable pulse-to-pulse energy density of the applied laser.

IV. Conclusion

The surface tension-induced shrinkage effect of multipulse excimer laser irradiation on pre-patterned α-Si films was successfully eliminated through the edge-thickened method. The proposed method can make uniform the performance of poly-Si TFTs due to the regular arrangement of the channel grains by the lateral modulation of temperature. The proposed TFTs with divided channel units can meet the application of various gate widths, and their performances depend on the grain-boundary control of each channel unit. Hence, how to further control the quality of a channel unit is still the major concern of the proposed TFTs.

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