The Impact of MOSFET Layout Dependent Stress on High Frequency Characteristics and Flicker Noise

Kuo-Liang Yeh, Chih-You Ku, and Jyh-Chyurn Guo

Institute of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan
Tel: +886-3-5131368, Fax: +886-3-5724361, E-mail: jcguo@mail.nctu.edu.tw

***Abstract* —Layout dependent stress in 90 nm MOSFET and its impact on high frequency performance and flicker noise has been investigated. Donut MOSFETs were created to eliminate the transverse stress from shallow trench isolation (STI). Both NMOS and PMOS can benefit from the donut layout in terms of higher effective mobility μ_{eff} and cutoff frequency f_T, as well as lower flicker noise. The measured flicker noise follows number fluctuation model for NMOS and mobility fluctuation model for PMOS, respectively. The reduction of flicker noise suggests the reduction of STI generated traps and the suppression of mobility fluctuation due to eliminated transverse stress using donut structure.**

***Index Terms* — Donut, Shallow-Trench Isolation (STI), Stress, Mobility, Flicker noise**

I. Introduction

With the advancement of CMOS technology to nanoscale regime, the stress introduced from materials and process become more sensitive to the device layout and topography. The shallow trench isolation (STI) process will induce compressive stress and traps, which may have impact on flicker noise (i.e., 1/f noise) in NMOS and PMOS devices. [1] Layout-dependent stress from STI and its impact on high frequency characteristics as well as flicker noise has been investigated but limited to NMOS [2]-[3]. A minor layout modification, namely edge-extended was implemented to reduce the stress and traps introduced by STI [2]. However, the edge-extended layout cannot eliminate the gate-to-STI edge overlap region and leaves STI stress an impact factor. A ring type device was proposed, trying to solve the mentioned problem and identify the influence on flicker noise [3]. However, the study is limited to the stress along the gate width, i.e. transverse to the channel (transverse stress $\sigma_{\perp}$) and the impact on high frequency performance is unknown. Furthermore, both studies of edge-extended and ring type layouts did not cover PMOS, which is even more important than NMOS for low phase noise design.

In this paper, a new MOSFET layout, namely doughnut (donut) is proposed to create devices free from transverse STI stress, along the gate width.. Meanwhile, an extensive investigation is performed on both NMOS and PMOS devices to explore the STI stress effect on channel current, cutoff frequency (f_T) and flicker noise. For each device structure under a specified bias, the flicker noise is averaged from several different dies to represent statistics of die-to-die variation. This work is aimed to identify the impact from STI stress on high frequency characteristics as well as flicker noise and the results can guide MOSFET layout optimization for RF and analog circuit design.

II. Device Fabrication and Characterization

In this work, the devices were fabricated in 90nm CMOS process, with 90nm gate length drawn on the layout L_{drawn} and the total gate width W_{tot} fixed at 64μm. In order to investigate the stress and interface traps generated near STI edge, two types of MOSFET layouts, namely standard and donut are designed and implemented. Standard device means multi-finger structure with finger width W_F=2 μm and finger number N=32. As shown in Fig. 1, donut MOSFETs are constructed as 4-side polygons in which the corners contribute very little to the channel current [4]. In this work, donut devices with two layout dimensions are implemented. In Fig. 1(a), D1S1 represents donut MOSFET in which the space from poly gate to STI edge follows the minimum rule, i.e. 0.3μm, to maximize the compressive stress from STI and along the channel (i.e., longitudinal stress $\sigma_{//}$). Meanwhile, D10S10 shown in Fig. 1(b) denotes donut MOSFET with 10 times larger space between poly gate and STI edge, i.e. 3μm, intentionally to relax $\sigma_{//}$ from STI.

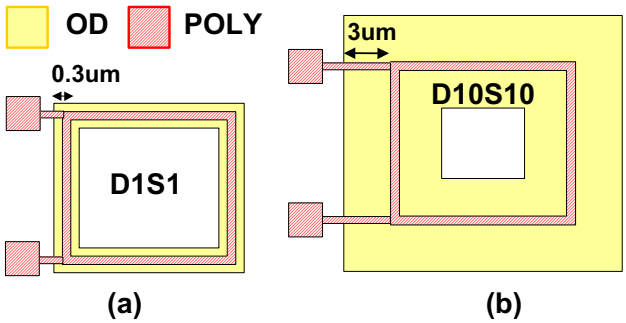

Fig. 1 A brief layout of donut MOSFET (a) D1S1 and (b) D10S10, with two major layers, such as active region (OD) and poly gate (PO)

978-1-4244-6241-4/978-1-4244-6242-1/
978-1-4244-6243-8/10/$26.00 © 2010 IEEE

S-parameters were measured by Agilent E8364B network analyzer for high frequency characterization and AC parameters extraction. Open and short deembedding was performed to remove the parasitic capacitances from the pads as well as interconnection lines and the resistances from all of the metal interconnect. The power spectral density (PSD) of drain current noise, namely S_{ID} was measured by low frequency noise (LFN) measurement system, consisting of Agilent dynamic signal analyzer (DSA 35670) and low noise amplifier (LNA SR570). The LFN measurement generally covers a wide frequency range from 4Hz to 10k Hz. The LFN was measured under various gate-over-drive ($|V_{GT}|$=0.1~0.7V) and $|V_{DS}|$=50mV for both NMOS and PMOS.

III. Results and Discussion

At first, STI stress introduced in MOSFETs with three different layouts as mentioned (standard, donut D1S1 and D10S10) is illustrated in **Fig.2** to assist an analysis and understanding of layout effect on STI stress and then the electrical characteristics. Note that STI stress is classified as longitudinal stress, denoted as $\sigma_{//}$, which is in parallel with the channel, and transverse stress, namely $\sigma_{\perp}$, which is transverse to the channel. We can see that standard MOSFETs (Fig.2(a)) are subject to $\sigma_{//}$ along the channel length and $\sigma_{\perp}$ along the gate width. On the other, donut MOSFETs are free from $\sigma_{\perp}$. Regarding the stress favorable for mobility enhancement, it has a critical dependence on the device types and orientations, as shown in **Table I [5]**. For NMOS, tensile stress, either $\sigma_{//}$ or $\sigma_{\perp}$ can improve μ_{eff}. As for PMOS, compressive stress in $\sigma_{//}$ or tensile stress in $\sigma_{\perp}$ is the right one for μ_{eff} enhancement.

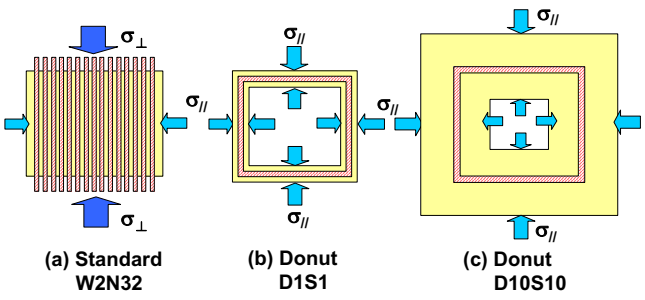

Fig. 2 Schematics of STI stress in MOSFETs with three different layouts (a) standard multi-finger device W2N32 (b) donut device D1S1 (c) donut device D10S10. Longitudinal stress : $\sigma_{//}$ in parallel with the channel, transverse stress : $\sigma_{\perp}$ transverse to the channel.

TABLE I

Stress favorable for mobility enhancement in NMOS and PMOS along longitudinal and transverse directions **[5]**

Directions	Stress favorable for mobility enhancement	
	NMOS	PMOS
Longitudinal ($\sigma_{//}$)	Tensile	Compressive
Transverse ($\sigma_{\perp}$)	Tensile	Tensile

A. DC Performance of Standard and Donut NMOS

Fig.3(a) presents the maximum transconductance $G_{m,max}$ measured from NMOS. It is found that $G_{m,max}$ of D1S1 is degraded by around 9.7% but that of D10S10 is enhanced by 7.5% as compared with the standard device. The experimental suggests the compressive $\sigma_{//}$ from STI, which is maximized in D1S1 due to the minimum gate to STI space is the primary factor responsible for $G_{m,max}$ degradation. As for D10S10, the much lower $\sigma_{//}$ due to 10 times larger space and eliminated $\sigma_{\perp}$ for donut layout contributes to $G_{m,max}$ improvement. The influence on effective mobility μ_{eff} shown in Fig. 3(b) reveals exactly the same trend. D1S1 suffers 9.2% degradation while D10S10 gain 7.45% enhancement in μ_{eff}. The results justify the mechanism that the layout dependence of $G_{m,max}$ is originated from the effect of STI stress $\sigma_{//}$ and $\sigma_{\perp}$ on electron mobility summarized in Table I.

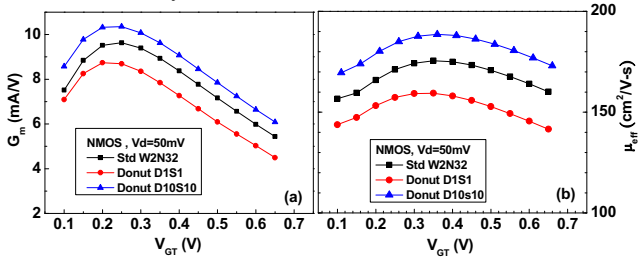

Fig. 3 (a) The transconductance G_m and (b) effective mobility μ_{eff} and extracted from linear I-V for standard and donut NMOS with different poly-gate to STI edge distances, D1S1 and D10S10 defined in Fig.1.

B. DC Performance of Standard and Donut PMOS

As for PMOS, the donut devices D1S1 and D10S10 demonstrate 12.2% and 7.6% higher $G_{m,max}$ than the standard one shown in Fig.4(a). Again, the layout dependence of μ_{eff} illustrated in Fig.4(b) indicates the same trend as that of $G_{m,max}$. The donut PMOS, D1S1 and D10S10 present 12.5% and 6.3% μ_{eff} enhancement compared to the standard device. According to Table I, it is believed that D1S1 with the min. gate to STI edge distance, resulting the highest compressive $\sigma_{//}$ and minimized $\sigma_{\perp}$ can benefit the most in hole mobility. The standard PMOS with relieved $\sigma_{//}$ in multi-finger structure and largest $\sigma_{\perp}$ along narrow width suffers the worst hole mobility.

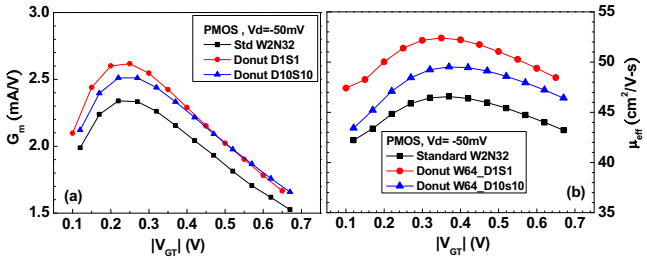

Fig. 4 (a) The transconductance G_m and (b) effective mobility μ_{eff} and extracted from linear I-V for standard and donut PMOS with different poly-gate to STI edge distances, D1S1 and D10S10 defined in Fig.1

C. High Frequency Performance of Donut and Standard MOSFETs

The impact from layout dependent STI stress on high frequency performance is of special concern for RF MOSFETs and circuits design. Fig. 5(a) and (b) illustrate the cutoff frequency f_T measured from NMOS and PMOS with donut and standard layouts. Note that f_T is extracted from the extrapolation of $|H_{21}|$ to unity gain. For NMOS in Fig.5(a), D10S10 gains 5% improvement in the maximum f_T compared to the standard and D1S1. The benefit from donut layout becomes particularly larger for PMOS. As shown in Fig.5(b), D1S1 presents the best performance with the highest f_T and realizes 28% increase in the maximum f_T than the standard device.

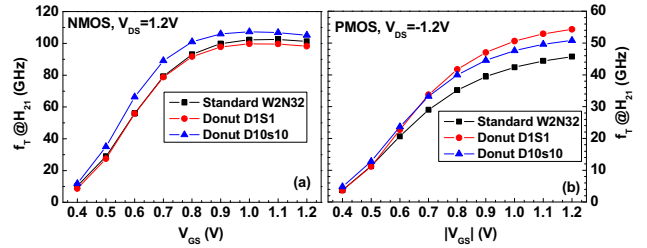

Fig. 5 The cut-off frequency f_T vs. V_{gs} measured for standard and donut devices (a) NMOS (b) PMOS. Standard : multi-finger W2N32. Donut : D1S1 and D10S10.

The resulted improvement on f_T in donut MOSFETs can be consistently explained by the enhancement of μ_{eff} and G_m. Referring to (1), an analytical model for calculating f_T **[6],** it is predicted that f_T is proportional to G_m and the enhancement of G_m can boost f_T under fixed gate capacitances (C_{gg} and C_{gd}). **Fig.6(a) and (b)** present C_{gg} measured from NMOS and PMOS with three different layouts. The results indicate much smaller difference in C_{gg} between donut and standard layouts, as compared with G_m (Fig.3 and Fig.4). Thus, layout dependence of f_T just follows that of G_m.

$$f_T = \frac{G_m}{2\pi\sqrt{C_{gg}^2 - C_{gd}^2}} \quad (1)$$

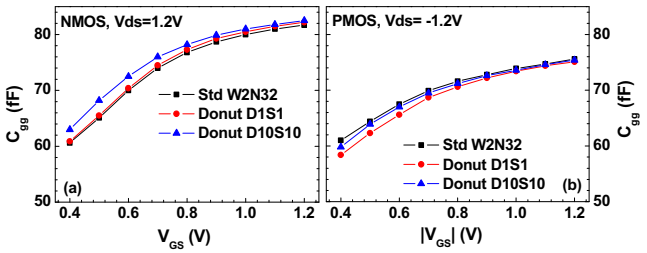

Fig. 6 C_{gg} vs. V_{gs} extracted from Y-parameters for standard and donut devices (a) NMOS (b) PMOS. Standard : multi-finger W2N32. Donut : D1S1 and D10S10.

Regarding other RF performance parameters, such as maximum oscillation frequency, f_{max} and noise figure, NF_{min} (not shown), the donut MOSFETs suffer significant degradation due to inherently larger gate resistances than the standard one with multiple gate fingers. The experimental suggests an innovative donut device layout is required to cover all of the RF and analog performance.

D. Low Frequency Noise of Standard and Donut MOSFETs

Fig. 7(a) and (b) make a comparison of LFN in terms of S_{ID}/I_D^2 between the standard and donut devices for NMOS and PMOS, respectively. The noise spectrum follows 1/f characteristics over a wide frequency domain from 4 to 10K Hz. It means that the measured LFN is a typical flicker noise. The standard device reveals near twice larger S_{ID}/I_D^2 as compared to donut devices for both NMOS and PMOS, under a specified gate overdrive voltage, $|V_{GT}|$=0.7V. In contrast, the donut device D10S10 with the most extended gate to STI-edge distance indicates the lowest S_{ID}/I_D^2. The results can be consistently explained by the fact that D10S10 can keep free from $\sigma_{\perp}$ as well as interface traps near STI edge, and the smallest $\sigma_{//}$ due to 10 times larger space away from the STI edge compared to D1S1.

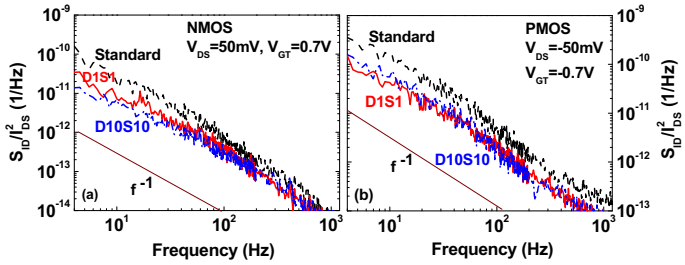

Fig. 7 The low frequency noise S_{ID}/I_{DS}^2 measured for the standard and donut devices (a) NMOS (b) PMOS. Standard : multi-finger W2N32. Donut : D1S1 and D10S10.

To further explore the mechanism responsible for LFN, the measured S_{ID}/I_{DS}^2 at frequency 50Hz are plotted versus

I_{DS} for three different devices, under various $|V_{GT}|$ (0.1~0.7V) shown in Fig.8 (a) and b) for NMOS and PMOS, respectively. For nMOS devices, the measured LFN characteristic is dominated by number fluctuation model given by (2) in which S_{ID}/I_{DS}^2 is proportional to N_t/I_{DS}^2 and that predicts the increase of LFN with increasing the traps density N_t **[7].** It is believed that the gate to STI-edge overlap region will suffer the most severe compressive strain as well as interface traps N_t**,** and the donut devices can eliminate these effects along the gate width, i.e. in the transverse direction. According to previous study, the stress generated traps may aggravate the scattering effect and increase the flicker noise [8]. The mentioned mechanism can explain why the donut devices free from gate to STI-edge overlap region can have the lowest LFN.

$$\frac{S_{ID}}{I_{DS}^2} = \frac{q^2 k_B T \lambda N_t}{f^{\gamma}} \frac{WC_{ox}\mu_{eff}^2 V_{DS}^2}{L^3} \frac{1}{I_{DS}^2} \quad (2)$$

N_t : *the density of traps at quasi - Fermi level*

As for PMOS shown in Fig.8(b), the measured S_{ID}/I_{DS}^2 follows a simple power law of $1/I_{DS}$ and manifests itself governed by mobility fluctuation model, according to Hooge empirical formula expressed in (3) **[9]**. Note that the Hooge parameter α_H is dimensionless and may vary with biases and process technologies. The reduction of LFN measured from donut PMOS suggests the suppression of mobility fluctuation due to the eliminated compressive $\sigma_{\perp}$.

$$\frac{S_{ID}}{I_{DS}^2} = \frac{1}{f} \frac{\alpha_H \mu_{eff}}{L^2} \frac{qV_{DS}}{I_{DS}} \quad (3)$$

α_H : *the Hooge parameter*

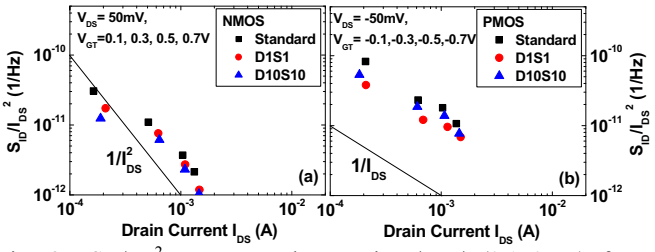

Fig. 8 S_{ID}/I_{DS}^2 vs. I_{DS} under varying $|V_{GT}|$ (0.1~0.7V) for standard and donut devices (a) NMOS (b) PMOS. Standard : multi-finger W2N32. Donut : D1S1 and D10S10.

IV. CONCLUSION

The proposed donut MOSFETs demonstrate the advantages over the standard MOSFETs, such as the lowest S_{ID}/I_{DS}^2 in low frequency domain (1~ 10K Hz) and higher f_T in very high frequency region (100/50 GHz for N/P MOS). The elimination of STI stress and excess traps along the gate width is validated as the primary mechanism responsible for the enhancement of μ_{eff} as well as f_T, and reduction of LFN. The layout dependent stress mechanism can be applied to both NMOS and PMOS, even though their LFN are governed by different models. An innovative donut device layout for solving the potential degradation of f_{max} and NF_{min} emerges as an interesting and important topic in the future work for RF and analog applications.

ACKNOWLEDGEMENT

This work is supported by NSC98-2221-E009-166-MY3. Besides, the authors acknowledge the support from NDL RF Lab. for noise measurement and Chip Implementation Center (CiC) for device fabrication.

REFERENCES

[1] T. Ohguro, Y. Okayama, K. Matsuzawa, K. Matsunaga, N. Aoki, K. Kojima, H. S. Momose, and K. Ishimaru, "The impact of oxynitride process, deuterium annealing and STI stress to 1/f noise of 0.11μm CMOS", in *Symp. on VLSI Tech*., 2003, pp. 37–38.

[2] C.-Y. Chan, Y.-S. Lin, Y.-C. Huang, S. S. H. Hsu, and Y.-Z. Juang, "Edge-extended Design for Improved Flicker Noise Characteristics in 0.13-μm RF NMOS", in *IEEE MTT-S Intl. Microwave Symp.* 3-8 June, 2007, pp.441-444.

[3] Y.-L. R. Lu, Y.-C. Liao, W. McMahon, Y-H. Lee, Helen Kung, R. Fastow, and S. Ma, "The Role of Shallow Trench Isolation on Channel Width Noise Scaling for Narrow Width CMOS and Flash Cells", in *Int. Symp. on VLSI TSA*, 21-23 April, 2008, pp. 85–86.

[4] P. L'opez, M. Oberst, H. Neubauer, D. Cabello and J. Hauer, "Performance analysis of high-speed MOS transistors with different layout styles", IEEE Int. Symposium on Circuits and Systems, Kobe, Japan, 23-25 May, 2005.

[5] Y. Luo and D. K. Nayak, "Enhancement of CMOS performance by process-induced stress" IEEE Trans. Semicond. Manuf., vol. 18, no. 1, pp. 63–68, Feb. 2005.

[6] Tajinder Manku, "Microwave CMOS—Device Physics and Design", IEEE Journal of Solid-State Circuits, vol. 34, no. 1, Mar. 1999, pp. 277-285.

[7] G. Reimbold, "Modified 1/f trapping noise theory and experiments in MOS transistors biased from weak to strong inversion-influence of interface states," IEEE Trans. Electron Devices, vol. ED-31, pp. 1190-1198, 1984.

[8] S. Maeda, Y. S. Jin, J. A. Choi, S. Y. Oh, H. W. Lee, J. Y. Woo, M. C. Sun, J. H. Ku, K. Lee, S. G. Bae, S. G. kang, J. H. Yang, Y. W. Kim, K. P. Suh, " Impact of Mechanical Stress Engineering on Flicker Noise Characteristics," in *Symp. on VLSI Tech.*, June 2004, pp.102-103.

[9] F. N. Hooge, *et al*., "Lattice scattering causes 1/f noise," Phys. Lett. A, vol. 66, pp. 315-316, 1978.