Resonator-based multi-stage ΣΔ modulator for wideband applications with improved dynamic range

T.-H. Chang and L.-R. Dung

A new design methodology for wideband, multi-stage, multi-bit ΣΔ modulators (ΣΔMs) with improved dynamic range, is presented. The key to improving dynamic range is to have the first stage oscillated, then the coarse quantisation noise vanishes and hence circuit nonlinearities do not cause a leakage quantisation noise problem. Based on the proposed methodology, a fourth-order four-bit ΣΔM can achieve the dynamic range of 80 dB at the OSR of 8 without using additional calibration techniques.

Introduction: With increasing demand of ΣΔ modulators (ΣΔMs) with broader bandwidth and wider dynamic range (DR), the multi-stage multi-bit architecture becomes attractive for this trend. It not only achieves high-order noise shaping without a stability problem, but also alleviates the effect of digital-to-analogue converter (DAC) error of the modulator. However, the leakage coarse quantisation noise caused by circuit nonlinearities seriously degrades the DR of modulator. Several calibration techniques have been proposed to improve this degradation, but they usually require the additional digital or analogue circuits. In this Letter, a new design methodology for multi-stage, multi-bit ΣΔM is proposed to effectively extend bandwidth and improve the DR with neither calibration nor trimming techniques.

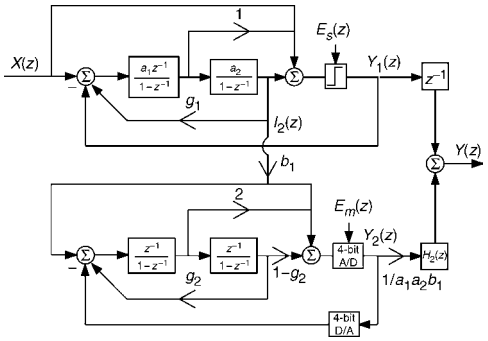

Fig. 1 *Proposed two-stage, resonator-based ΣΔM*

Proposed methodology: Our approach is based on two resonator topologies, the single-delay resonator (SDR) and the double-delay resonator (DDR). Fig. 1 shows the proposed two-stage resonator-based ΣΔM, where the first stage is an SDR-based single-bit structure and the second stage is a DDR-based multi-bit one. After analysing, the input of the second stage can be written as:

$$I_2(z) = \frac{z^{-1}}{D(z)}[(a_1a_2 - q)X(z) - a_1a_2E_S(z)] \tag{1}$$

The final modulator output after digital cancellation logic can be formulated as (2), where $\mathrm{NTF}_{SDR}(z)$ and $\mathrm{NTF}_{DDR}(z)$ denote the noise transfer functions (NTF) of SDR- and DDR-based structures:

$$Y(z) = z^{-1}X(z) + \frac{1}{a_1a_2b_1}H_2(z)NTF_{DDR}(z)E_m(z) \tag{2}$$

where

$$H_2(z) = 1 - (2 - a_1a_2g_1)z^{-1} + z^{-2} \tag{3}$$

$$NTF_{DDR}(z) = 1 - 2z^{-1} + (1 + g_2)z^{-2} \tag{4}$$

In (1) and (2), $X(z)$ and $Y(z)$ represent the input and output of the modulator, respectively; $E_s(z)$ and $E_m(z)$ are the respective quantisation noise of the single-bit and four-bit quantisers. The $D(z)$ is the denominator of $\mathrm{NTF}_{SDR}(z)$ and q is the gain of the single-bit quantiser. The digital cancellation filter $H_2(z)$ is essentially equal to the numerator of $\mathrm{NTF}_{SDR}(z)$.

From (2), it is observed that each stage contributes a pair of complex zeros into the NTF of the modulator. The NTF with zeros has been proved to be effective in wideband applications and article [1] addresses the optimal placing of zeros for obtaining the maximum amount of quantisation noise suppression. Based on that approach, the optimised loop gains of SDR and DDR, respectively, turn out to be:

$$a_1a_2g_1 = 0.7416\frac{\pi^2}{OSR^2} \tag{5}$$

$$g_2 = 0.1156\frac{\pi^2}{OSR^2} \tag{6}$$

Unfortunately, in practice, any inconsistency between the numerator of the $\mathrm{NTF}_{SDR}(z)$ and $H_2(z)$ can result in leakage coarse quantisation noise and hence degrade the DR of the modulator. This inconsistency is usually caused by circuit nonlinearities, such as finite opamp gain and capacitor mismatching. To alleviate the circuit nonlinearities, we intentionally let the first stage operate in oscillation mode. When the first stage is operating in oscillation mode, the feedback path from the single-bit quantiser output to the input summing node is disabled and hence the modulator output is free of the coarse quantisation noise terms. Depending on the input amplitude, the first stage, based on the SDR single-bit structure, can operate in either modulation mode or oscillation mode. When the input amplitude is less than a threshold level, the first stage oscillates because its NTF has infinite gain at resonance frequency [2]. Note that the DDR structure in the second stage has not this oscillation mode to ensure the successful analogue-to-digital conversion of the modulator. Once the first stage is operating in oscillation mode, (1) and (2) become:

$$I_{2,osc}(z) = \frac{a_1a_2z^{-1}}{1 - (2 - a_1a_2g_1)z^{-1} + z^{-2}}X(z) + R(z) + T(z) \tag{7}$$

$$Y_{osc}(z) \cong z^{-1}X(z) + \frac{1}{a_1a_2b_1}H_2(z)NTF_{DDR}(z)E_m(z) \tag{8}$$

where $R(z)$ and $T(z)$ represent the oscillating signal of the SDR and a single-tone signal at $f_s/2$, respectively. Obviously, from (7), the coarse quantisation noise is dismissed in oscillation mode.

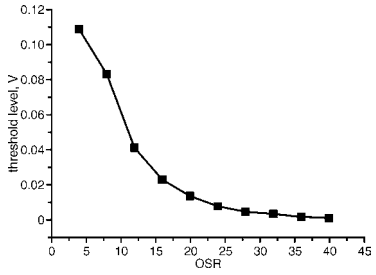

Fig. 2 *Threshold voltage level against OSR*

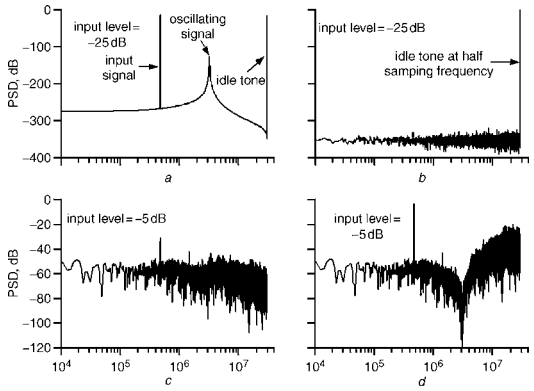

Fig. 3 *Output spectra of first stage with two operating modes*

a FFT of $I_2(z)$ in oscillation mode
b FFT of $Y_1(z)$ in oscillation mode
c FFT of $I_2(z)$ in modulation mode
d FFT of $Y_1(z)$ in modulation mode

Because of the absence of coarse quantisation noise, the modulator does not suffer from the DR degradation caused by circuit nonlinearities. Because of the deeply-notched filtering of $H_2(z)$ at oscillating frequency, the oscillation signal can be suppressed after digital cancellation logic. As shown in Fig. 2, the threshold level of oscillation depends on the OSR of the modulator. Accordingly, the lower the OSR, the higher the threshold level. It is implies that the DR can be significantly improved when OSR is low. Thus, the proposed resona-

tor-based modulator is quite suitable for wideband applications. Yet, when the first stage operates in modulation mode, the leakage coarse quantisation noise occurs and limits the achievable peak signal-to-noise (SNR) of the modulator. Because of the NTF with additional zeros, the proposed modulator still has higher peak SNR compared to the conventional multi-stage one.

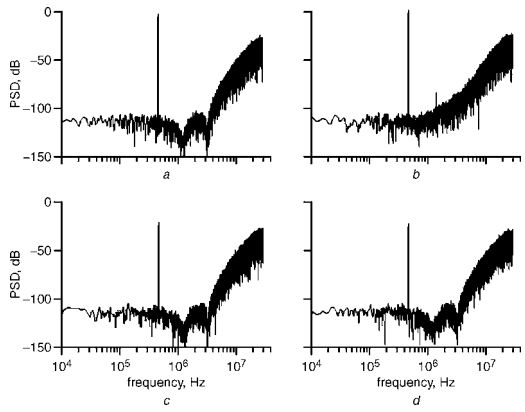

Fig. 4 *Output spectra of proposed ΣΔM with circuit nonlinearities*

a FFT of modulator output in modulation mode; ideal case, SNDR = 80 dB
b FFT of modulator output in modulation mode; ideal non-ideal case, SNDR = 67 dB
c FFT of modulator output in oscillation mode; ideal case, SNDR = 63 dB
d FFT of modulator output in oscillation mode; non-ideal case, SNDR = 63 dB

Simulation results and discussion: Given a sampling rate of 60 MHz and a fixed OSR of 8, we employ Matlab® to perform simulation on a fourth-order, four-bit resonator-based ΣΔM with a practical integrator model proposed in [3]. In the simulation, the DC gain, slew rate, unity-gain bandwidth, and saturation voltage of opamp are set to 50 dB, 150 V/μs, 300 MHz, and ±1 V, respectively. The capacitor mismatching of the modulator is set to 1%. The conventional fourth-order, four-order ΣΔM [4] with the same circuit specifications is also simulated for comparison. The output spectra of the first stage with two operating modes are shown in Fig. 3. Based on these two modes of operation, Fig. 4 shows the output spectra of the proposed two-stage ΣΔM with circuit nonlinearities. It can be observed that the SNR of the modulator in oscillation mode is insensitive to circuit nonlinearities. Fig. 5 illustrates the SNR curves against input amplitude. As the simulation result shows, the proposed fourth-order, four-bit ΣΔM can achieve the dynamic range of 80 dB at the OSR of 8 without using additional calibration techniques. Therefore, the proposed modulator does significantly improve DR for wideband application. Also, this novel design methodology can be applied to a bandpass ΣΔM by replacing the second stage with the bandstop-NTF structure.

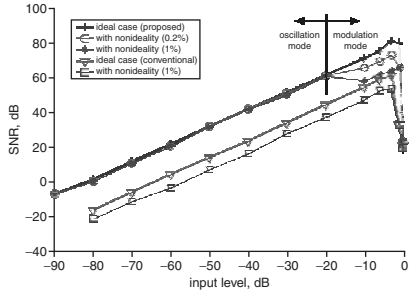

Fig. 5 *SNR curves against input amplitude in proposed ΣΔM (OSR = 8)*

21 February 2004
Electronics Letters online no: 20040450
doi: 10.1049/el:20040450

T.-H. Chang and L.-R. Dung (*Department of Electrical and Control Engineering, National Chiao Tung University, 1001 TA Hsueh Road, Hsinchu 30050, Taiwan, Republic of China*)

References

1 Schreier, R.: 'An empirical study of high-order single-bit delta-sigma modulators', *IEEE Trans. Circuits Syst. II*, 1993, **40**, pp. 461–466
2 Lee, W.L., and Sodini, C.G.: 'A topology for higher order interpolative coders'. Proc. IEEE Int. Symp. Circuits and Systems, Philadelphia, PA, USA, May 1987, pp. 459–462
3 Malcovati, P., *et al.*: 'Behavior modeling of switched-capacitor sigma-delta modulators', *IEEE Trans. Circuits Syst. I*, 2003, **50**, pp. 352–364
4 Medeiro, F., *et al.*: 'Fourth-order cascade SC ΣΔ modulators: a comparative study', *IEEE Trans. Circuits Syst. I*, 1998, **45**, pp. 1041–1051