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## Deep depletion phenomenon of SrTiO<sub>3</sub> gate dielectric capacitor

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SrTiO<sub>3</sub> (STO) thin films were deposited on *p*-type silicon substrate by radio-frequency (rf) magnetron sputtering in an Ar–O<sub>2</sub> and Ar–N<sub>2</sub> mixed ambient to form metal/insulator/semiconductor (MIS) structure. We found the Schottky emission and Fowler–Nordheim tunneling mechanisms as responsible for the leakage current in the STO-based MIS structures at low and high electric fields under negative bias voltage, respectively. On the other hand, it was also observed that the generation current dominated the leakage mechanism at the high electric field under positive bias voltage due to the highly leaky insulator and lack of electrons. To maintain the leakage current at the higher electric field, the depletion width would broaden to generate more electrons, which is called deep depletion. Therefore, deep depletion was induced by high leakage current density under positive bias voltage. We also investigated the correlation between deep depletion and the leakage mechanism in STO-based gate dielectric capacitors under positive bias voltage to extract the generation lifetime of silicon substrates. The extracted generation lifetime can be used to examine the quality of silicon substrates after different processing conditions. © 2004 American Institute of Physics. [DOI: 10.1063/1.1704850]

### I. INTRODUCTION

Device scaling was the main method adopted by the semiconductor industry to increase the packing density and performance of various types of electronic devices in the past decade. Based on the International Technology Roadmap for Semiconductor (ITRS), the equivalent oxide thickness (EOT) of gate dielectrics in the transistors should be less than 2 nm in the near future.<sup>1</sup> However, the conventional SiO<sub>2</sub> gate dielectric of thickness less than 2 nm will give rise to several issues, including high gate leakage current, reduced drive current, reliability degradation, boron penetration, and the necessity to grow ultrathin and uniform SiO<sub>2</sub> layers. Improvement in thin film processing can solve most of these issues, except the high gate leakage current caused by direct tunneling, which is the fundamental physical limit in device scaling. Therefore, scaling the effective gate dielectric thickness to less than 2 nm will require alternative materials with higher permittivities and greater physical thicknesses to prevent direct gate tunneling. Recent studies have shown that the gate tunneling current is significantly reduced with the use of the high-*k* gate dielectrics, such as ZrTiO<sub>4</sub>,<sup>2</sup> Al<sub>2</sub>O<sub>3</sub>,<sup>3</sup> HfO<sub>2</sub>,<sup>4</sup> ZrO<sub>2</sub>,<sup>5</sup> and SrTiO<sub>3</sub>. Among many possible candidates for high-*k* gate dielectrics, STO provides special functions because it can be epitaxially grown on silicon substrates, resulting in an interfacial trap density of 10<sup>10</sup>–10<sup>11</sup> cm<sup>-2</sup> eV<sup>-1</sup>, which is as good as that in Si/SiO<sub>2</sub> interfaces.<sup>6</sup> In metal/ferroelectric/insulator/semiconductor (MFIS) capacitors, STO could match the ferroelectric material to reduce the operation voltages of the capacitors due to its high dielectric constant.<sup>7</sup> Furthermore, STO is a

perovskite-type material which provides a good buffer layer for the growth of perovskite-type ferroelectric thin films.

Recently, some theories have been proposed to explain the leakage mechanism under the accumulation condition of the MIS capacitance–voltage (*C*–*V*) curve to study the properties of gate dielectrics, but systematic studies of the leakage mechanism under the inversion condition are quite few.<sup>8</sup> Compared with the conventional thick SiO<sub>2</sub> gate dielectric, the leakage current density of the high-*k* gate dielectric is still larger than that of the thick SiO<sub>2</sub> gate dielectric. Therefore, the leakage mechanism of high-*k* gate dielectrics is very different from that of the thick SiO<sub>2</sub> gate dielectric. In this paper, we report studies of the leakage mechanism under the accumulation condition as well as under the inversion condition. It has been reported that the increase of capacitance depends on the ability of the electron concentration to follow the applied ac signal.<sup>8</sup> Due to the highly leaky dielectrics, the substrates do not have enough electrons to maintain the leakage current. Therefore, the depletion width broadens to generate more electrons, which is called deep depletion. In this situation, the capacitance will be further decreased while the gate bias voltage increases. In the present study, the generation lifetime of silicon substrates is extracted to examine the quality of the silicon substrate from the investigation of the correlation between the leakage mechanism and deep depletion.

### II. EXPERIMENTAL PROCEDURES

The 4-in. boron-doped *p*-type silicon (100) wafers (resistivity 1–10 Ω cm) with thickness ranging from 500 to 550 μm from Shinkosha Co., Ltd., were cleaned by the standard Radio Corporation of America (RCA) cleaning process and chemically etched in dilute HF solution to remove the native oxide from the silicon substrate. After RCA cleaning, STO

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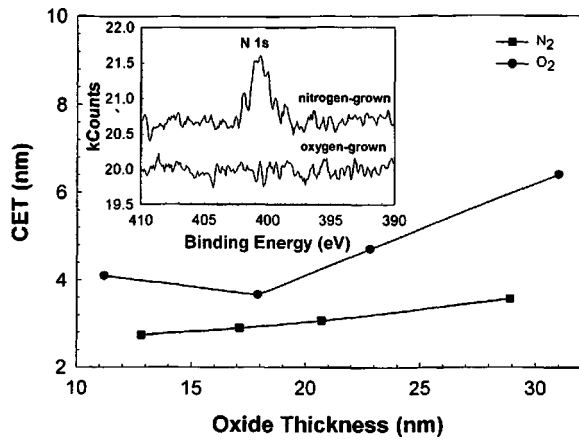


FIG. 1. Variation of the CET with oxide thickness for nitrogen-grown and oxygen-grown STO film. The inset is the XPS characteristics of nitrogen in nitrogen-grown and oxygen-grown films.

thin films were deposited by the rf-magnetron sputtering technique with a 3-in.-diam SrTiO<sub>3</sub> target. The substrate temperature was kept at 500 °C. The background pressure of the vacuum chamber was  $1 \times 10^{-5}$  Torr. All films were prepared at a fixed power of 150 W and constant pressure of 40 mTorr which was maintained by a mixture of Ar and O<sub>2</sub> or Ar and N<sub>2</sub> at a mixing ratio of 4:1 with a total flow of 10 sccm. The thickness of deposited STO thin films varied from 11 to 30 nm which was determined by ellipsometry. The composition of STO films were characterized by using x-ray photoelectron spectroscopy (XPS). For the electrical measurement, an Al top electrode with an area of  $7.0 \times 10^{-4}$  cm<sup>2</sup> was formed by thermal evaporation, and then patterned by a wet lithography process. Then Al was also used as backside electrode for obtaining ohmic contact. The C–V measurements were performed using a HP 4284A LCR meter at 100 kHz and the current–voltage (I–V) characteristics were recorded using a HP 4156A semiconductor parameter analyzer.

### III. RESULTS AND DISCUSSION

#### A. Leakage mechanism

Figure 1 shows the variation of capacitance equivalent thickness (CET) of the nitrogen-grown and oxygen-grown SrTiO<sub>3</sub> thin films with oxide thickness. Generally speaking, the CET of the films increases with increasing interfacial layer thickness and decreases with increasing crystallinity of the thin films.<sup>9</sup> Under the consideration of these two points, the oxygen-grown films with a thickness of 18 nm have the minimal CET (Fig. 1). The presence of nitrogen in STO films was verified using XPS. It can be observed from the inset of Fig. 1 that the characteristic peak of N 1s appears in the nitrogen-grown films, indicating that such STO thin film contains some nitrogen. The nitrogen in the thin films would suppress the growth of interfacial layer when deposited at high temperature.<sup>10</sup> Therefore, the interfacial layer thickness of the nitrogen-grown film is expected to be thinner than that of the oxygen-grown film, which leads to a smaller CET of nitrogen-grown thin films as shown in Fig. 1. The difference in the leakage current characteristics of the oxygen-grown

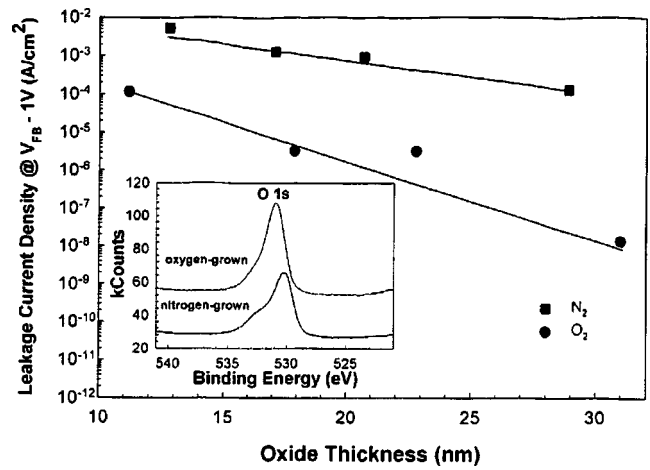


FIG. 2. Variation of leakage current density with oxide thickness for nitrogen-grown and oxygen-grown STO films. The inset is the XPS characteristics of oxygen in nitrogen-grown and oxygen-grown STO films.

and nitrogen-grown thin films is depicted in Fig. 2, indicating that the leakage current densities increase with decreasing oxide thickness and the leakage current densities of the nitrogen-grown films is 2–3 orders of magnitude higher than those of the oxygen-grown films. As indicated in the inset of Fig. 2, the oxygen concentration of nitrogen-grown film is less than that of oxygen-grown film, which implies that the nitrogen-grown thin film might have more oxygen vacancies than oxygen-grown thin film. It is indicated in Fig. 3 that the leakage current density under negative bias voltage decreases with increasing oxide thickness, while the leakage current density under positive bias voltage increases with decreasing oxide thickness at low electric field but it increases with increasing oxide thickness at high electric field. The leakage current density increases exponentially with increasing negative bias voltage. As for under positive bias voltage it increases exponentially at low electric field and then saturates at high electric field. The saturation voltage increases with increasing oxide thickness. This phenomenon will be explained in detail later. Figure 4 shows the comparison between theoretical model and experimental data under the accumulation condition of the 17.1-nm-thick nitrogen-grown

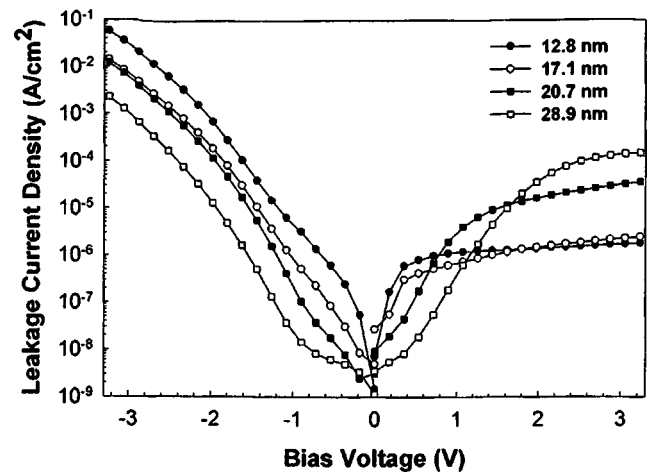


FIG. 3. Plots of leakage current density versus bias voltage for various thickness STO MIS capacitors.

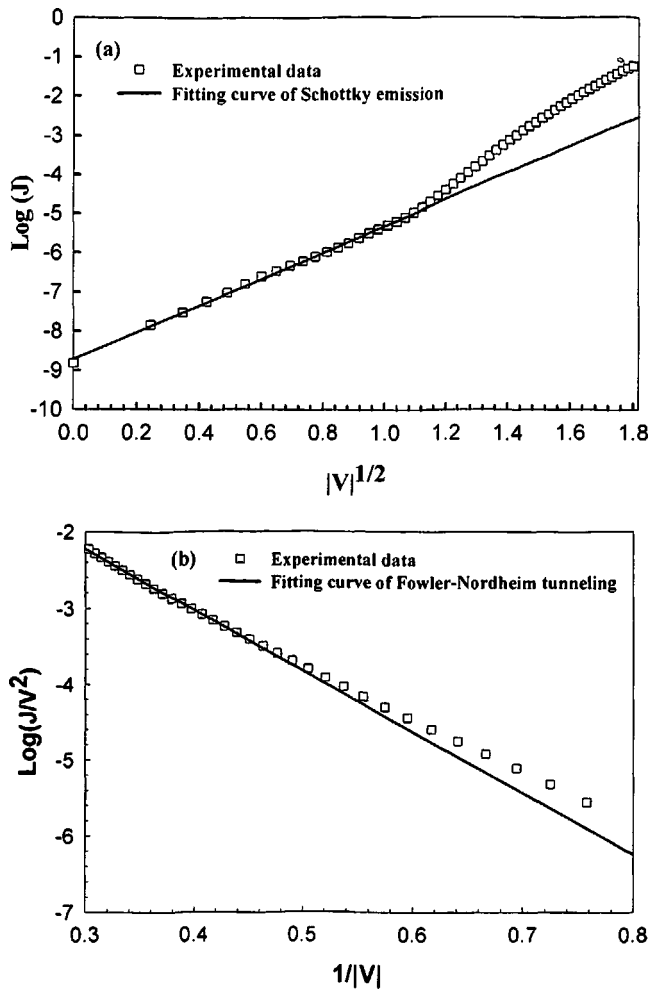


FIG. 4. (a) Comparison between Schottky emission model and experimental data at low electric field under negative bias voltage. (b) Comparison between Fowler-Nordheim tunneling model and experimental data at high electric field under negative bias voltage.

film. The leakage current density  $J_{SE}$  is governed by Schottky emission, which can be expressed as<sup>8</sup>

$$J_{SE} = A^* T^2 \exp\left\{-q\left[\varphi_B - (qE/4\pi\epsilon_d)^{1/2}\right]/kT\right\}, \quad (1)$$

where  $A^*$  is a constant,  $\varphi_B$  the potential barrier height on the surface,  $\epsilon_d$  the permittivity of the films,  $q$  the unit charge,  $k$  the Boltzmann constant,  $T$  the temperature, and  $E$  the electric field ( $E = V/d$ , where  $V$  is the voltage across the film and  $d$  is the thickness of the film). As shown in Fig. 4(a),  $\text{log}(J)$  versus  $V^{1/2}$  is plotted. When the magnitude of the gate bias  $< 1$  V ( $|V|^{1/2} < 1$ ) in negative bias voltage, the solid line illustrated in Fig. 4(a) corresponding to the Schottky emission mode provides a good fit to the experimental data. Therefore, Schottky emission is responsible for the leakage current at low electric field under negative bias voltage. When the current transport is Fowler-Nordheim tunneling, the leakage current density  $J_{FN}$  has the form<sup>8</sup>

$$J_{FN} = BE^2 \exp(-E_0/E), \quad (2)$$

where  $E$  is the electric field, and  $B$  and  $E_0$  are constants in terms of effective mass and barrier height. When the magnitude of the gate voltage  $> 2.5$  V ( $1/|V| < 0.4$ ) under negative bias, the solid line in the  $\text{log}(J/V^2)$  versus  $1/V$  plot [Fig. 4(b)]

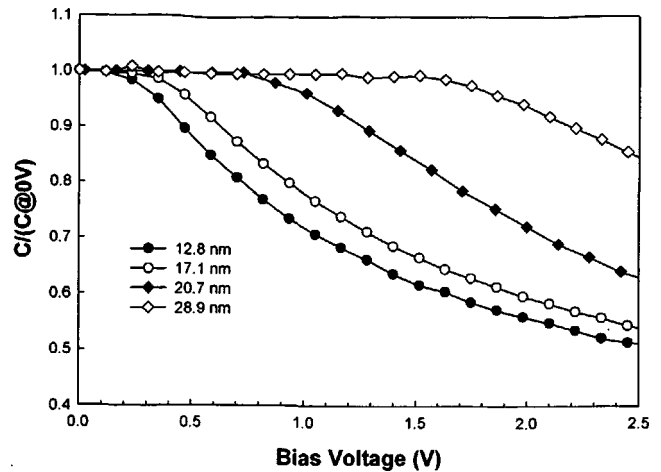


FIG. 5. Normalized capacitance measured at 100 kHz for various dielectric film thicknesses of the MIS capacitors.

of representing Fowler-Nordheim tunneling provides a good fit to the data. This is evident that Fowler-Nordheim tunneling is responsible for the leakage current at high electric field under negative bias voltage.

## B. Deep depletion

Some studies<sup>11,12</sup> have reported that when gate bias is swept into the inversion condition too fast for minority electron carriers to follow, the charge neutrality must be satisfied by the ionized donors alone. Therefore, the depletion width becomes broader than that in thermal equilibrium and the capacitance decreases below its thermal equilibrium saturation value. Such a nonequilibrium condition is called deep depletion. The system at room temperature usually is not in equilibrium when the gate bias is swept in the direction of increasing inversion condition, but it is in equilibrium when gate bias is swept in the direction of decreasing inversion condition. We also observed the deep depletion in the  $C-V$  measurements. However, the  $C-V$  curves of gate bias swept in the direction of increasing and decreasing inversions are the same. Therefore, the deep depletion phenomenon in our  $C-V$  measurements was not caused by being swept too fast. The main reason may be due to the lack of carriers which caused the leakage current saturation in the positive bias voltage. Figure 5 shows the normalized capacitance of the nitrogen-grown films under the inversion condition. It can be observed that the initiation voltage of the deep depletion increases with increasing oxide thickness. The increasing trend of the initiation voltage of deep depletion for thicker films was similar to that of the saturation voltage of the leakage current density under positive bias voltage. Some formulas have been derived to further clarify the deep depletion phenomenon. For MIS structure, the depletion width  $W$  is given by<sup>8</sup>

$$W = \sqrt{\frac{2\epsilon_{si}\psi_s(\text{inv})}{qN_A}}, \quad (3)$$

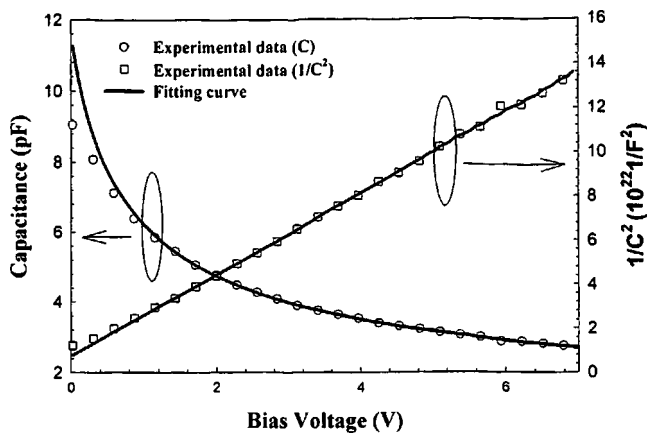


FIG. 6. Plots of capacitance under the inversion condition vs bias voltage and the corresponding fitting curves for the STO-based MIS capacitor.

where  $\epsilon_{si}$  is the permittivity of silicon,  $\psi_s(\text{inv})$  the surface potential under inversion condition, and  $N_A$  the substrate dopant concentration. The formula of depletion capacitance  $C_D$  is given by

$$C_D = \frac{A \epsilon_{Si}}{W}, \quad (4)$$

where  $A$  is the capacitor area. Because the capacitance of the gate dielectric is much larger than the depletion capacitance under the inversion condition, the surface potential is almost equal to the gate bias voltage ( $V_G$ ). Therefore, we can obtain

$$\psi_s \cong V_G \propto \frac{1}{C^2}. \quad (5)$$

Figure 6 shows the capacitance and  $1/C^2$  as a function bias voltage and their corresponding fitting curves. We assume that the dopant is uniformly distributed in the silicon substrate. It can be observed in Fig. 6 that  $V_G$  is directly proportional to  $1/C^2$  for  $V_G > 1.5$  V. Therefore, we can associate the deep depletion phenomenon with the broadening of the depletion width. In general, the dopant concentration of silicon substrates is determined by calculating the minimal high-frequency capacitance. However, it is difficult to determine the minimal high-frequency capacitance while deep depletion occurs. The dopant concentration of the silicon substrate for nitrogen-grown films is illustrated in Fig. 7, which can be calculated from the slope of the  $1/C^2-V$  curve. The calculated dopant concentrations ranging from  $10^{15}$  to  $10^{16} \text{ cm}^{-3}$  are consistent with those of the starting substrate we used ( $1-10 \Omega \text{ cm}$ ). Therefore, this study provides an alternative method to successfully determine the dopant concentration in the underlying Si substrate.

### C. Correlation between the leakage mechanism and deep depletion

In this experiment, electrons are injected from the  $p$ -type silicon substrate when the gate bias is at positive voltage. Therefore, the leakage current density could be limited by the supply of electrons from the substrates, tunneling or Schottky emission to the corresponding band in the dielec-

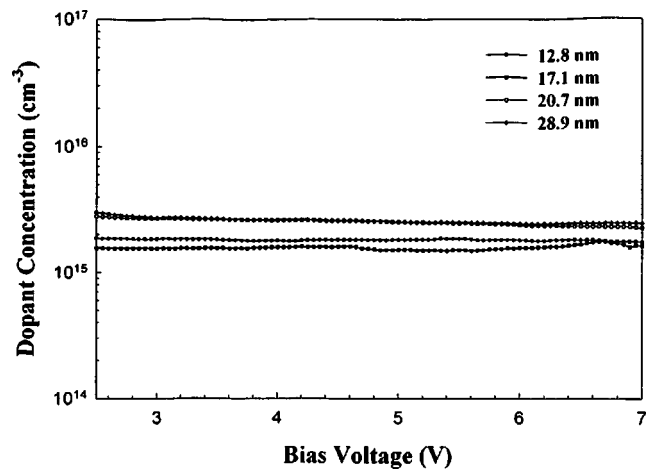


FIG. 7. Variation of substrate dopant concentration extracted for various STO film thicknesses with bias voltage.

tric, or electron drift in the dielectric.<sup>13</sup> For the STO gate capacitor at room temperature, the drift of electrons is not a limiting factor. As in the previous discussion the leakage mechanism under negative bias voltage is dominated by the Schottky emission and Fowler–Nordheim tunneling which is limited by the tunneling to the corresponding band in the dielectric. The behaviors of leakage current density under positive bias voltage and negative bias voltage are quite different. Consequently, the limiting factors of leakage current density under positive bias voltage and negative bias voltage should be different. When the gate bias is at negative voltage, the metal gate is the cathode which provides electrons to maintain the leakage current. Therefore, the supply of electrons is also not a limitation and the  $I-V$  relation obeys the Schottky emission and Fowler–Nordheim tunneling as shown in Fig. 4. However, when the gate bias is at positive voltage, the supply of electrons depends on the inversion condition of the semiconductor. Because of the high leaky insulator, the number of electrons on the silicon surface is not enough to support the high leakage current density under positive bias voltage. Therefore, the supply of electrons could be a limiting factor and could control the  $I-V$  characteristic. The leakage current density under positive bias voltage was saturated in high electric field and the depletion width increased to generate more electrons. The saturation of current density under positive bias voltage is accompanied by the appearance of deep depletion phenomenon in the  $C-V$  measurements. It can be inferred from the previous discussion that there should be some correlation between the saturation in the leakage current and the deep depletion phenomenon. As indicated in Fig. 3, the saturation voltage of the leakage current density under positive bias voltage increases with increasing oxide thickness. The thicker STO thin films would be less leaky under the same voltage bias, leading to the larger saturation voltage which occurred. For the same reason, the initiation voltage of deep depletion should increase with increasing oxide thickness.

The leakage current density due to the generation current density is thus given by<sup>13</sup>

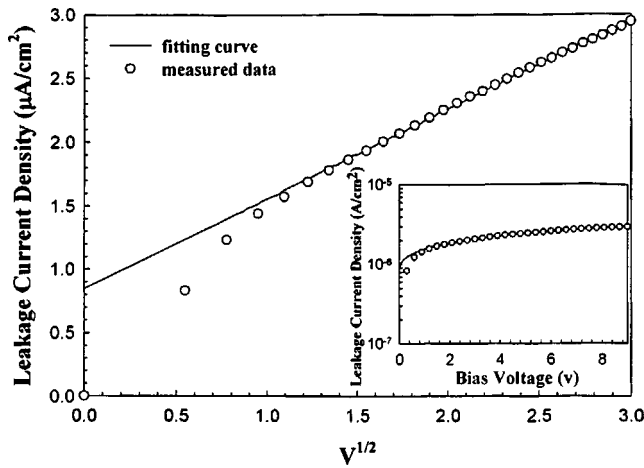


FIG. 8. Comparison between experimental data and generation current mechanism. The inset is the relation of leakage current density vs bias voltage.

$$J = \int_{w_m}^w \frac{qn_i}{\tau} dx + qn_i s + \frac{qn_i^2 D_n}{N_A L_n}, \quad (6)$$

where  $J$  is the leakage current density,  $w$  the depletion width when the potential drop across the semiconductor is  $\psi_s$ ,  $w_m$  the depletion width at strong inversion,  $n_i$  the intrinsic concentration,  $\tau$  the generation lifetime,  $s$  the surface recombination velocity which depends on the interface state density, and  $D_n$  and  $L_n$  the diffusion coefficient and diffusion length of minority carriers, respectively. The generation current is dominated by three different mechanisms described as follows. The first term in the above equation is associated with the bulk traps; the second term corresponds to interface states; the last one is contributed by minority carriers diffused from backcontact, which dominate at high temperature and can be neglected at room temperature. The amount of interface states should be invariant under deep depletion and therefore contributes a constant component to the gate leakage current. However, the amount of bulk traps increases very slowly with depletion width under deep depletion and results in a very slowly increasing current component. The greater generation current in the new deep depletion layer leads to the increased leakage current.

The plot of  $J$  vs  $V^{1/2}$  is illustrated in Fig. 8. When the gate bias is larger than 1.5 V, the equation of generation current as represented by the straight solid line provides a good fit to the experimental data, indicating that the generation current due to the bulk trap is responsible for the leakage current at high electric field of positive bias voltage. According to our previous discussion, deep depletion arises due to the broadening of the depletion width and the saturation of the leakage current density in the positive bias voltage as a result of a lack of electrons in the silicon substrate. Figures 6 and 8 indicate that the initiation voltage of both deep depletion and generation current which occur are almost equivalent, which is about 1.5 V. Obviously, the experimental results are consistent with previous explanations for deep depletion and the saturated leakage current density. It is noted that beyond the saturation voltage, the leakage current density increases very slowly and more electrons are gener-

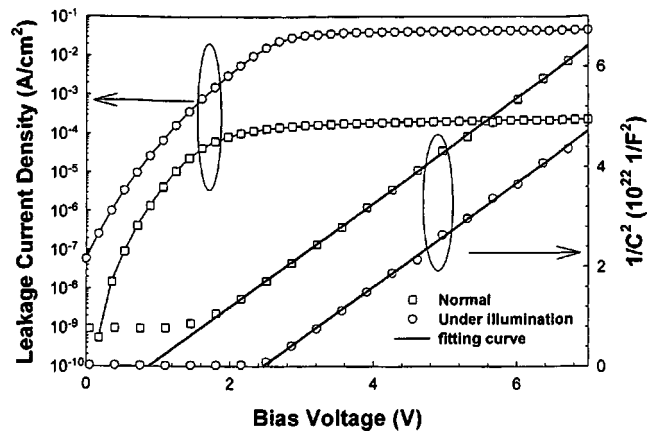


FIG. 9. Effect of electrical measurement under illumination on the nitrogen-grown 28.9-nm-thick STO film.

ated in the new deep depletion layer to cause the leakage current increase. The influence of electrical measurements under illumination on the nitrogen-grown STO film with 28.9 nm thickness is also investigated. As can be seen in Fig. 9, the magnitude of the leakage current density measured under illumination increases more than 2 orders of magnitude due to the electron-hole pairs being generated by being illuminated with light. The saturation voltage of the leakage current density increases due to the illumination. Therefore, the initiation voltage of deep depletion should also increase which is consistent with the prediction. The difference between two slopes of the  $1/C^2 - V$  curves in Fig. 9 is smaller than 1%, indicating that the dopant concentrations of the silicon substrate calculated by those two conditions are almost the same. Therefore, no matter under what conditions deep depletion is still induced by the lack of electrons to maintain the high leakage current density. The generation lifetime of silicon substrates can be extracted from Eq. (6) with known dopant concentrations of the silicon substrate. Figure 10 shows the variation of the generation lifetime with oxide thickness. The generation lifetime decreased with increasing oxide film thickness. That may be due to the more bulk traps with thicker films. When the thicker STO thin film

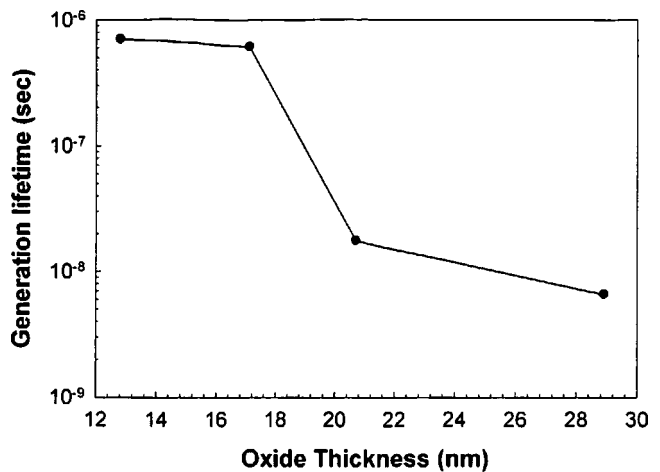


FIG. 10. Plot of generation lifetime vs oxide thickness for the nitrogen-grown STO MIS capacitor.

grows on the silicon substrate, it has more time to diffuse more ions into the substrate or to damage the substrate to have more bulk traps. Therefore, the samples with thicker films have a smaller generation lifetime. The generation lifetime in bulk silicon is 2.5 m sec (Ref. 8). Because STO thin films are deposited on the silicon substrate, the trap density in the silicon substrate will be larger than that of bulk silicon substrate. Consequently, the generation lifetime should be smaller than 2.5 m sec. Therefore, the extracted generation lifetime is a reasonable value. The generation lifetime can be given by<sup>8</sup>

$$\tau = \frac{1}{\sigma v_{th} N_t}, \quad (7)$$

where  $\sigma$  is the capture cross section,  $v_{th}$  the carrier thermal velocity, and  $N_t$  the trap density. Therefore, the extracted generation lifetime also provides a method to examine the quality of silicon substrates with different processing conditions. When the processing conditions are similar, this method can examine the degree of diffusion from the deposited films into the substrates.

#### IV. CONCLUSIONS

We deposited STO thin films on silicon substrates in an Ar–O<sub>2</sub> and Ar–N<sub>2</sub> mixed ambient. The CETs of the nitrogen-grown films are less than those of oxygen-grown films due to smaller interfacial layer thicknesses. The leakage current densities of nitrogen-grown films are larger than those of oxygen-grown films as a result of more oxygen vacancies in nitrogen-grown films. Schottky emission and Fowler–Nordheim tunneling were responsible for the leakage mechanics of nitrogen-grown films at low and high electric fields under negative gate bias, respectively. Because of the high leaky insulator, the number of electrons in the silicon substrates is not enough to maintain the leakage current density of STO-based MIS capacitor under positive bias voltage, which leads to the leakage current density saturating and

increasing slowly in the positive bias voltage. Therefore, in order to generate more electrons, the depletion width gets broadened, which is called deep depletion. The dopant concentration of silicon substrates can also be determined by deep depletion. The influence of electrical measurements under illumination on the nitrogen-grown STO film was also investigated. We also demonstrated that the generation current dominated the leakage current density at the high electric field under positive bias voltage. The correlation between deep depletion and leakage current mechanics under positive bias voltage was established. The generation lifetime of silicon substrates can be extracted with this correlation to examine the quality of silicon substrates.

#### ACKNOWLEDGMENT

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- <sup>1</sup>International Technology Roadmap for Semiconductors (Semiconductor Industry Association, Austin, Texas, 2001).
- <sup>2</sup>D. A. Chang, P. Lin, and T. Y. Tseng, J. Appl. Phys. **78**, 7103 (1995).
- <sup>3</sup>A. Chin, C. C. Liao, C. H. Lu, W. J. Chen, and C. Tsai, Symp. VLSI Tech. Dig., 1999, p. 135.
- <sup>4</sup>B. H. Lee, L. Kang, W. J. Qi, R. Nieh, Y. Jeon, K. Onishi, and J. C. Lee, Tech. Dig. - Int. Electron Devices Meet. **1999**, 133 (1999).
- <sup>5</sup>J. C. Wang, S. H. Chiao, C. L. Lee, T. F. Lei, Y. M. Lin, M. F. Wang, S. C. Chen, C. Y. Lu, and M. S. Liang, J. Appl. Phys. **92**, 3936 (2002).
- <sup>6</sup>K. Eisenbeiser, J. M. Finder, Z. Yu, J. Ramdani, J. A. Curless, J. A. Hallmark, R. Droopad, W. J. Ooms, L. Salem, S. Bradshaw, and C. D. Overgaard, Appl. Phys. Lett. **76**, 1324 (2000).
- <sup>7</sup>H. T. Lue, C. J. Wu, and T. Y. Tseng, IEEE Trans. Ultrason. Ferroelectr. Freq. Control **50**, 5 (2003).
- <sup>8</sup>S. M. Sze, *Physics of Semiconductor Device*, 2nd ed. (Wiley, New York, 1981).
- <sup>9</sup>G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **89**, 5243 (2001).
- <sup>10</sup>C. Y. Liu, H. T. Lue, and T. Y. Tseng, Appl. Phys. Lett. **81**, 4416 (2002).
- <sup>11</sup>E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley, New York, 2003).
- <sup>12</sup>R. F. Pierret, IEEE Trans. Electron Devices **7**, 869 (1972).
- <sup>13</sup>R. M. Patrikar, R. Lal, and J. Vasi, J. Appl. Phys. **73**, 3857 (1993).