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Effects of grain boundaries on performance and hot-carrier reliability of excimer-laser annealed polycrystalline silicon thin film transistors

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This work examines the effects of grain boundaries on the performance and hot-carrier reliability of excimer-laser-annealed polycrystalline silicon thin film transistors (poly-Si TFTs) before and after NH_3 plasma treatment. Self-aligned poly-Si TFTs, whose channel regions include a 150 nm thick laser-crystallized poly-Si layer with small grains and a 100 nm thick layer with large grains, are fabricated. Other TFTs, with large grains throughout their channels, are fabricated nearby for comparison. The trapping of electrons at grain boundaries in the drain junction creates strong local electric fields that boost the leakage current, cause the threshold voltage to decline as the drain bias increases, enhance the kink effect in the output characteristics, and degrade the hot-carrier reliability of devices. When static hot-carrier stress is applied to nonhydrogenated poly-Si TFTs for less than 10^4 s at $V_{GS}=10$ V and $V_{DS}=20$ V, hot holes are injected into the gate oxide at the same time trap states are created in the drain junction. The screening effect is observed when the same stress is applied to devices that have many grain boundaries in their drain junctions. NH_3 plasma treatment prevents the trapping of electrons at grain boundaries. The performance of hydrogenated poly-Si TFTs improves, but the hot-carrier reliability of those TFTs with large grains in their drain junctions degrades. The hydrogenation causes a trade-off between the electrical characteristics and the hot-carrier reliability, and introduces irregular humps in the subthreshold region. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1699504]

I. INTRODUCTION

Excimer-laser-annealed polycrystalline silicon thin film transistors (poly-Si TFTs) have been extensively investigated due to their potential for integration into peripheral driver circuits with active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting displays (AMOLEDs) on large area glass substrates.[1] A laser-crystallized poly-Si TFT with a high driving current, good reliability and uniform device performance is necessary to develop a system on a panel (SOP). Many techniques have been proposed to improve the electrical characteristics of poly-Si TFTs, such as enlarging the channel grains by laser-induced lateral crystallization[2] and reducing the number of grain-boundary trap states by plasma treatment.[3] However, the inability to control grain boundaries and their location in the channel region reduces the uniformity of devices. In particular, the instability of an applied laser can simultaneously introduce grains of various sizes into the channel regions,[4] because the formation of channel regions follows the definition of active islands. Meanwhile, the charge trapped at the grain boundaries, which is always associated with surface roughness, enhances local electric fields.[5] A self-aligned poly-Si TFT may exhibit different behavior in its forward and reverse modes because of asymmetry of the grain boundaries, particularly in the drain junction.[6] Although many studies of the influence of grain-boundary locations and trap states on device performance have involved simulation,[7] we found none that has yet applied experimental methods to laser-crystallized poly-Si TFTs.[8]

In this work, self-aligned poly-Si TFTs are fabricated with various numbers of grain boundaries in their drain junctions. Other TFTs with fewer grain boundaries throughout their channel regions are fabricated nearby as a reference. Various numbers of grain boundaries in the drain junctions and throughout the channel regions are used to determine the effects of grain boundaries on the performance and hot-carrier reliability of excimer-laser-crystallized poly-Si TFTs with and without NH_3 plasma treatment. Interdevice variations, such as the difference between the numbers of grain boundaries in the channels[9] and the channel shortening effect by diffusion of dopants from the source and drain,[10] can be eliminated by comparing the forward and reverse modes of a single device. The strong local electric fields created by the trapping of electrons at the grain boundaries critically affect the performance and hot-carrier reliability of excimer-laser-crystallized poly-Si TFTs.[11] Local electric fields can be then reduced by passivating grain boundaries using NH_3 plasma treatment.[12]

II. EXPERIMENT

Figure 1 shows key process flows for fabricating self-aligned poly-Si TFTs. Silicon wafers with 2 μm thermal oxide layers were used as the starting substrates. A 50 nm thick amorphous silicon (α-Si) layer was deposited by decomposing SiH_4 in a low pressure chemical vapor deposition

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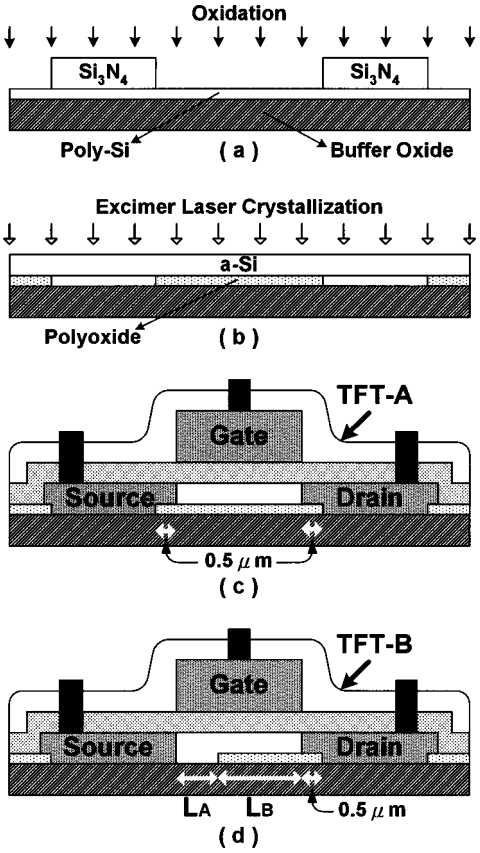

FIG. 1. Key process flows for fabricating self-aligned poly-Si TFTs.

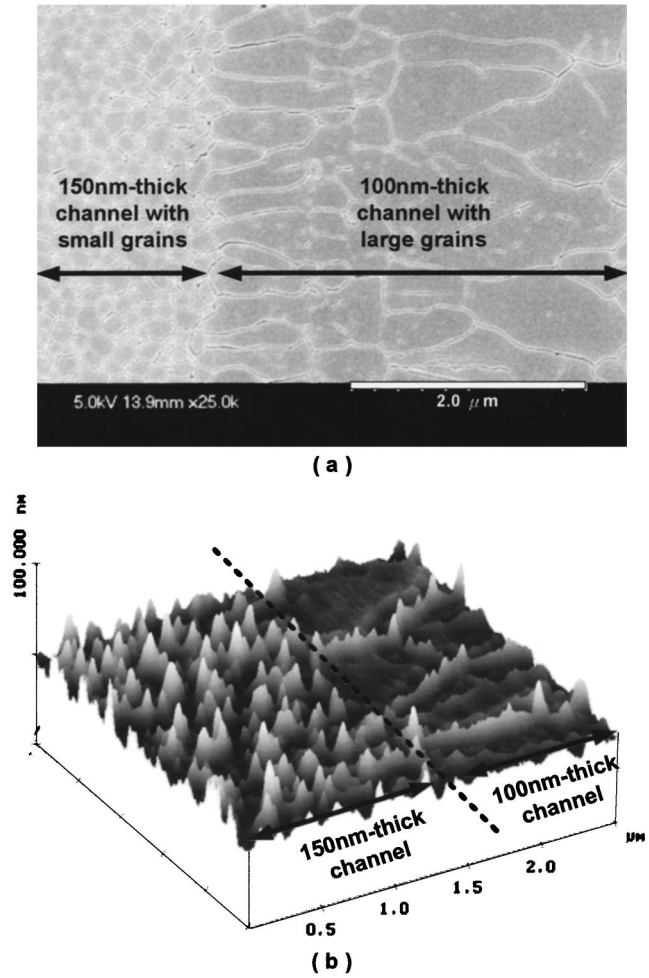

FIG. 2. (a) SEM photograph of the excimer laser-crystallized poly-Si film after Secco etching and (b) AFM image of the surface roughness of the excimer laser-crystallized poly-Si film near where the 150 and 100 nm thick regions are connected.

(LPCVD) system at 550 °C. Next, a 150 nm thick silicon nitride (Si_3N_4) layer was deposited and then patterned. The exposed silicon films were fully oxidized at 925 °C using the Si_3N_4 patterns as hard masks, as indicated in Fig. 1(a). Subsequently, the Si_3N_4 patterns were selectively etched in a hot phosphoric acid bath at 165 °C. After the native oxide was removed from the region of silicon films, a 100 nm α-Si layer was deposited by decomposing SiH_4 in a LPCVD system at 550 °C. The α-Si films were then crystallized under irradiation by a KrF excimer laser, as shown in Fig. 1(b). After the active channel regions were defined, a 135 nm thick tetraethylorthosilicate (TEOS) gate oxide was deposited by plasma-enhanced CVD (PECVD) at 350 °C. Thereafter, a 250 nm an α-Si layer was deposited and then patterned as the gate electrodes. The source and drain regions were formed after self-aligned ion implantation of phosphorus with dose of $5\times10^{15}\,\mathrm{cm}^{-2}$ at 50 keV. A 300 nm TEOS oxide layer was deposited, and then the dopants were activated at 600 °C for 12 h. Finally, contact opening and metallization were performed to complete the self-aligned structure. The TFT shown in Fig. 1(c) is called TFT-A; it has large grains throughout its channel region. The other TFT, shown in Fig. 1(d), is called TFT-B, and it has large and small grains on both sides of its channel region.

The electrical characteristics of these devices were evaluated before and after NH_3 plasma hydrogenation in a parallel plate reactor at 300 °C at power density of 0.7 $\mathrm{W/cm}^2$. A Secco etchant, which consists of 7.30 g of $K_2Cr_2O_7$ dissolved in 165 ml of H_2O and 335 ml of HF, was used to delineate grain-boundary defects. The side of the 100 nm thick channel of TFT-B is defined as a drain of forward mode, and the other side of the 150 nm thick channel of TFT-B is defined as a drain of reverse mode. The channel length L of TFT-B includes channel length L_A of the 150 nm thick region and channel length L_B of the 100 nm thick region. In evaluation of the transfer characteristics of the devices, the threshold voltage V_{th} is defined as the gate voltage V_{GS} at constant drain current; for example, $I_{\mathrm{DS}}=(W/L)\times10\,\mathrm{nA}$ at drain voltage of $V_{\mathrm{DS}}<5\,\mathrm{V}$ and $I_{\mathrm{DS}}=(W/L)\times100\,\mathrm{nA}$ at drain voltage of $V_{\mathrm{DS}}\geqslant5\,\mathrm{V}$. The field-effect mobility and the transconductance are evaluated at $V_{\mathrm{DS}}=0.1\,\mathrm{V}$. All hot-carrier stress on the devices with and without NH_3 plasma treatment is applied at drain voltage of $V_{\mathrm{DS}}=20\,\mathrm{V}$ and gate voltage of $V_{\mathrm{GS}}=10\,\mathrm{V}$. The dimensions of the stressed devices are $L=6\,\mu\mathrm{m}$ and $W=10\,\mu\mathrm{m}$. The channel length of TFT-B is the sum of $L_A=2\,\mu\mathrm{m}$ and $L_B=4\,\mu\mathrm{m}$. ΔV_{th} is defined as $V_{\mathrm{th},s}-V_{\mathrm{th},i}$ where $V_{\mathrm{th},i}$ represents the initial V_{th} and $V_{\mathrm{th},s}$ represents V_{th} at each stress time. The degradation of $G_{m\,\max}$ is defined as $\Delta G_{m\,\max}/G_{m\,\max,i}$, where $\Delta G_{m\,\max}=G_{m\,\max,s}-G_{m\,\max,i}$; $G_{m\,\max,i}$ denotes the initial $G_{m\,\max}$, and $G_{m\,\max,s}$ represents $G_{m\,\max}$ at each stress time.

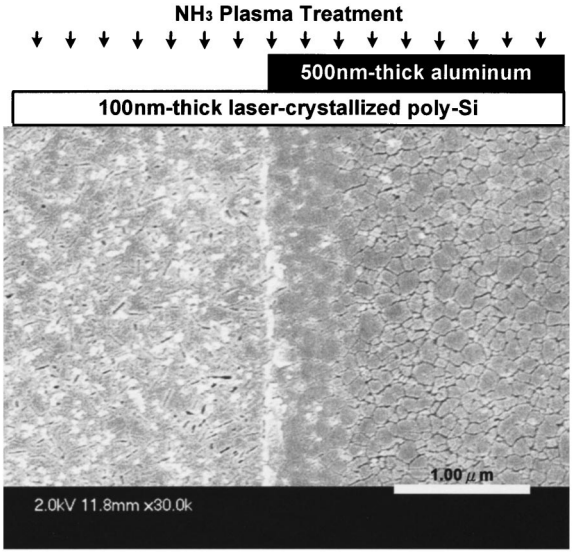

FIG. 3. SEM photograph of an excimer laser-crystallized poly-Si film with and without NH_3 plasma treatment after Secco etching. A 100 nm thick laser-crystallized poly-Si film was selectively treated with NH_3 plasma using aluminum patterns as hard masks, shown schematically at the top.

III. RESULTS AND DISCUSSION

A. Features of the excimer-laser-crystallized poly-Si films

Figure 2(a) shows a scanning electron microscopy (SEM) photograph of grains of different size of the laser-crystallized poly-Si film between the 150 and 100 nm thick regions. Laser energy densities between that which completely melted the 100 nm thick silicon films and that which partially melted the 150 nm thick films were employed to form various size grains of laser-crystallized poly-Si films. Large grains in the 100 nm thick regions formed in the superlateral growth (SLG) regime.[13] Meanwhile, a lateral thermal gradient from the modulated thickness of silicon films facilitates the formation of longitudinal grains.[14] Small grains of the 150 nm thick regions are grown from unmelted residuals that act as nucleation sites. In the fabrication of TFT-B devices, large and small grains form simultaneously in the channel regions, leading to different numbers of grain boundaries in the drain junctions when measurements of TFT-B were made in forward and reverse modes. However, grain boundaries of excimer-laser-crystallized poly-Si films always have protrusions, and they roughen the surface of the poly-Si films.[15] Figure 2(b) shows an atomic force microscopy (AFM) image of the surface of excimer-laser-crystallized poly-Si films near where the 150 and the 100 nm thick regions are connected. The 150 nm thick channel with surface roughness of 5.36 nm root mean square (rms) and the 100 nm thick channel with surface roughness of 2.88 nm rms are evaluated from Fig. 2(b). Significant mass transport toward the grain boundaries roughens the surface and then causes carriers trapped at the grain boundaries to enhance local electric fields.

Additionally, Secco etching was also used to delineate grain boundaries with and without passivation. As shown in Fig. 3, a 100 nm thick laser-crystallized poly-Si film was selectively treated with NH_3 plasma using aluminum patterns as hard masks, the insertion of which is schematically depicted above Fig. 3. The aluminum patterns were then selectively removed using wet etchant. The grain boundaries in the aluminum cap region were clearly seen after Secco etching. However, the grain boundaries near the aluminum-capped edge were ambiguous because they were passivated by hydrogen lateral diffusion,[16] thereby reducing the etching rate around the grain boundaries. This result implies that lateral diffusion of hydrogen may lead to a lack of uniformity in the passivation of grain boundaries throughout the channel region. Therefore, irregular $I-V$ characteristics, such as hump effects, are evident in the subthreshold region.

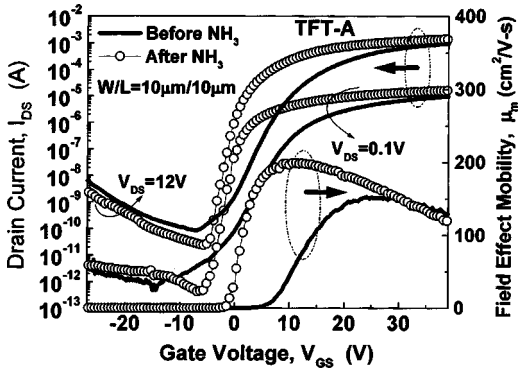

FIG. 4. Transfer characteristics of TFT-A measured before and after NH_3 plasma treatment for 2 h.

B. *I–V* characteristics

Figures 4 and 5 show the transfer characteristics of a single TFT-A and the forward and reverse modes of a single TFT-B before and after NH_3 plasma treatment. A comparison between TFT-A and TFT-B reveals that the decrease in the number of grain boundaries of the channel regions is accompanied by a reduction in the threshold voltage and an increase in the field-effect mobility. This is because the grain boundaries trap electrons when gate voltage V_{GS} is applied, and generate surrounding depletion regions and lead to the formation of potential barriers. Meanwhile, strained bonds and dangling bonds at the grain boundaries generate band tail

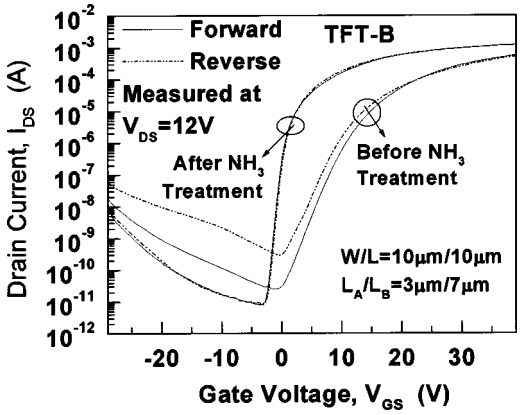

FIG. 5. Transfer characteristics of a single TFT-B measured in forward and reverse modes before and after NH_3 plasma treatment for 4 h.

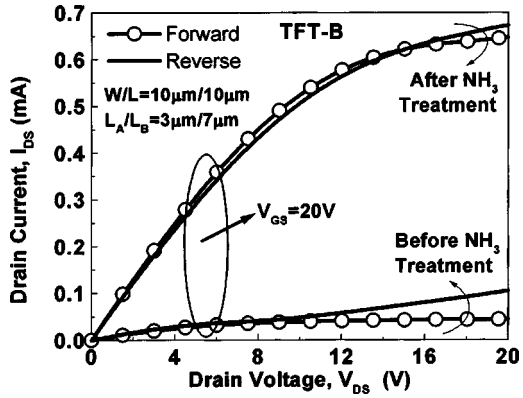

FIG. 6. Output characteristics of a single TFT-B measured in forward and reverse modes before and after NH_3 plasma treatment for 4 h.

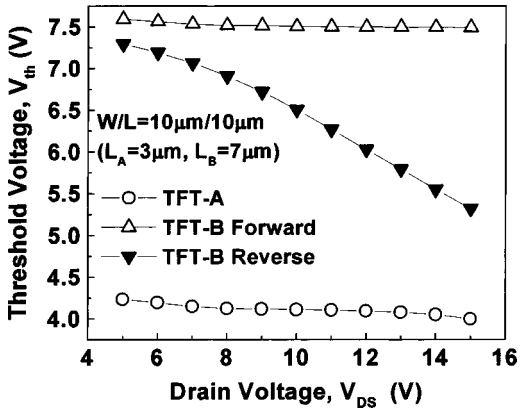

FIG. 7. Variations of threshold voltage V_{th} with drain bias V_{DS} for nonhydrogenated TFT-A and nonhydrogenated TFT-B in both modes.

states and deep level states in the band gap, respectively. These states can trap electrons, and reduce the ON current and increase the OFF current. However, the states can be passivated during NH_3 plasma treatment,[17] and that would yield a steeper subthreshold slope for the hydrogenated TFT than that for the nonhydrogenated TFT. The ON/OFF current ratios and the field-effect mobility improve simultaneously after the grain boundaries are passivated. It should be noted that the leakage current of nonhydrogenated TFT-B at $V_{DS}=12\,V$ in reverse mode is significantly higher than that in forward mode, as shown in Fig. 5. The increase in leakage current results from the marked increase in the number of grain-boundary trap states in the drain junction. Many carriers released by thermionic-field emission from the trap sites cause the leakage current in reverse mode to exceed that in forward mode.[18,19] The leakage current is a function of the trap density in the drain junction, which was formulated by Olasupo and Hatalis[18] and Fossum *et al.*[20] Besides, the ON currents in both modes are almost identical because TFT-B is operated in the linear region. Figure 5 also indicates that measured threshold voltage V_{th} at $V_{DS}=12\,V$ is 7.91 V in forward mode and 6.60 V in reverse mode. The fall in V_{th} in reverse mode results from an avalanche-induced short channel effect.[21] Electrons trapped at the grain boundaries enhance the drain depletion length, essentially shortening the channel length at high drain bias. Furthermore, the transfer characteristics of TFT-B in both modes become symmetric following NH_3 plasma treatment for 4 h because the grain boundaries are effectively passivated, thus reducing the difference between the numbers of trap states in the drain junctions in both modes.

The effects of grain boundaries in the drain junction on the performance of devices can be further elucidated from output characteristics of a single TFT-B in both modes and by comparing variation of V_{th} of devices of TFT-A and TFT-B with the drain voltage. As shown in Fig. 6, the kink effect of nonhydrogenated TFT-B at $V_{GS}=20\,V$ in reverse mode appears to be stronger than that in forward mode. This phenomenon can be attributed to the drain-induced grain-boundary barrier lowering effect,[22,23] and the grain-boundary trap-induced avalanche generation effect.[11] The former effect is caused by drain bias V_{DS} modulating the grain-boundary potential barrier heights in the drain junction and forming asymmetric barriers. Extra carriers, which are injected from the lower side of the barriers into the side of the drain junction, increase the drain current as the drain bias increases. The latter effect results from the high local electric fields created by charge states at grain boundaries of the drain junction. The impact ionization process generates electron-hole pairs, resulting in the absence of saturation in the output characteristics.[24] Rates of carrier ionization, often expressed as an exponential function of the electric field, depend strongly on the electric field of the drain junction.[25] Section III C, in which hot-carrier reliability is discussed, further elucidates this phenomenon. Besides, the drain currents in both modes are close to each other and significantly increase after NH_3 plasma treatment for 4 h. The grain-boundary barrier heights are lowered and more electrons are induced to become conduction carriers. Figure 7 shows a comparison of the variation of V_{th} with the drain bias in TFT-A with that in TFT-B. As V_{DS} is varied from 5 to 15 V, V_{th} of TFT-A and forward mode of the TFT-B remain almost unchanged, but V_{th} in reverse mode of TFT-B decreases as V_{DS} increases. This implies that V_{GS} must be reduced to maintain a constant drain current as V_{DS} increases, because grain boundaries themselves create space charge regions that enhance local electric fields in the drain junction. V_{th} evaluated above $V_{DS}=5\,V$ depends strongly on the location of the grain boundary. However, V_{th} at low drain bias, like $V_{DS}=0.1\,V$, depends strongly on the number of grain boundaries in the channel region, rather than on the grain-boundary locations. Trapping of charge at the grain boundaries also influences the drain depletion length when gate and drain voltages are applied.

C. Characterization of hot-carrier reliability

When excimer laser-crystallized poly-Si TFTs, with and without NH_3 plasma treatment, are under static hot-carrier stress, the behavior of these devices is degraded. The degradation can be characterized by the creation of trap states and the injection of hot carriers into the gate oxide. Figure 8 shows variations of the threshold voltage and the maximum transconductance of nonhydrogenated TFT-A and nonhydrogenated TFT-B associated with static hot-carrier stress for

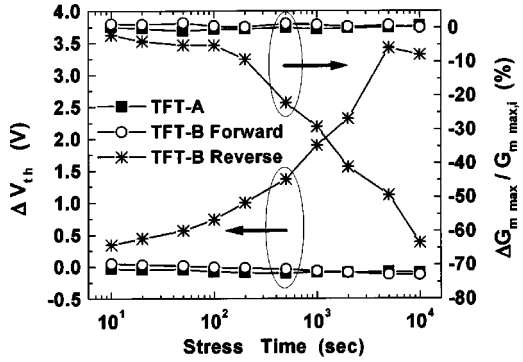

FIG. 8. Degradation of both the threshold voltage and the maximum transconductance of nonhydrogenated devices with the stress time. ΔV_{th} and $\Delta G_{m\ \max}/G_{m\ \max,i}$ were evaluated at $V_{\mathrm{DS}}=0.1$ V for the each stress time. The single TFT-B was first stressed in forward mode and then stressed in reverse mode.

10^4 s. In particular, the single TFT-B was first stressed in forward mode for 10^4 s and then stressed in reverse mode for 10^4 s. TFT-A and TFT-B in forward mode are robust to hot-carrier stress, but the same stress strongly degrades the performance of TFT-B in reverse mode. Hence the hot-carrier reliability of the laser-crystallized poly-Si TFTs depends strongly on the locations of grain boundaries, rather than on the number of grain boundaries in the channel region. Meanwhile, the number of grain boundaries of the drain junction is critical to the hot-carrier reliability of the devices. While TFT-B undergoes reverse stress for 10^4 s, avalanche multiplication occurs through impact ionization in the drain junction, generating many electron-hole pairs from the initially broken weak Si–Si bonds at grain boundaries of the drain junction and the more recently broken strong Si–Si bonds in the drain junction.[26] The hot carriers induced damage at the grain boundaries of the drain junction, equivalent to introducing serial resistance into the current path, thus reducing the ON currents, as evidenced by the serious degradation of TFT-B in reverse mode, as shown in Fig. 8. However, the ON currents of the devices with large grains in the drain junction, following the same stress for 10^4 s, are either slightly increased or almost unchanged with respect to the initial ON currents. Figure 9 shows the transfer characteristics of forward mode of another TFT-B treated with the same

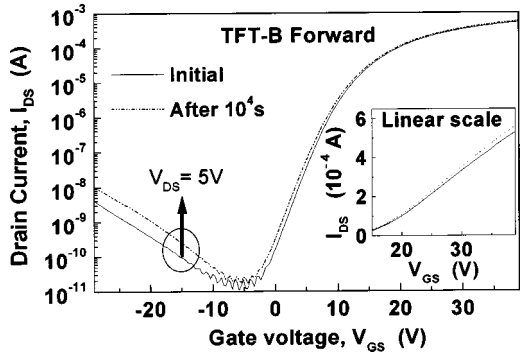

FIG. 9. Transfer characteristics of nonhydrogenated TFT-B measured in forward mode before and after forward stress was applied for 10^4 s. The inset presents a linear scale to show ON currents.

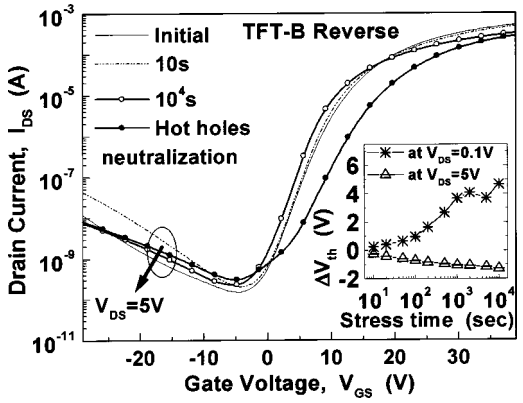

FIG. 10. Transfer characteristics of nonhydrogenated TFT-B measured in reverse mode before and after reverse stress was applied for 10^4 s. The curve associated with the neutralization of hot holes was plotted after the hot holes were released from the gate oxide by final forward stress applied for 10^2 s. The inset plots ΔV_{th} with the stress time at $V_{\mathrm{DS}}=0.1$ and 5 V, respectively.

stress for 10^4 s. Meanwhile, drain avalanche hot holes are injected into the gate oxide by positive voltage $V_{\mathrm{DG}}=10$ V, slightly reducing V_{th} and slightly increasing the ON current, as clearly shown in the inset in Fig. 9. The hot holes screen damage at the grain boundaries of the drain junction, and this was also observed by stressing another TFT-B in reverse mode.

The hot-carrier reliability of devices with grain boundaries in the drain junction is further investigated using another single TFT-B, which was first stressed in reverse mode for 10^4 s and then directly stressed in forward mode for 10^2 s. It should be noted that forward stress for 10^2 s does not significantly damage TFT-B because the drain junction contains large grains in forward mode. The behavior of TFT-B in reverse mode was characterized continuously after the last 10^2 s forward stress. As shown in the inset in Fig. 10, V_{th} at $V_{\mathrm{DS}}=0.1$ V increases with the stress time, but V_{th} at $V_{\mathrm{DS}}=5$ V decreases as the stress time increases. This implies that the hot holes injected into the gate oxide and the trap states created at the grain boundaries of the drain junction screen each other as gate voltage V_{GS} is swept from low to high at constant drain voltage of $V_{\mathrm{DS}}=5$ V. After stress is applied for 10^4 s, the subthreshold region in which the channel exhibits weak inversion undergoes a parallel shift to lower V_{GS}, because the hot holes injected into the gate oxide shorten the channel. The hot holes in the gate oxide can be neutralized by attracting channel electrons during the forward stress applied for 10^2 s.[27] After the hot holes are released from the gate oxide, the subthreshold region shifts significantly toward higher V_{GS}, as shown in Fig. 10. This implies that a large number of deep states are generated at the grain boundaries of the drain junction after the first reverse stress has been applied for 10^4 s. However, the drain currents at large V_{GS} always decline as the stress time increases because acceptor-like states created at the grain boundaries of the drain junction are introduced into the channel and exhibit deep inversion. A comparison between OFF currents reveals donor-like states, as it does the acceptor-like states located near midgap. When negative V_{GS} is applied,

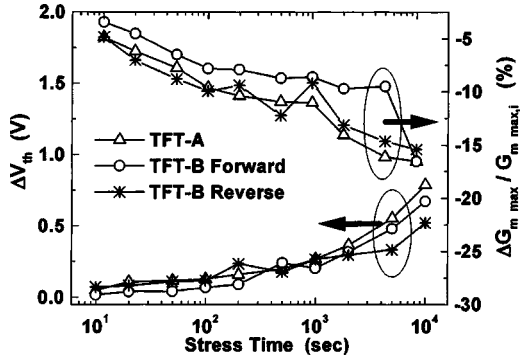

FIG. 11. Degradation of both the threshold voltage and the maximum transconductance of hydrogenated devices with the stress time. These devices were treated with NH_3 plasma for 4 h, and $\Delta V_{\rm th}$ and $\Delta G_{m\,\max}/G_{m\,\max,i}$ were evaluated at $V_{\rm DS}=0.1$ V for each stress time. Two devices of TFT-B were stressed in forward and reverse modes, respectively.

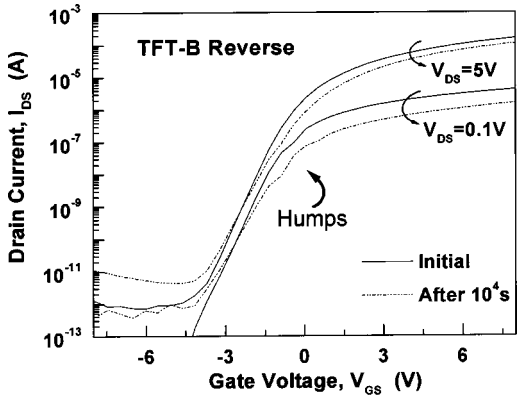

FIG. 12. Transfer characteristics of hydrogenated TFT-B measured in reverse mode before and after the reverse stress was applied for 10^4 s. The device was treated using NH_3 plasma for 4 h. The hump effect in the subthreshold region is observed before and after hot-carrier stress is applied.

the OFF current of the neutralization of hot holes increases more slowly than the initial OFF current at $V_{\rm DS}=5$ V, as shown in Fig. 10. The donor-like states are positively charged when negative $V_{\rm GS}$ is applied, so the electric field becomes weaker in the drain depletion region. This effect causes the OFF current that flows after stress has been applied for 10^4 s to be less than the initial OFF current at $V_{\rm GS}<-25$ V. This phenomenon is consistent with the results obtained by Brown and Migliorato.[28]

NH_3 plasma treatment can destroy the excellent hot-carrier reliability of devices with large grains in the drain junction. Figure 11 shows variations of $\Delta V_{\rm th}$ and $\Delta G_{m\,\max}/G_{m\,\max,i}$ with the stress time for devices that have been hydrogenated. One can see that hot-carrier reliability of hydrogenated TFT-B in reverse mode is effectively promoted. The high local electric fields created at grain boundaries of the drain junction can be effectively reduced because atomic hydrogen ties up the dangling and strained bonds during hydrogenation, thus reducing the number of carriers trapped at the grain boundaries. The Si–H bonds of the shallow tail states are easily bound and are easily broken because they have small binding energy.[17] Therefore, the behavior associated with degradation of devices differs from that of nonhydrogenated devices. Figure 11 exhibits the tendency to degrade. The degradation of devices after hydrogenation becomes independent of the original distribution of the grain boundaries in the channel region. Figure 12 shows the transfer characteristics in reverse mode of another hydrogenated TFT-B following stress for 10^4 s. In fact, the hydrogenated devices of TFT-A and TFT-B after being stressed exhibit increased OFF currents, decreased ON currents, and reduced subthreshold slopes. The mechanism for device degradation involves the breaking of many Si–H bonds, which creates the shallow tail states in the upper half of the band gap. Additionally, the hump effect appears in the subthreshold region, especially after the channel region is asymmetrically damaged by hot-carrier stress, as shown in Fig. 12. This is also consistent with observations of hydrogenated TFT-A and hydrogenated TFT-B in forward mode. The hump effect originates in the nonuniformity of the passivation of grain boundaries throughout the channel region. The center of the channel region has different turn-on characteristics from the two sides of the region because the lateral diffusion of hydrogen activates trap states.

IV. CONCLUSION

In this study we reported the effects of grain boundaries on the performance and hot-carrier reliability of the laser-crystallized poly-Si TFTs with and without hydrogenation. The hot-carrier reliability of the devices strongly depends on the location of grain boundaries rather than on the number of grain boundaries of the channel region. Grain boundaries in the drain junction increase the leakage current, cause the threshold voltage to decline as the drain bias increases; enhance the kink effect in output characteristics, and strongly degrade device performance under static hot-carrier stress. These effects are attributed to the generation of high local electric fields from surface roughness and trapping of charge at grain boundaries in the drain junction. NH_3 plasma treatment can effectively passivate grain boundaries that are randomly distributed in the channel region. However, hydrogenation introduces the hump effect into the subthreshold region, and causes a trade-off between the electrical characteristics and the hot-carrier reliability of laser-crystallized poly-Si TFTs.

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