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Citation: Applied Physics Letters **84**, 3822 (2004); doi: 10.1063/1.1745104
View online: http://dx.doi.org/10.1063/1.1745104
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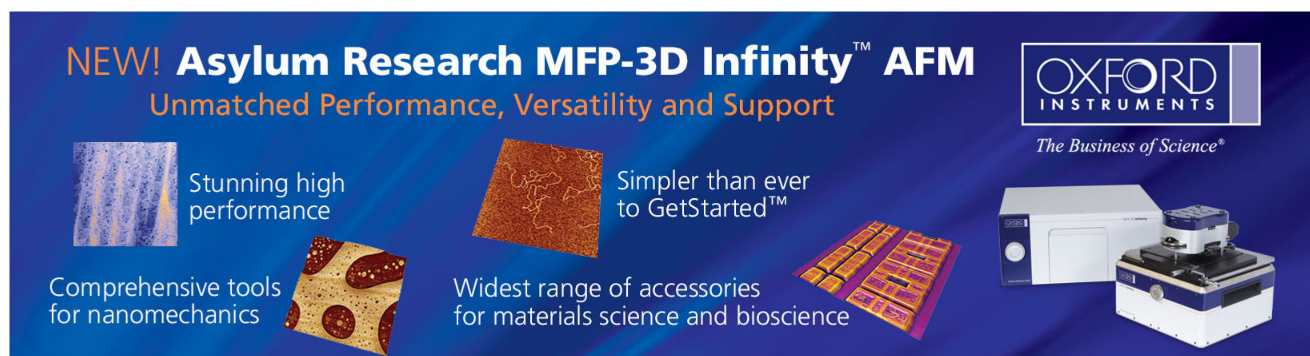

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HTML ABSTRACT + LINKS

High-performance polycrystalline silicon thin-film transistor with multiple nanowire channels and lightly doped drain structure

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(Received 6 January 2004; accepted 18 March 2004; published online 29 April 2004)

This investigation examines polycrystalline silicon thin-film transistors (TFTs) with multiple nanowire channels and a lightly doped drain (LDD). A device with an LDD structure exhibits low leakage current because the lateral electrical field is reduced in the drain offset region. Additionally, multiple nanowire channels can generate fewer defects in the polysilicon grain boundary and have more efficient NH_3 plasma passivation than single-channel TFTs, further reducing leakage current. They exhibit superior electrical characteristics to those of single-channel TFTs, such as a higher ON/OFF current ratio ($>10^8$), a better subthreshold slope of 110 mV/decade, an absence of drain-induced barrier lowering, and suppressed kink-effect. Devices with the proposed TFTs are highly promising for use in active-matrix liquid-crystal display technologies. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1745104]

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have attracted considerable attention because they can be used in active-matrix liquid crystal displays, since they perform very well and can be integrated with peripheral driving circuits on a low-cost glass substrate.[1,2] In addition, poly-Si TFTs have potential for use in three-dimensional circuits, including vertically integrated static[3] and dynamic random access memories.[4] Conventional poly-Si TFTs, however, suffer from anomalous leakage current in the OFF state, which correlates with the drain voltage and the gate voltage.[5,6] This undesirable OFF-state leakage current limits the application of poly-Si TFTs in switching devices. The dominant mechanism by which the leakage current in poly-Si TFTs is induced involves the field emission of carriers in grain boundary traps, due to the high electric field near the drain junction.[7] An effective method for reducing the electric field in the drain region is to incorporate a lightly doped drain (LDD) region between the heavily doped region and the active channel region.[8] Additionally, the presence of poly-Si grain boundary defects in the channel region of TFTs drastically affects the electrical characteristics.[9,10] Therefore, the reduction of the number of poly-Si grain boundary defects improves the performance of TFTs. TFTs with several multiple channels have been reported to effectively reduce grain boundary defects.[11–13] This work employs both the LDD structure and multiple nanowire channels (MNCs) to solve the problems just described to realize high-performance poly-Si TFTs.

This investigation proposes TFTs with a gate length of 0.5 μm consisting of ten strips of multiple 67-nm wire channels; a single-channel (SC) structure with $W=1$ μm was also fabricated for comparison. Silicon wafers with a 400-nm-thick layer of thermal oxide were used as the starting substrate. A thin 50-nm-thick undoped amorphous-Si (a-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C. The deposited a-Si layer was then recrystallized at 600 °C for 24 h in nitrogen ambient. After lithographicpatterning and plasma etching, the device active islands were formed. A 26-nm-thick layer of tetra-ethyl-ortho-silicate (TEOS) oxide and a 150-nm-thick layer of polysilicon were then deposited by LPCVD, and transferred to a gate electrode. Phosphorous ions were implanted in the lightly doped source and drain region at a dose of 5×10^{13} cm^{-2}. A 200-nm-thick layer of TEOS oxide was then deposited by LPCVD, and anisotropically etched by reactive ion etching to form a sidewall spacer that abutted the poly-Si gate. The self-aligned source and drain regions were then formed by the implantation of phosphorous ions at a dose of 5×10^{15} cm^{-2}. The dopant was activated by rapid thermal annealing. After source and drain implantation, a 300-nm-thick TEOS oxide layer was deposited as the passivation layer by LPCVD. Next, the contact hole was defined and Al metallization performed. The devices were then sintered at 400 °C in nitrogen ambient for 30 min. Finally, each device

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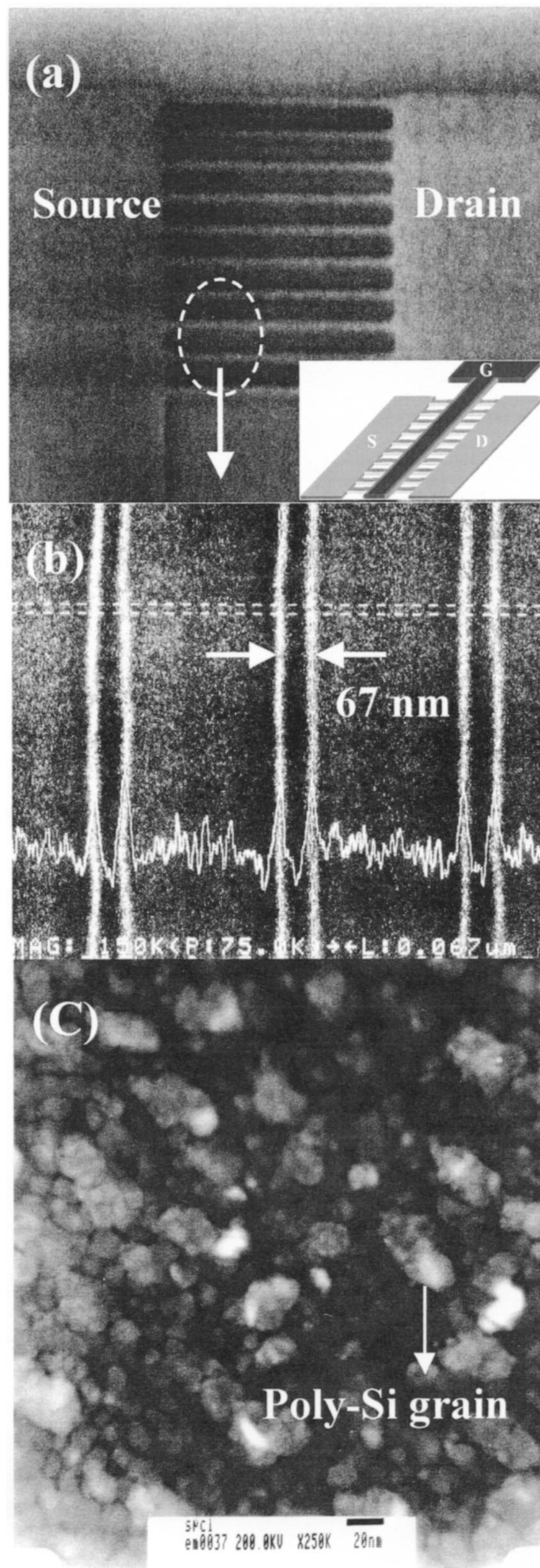

FIG. 1. (a) SEM photography of active pattern with the source, the drain, and MNCs. The inset plot shows the schematic figure of purposed TFTs. (b) Magnified area of MNCs. The each nanowire width is 67 nm. (c) TEM photography of poly-Si grains by solid phase crystallization. The average poly-Si grain size is about 30 nm.

was passivated by NH_3 plasma treatment for 1 h. Electron-beam lithography was used to perform all submicron pattern.

Figure 1(a) presents a scanning electron microscopy (SEM) photograph of the poly-Si active region in the TFTs, including the source, the drain, and MNCs. The inset plot depicts the proposed TFTs. Figure 1(b) presents a magnified area of MNCs in the TFTs, each of which is 67 nm wide. Figure 1(c) presents a plane view of a transmission electron microscope (TEM) photograph of the active region in the proposed TFTs. The average grain size in the poly-Si channel formed by solid phase crystallization is approximately 30 nm. Figures 2 and 3 present the electrical characteristics of these TFTs. Figure 2 plots a typical normalized transfer curve and the field-effect mobility of TFT devices with a SC and MNCs, respectively. The transfer characteristics imply that the ON-state current of MNC TFTs is approximately similar to that of SC TFTs. This fact suggests that the SC and MNC TFTs can yield almost the same carrier mobility, indicating that the carrier mobility is not degraded in MNC TFTs. Additionally, the leakage current of MNC TFTs is reduced significantly as gate voltage (V_g) becomes more negative at $V_d = 2$ V, compared to the SC TFTs. The MNC TFTs therefore have a higher current ON/OFF ratio ($>10^8$) than SC TFTs.

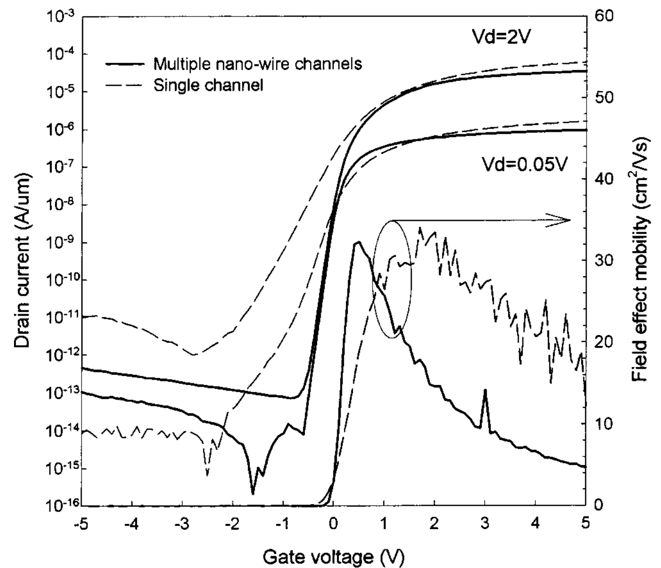

FIG. 2. Comparison of $I_d - V_g$ transfer characteristics of MNC ($W/L = 0.5$ μm/67 nm$\times$10) and SC ($W/L = 0.5$ μm/1 μm) poly-Si TFTs.

In addition, MNC TFTs have a smaller subthreshold slope (SS), and are free of drain-induced barrier lowering (DIBL), because they exhibit better gate control ability. The electrical characteristics of MNC TFTs are also better because the width of each NC is close to the size of a poly-Si grain (approximately 30 nm), as presented in Fig. 1(c). Therefore, MNC have fewer effective grain boundary defects than SC TFTs. Moreover, the effect of NH_3 plasma passivation more efficiently affects MNC TFTs than it does in SC TFTs, because the former has split nanowire structures that are mostly exposed to NH_3 plasma.

Figure 3 depicts the output characteristics of SC TFTs with channel length (L) of 0.5 μm and width (W) of 1 μm, as well as those of MNC TFTs with channel length (L) of 0.5 μm and width (W) of 67 nm$\times$10=0.67 μm. The applied gate voltage was maintained at a constant value of $V_g - V_{th} = 0.5$, 1.0, and 1.5 V, to prevent threshold voltages from being different. The suppressed kink-effect was observed for MNC TFTs, because they had fewer polysilicon grain boundary defects and exhibited more efficient NH_3

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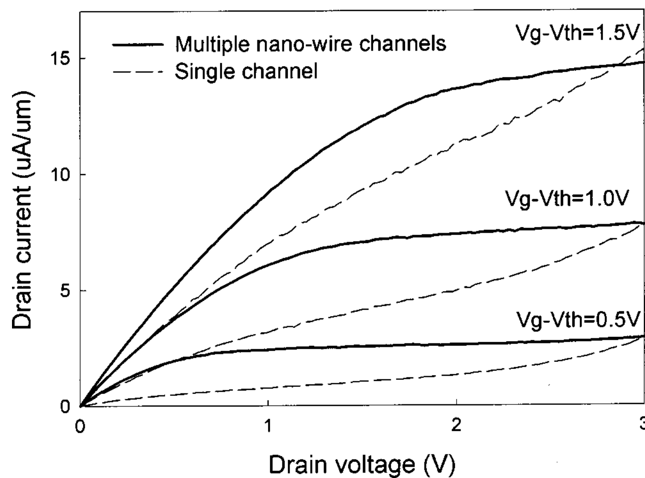

FIG. 3. Comparison of I_d–V_d output characteristics of MNC ($W/L = 0.5\ \mu$m/67 μm$\times 10$) and SC ($W/L = 0.5\ \mu$m/1 μm) poly-Si TFTs.

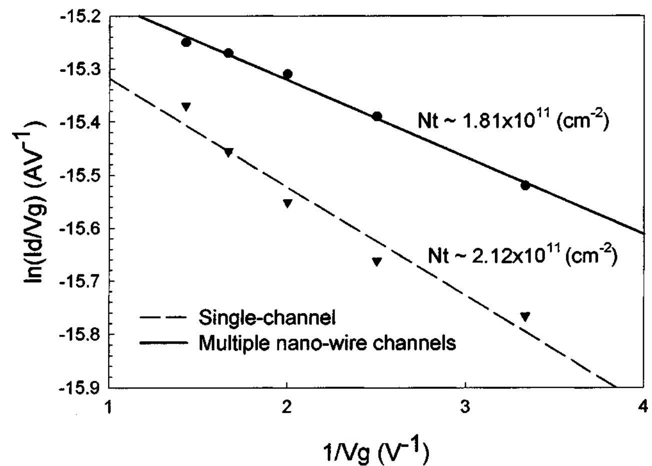

FIG. 4. Effective trap state density of MNC ($W/L = 0.5\ \mu$m/67 nm$\times 10$) and SC ($W/L = 0.5\ \mu$m/1 μm) poly-Si TFTs.

plasma passivation. Table I lists the electrical parameters of the TFTs, including threshold voltage (V_{th}), SS, ON/OFF ratio, and DIBL. V_{th} is defined as the gate voltage required to achieve a normalized drain current of $I_d = (W/L) \times 10^{-7}$ A at $V_d = 2$ V. DIBL is defined as $\Delta V_g / \Delta V_d$ at $I_d = 10^{-10}$ A. The effective trap state density (N_t) was extracted from the slope of $\ln(I_d/V_g)$ versus $(1/V_g)$ characteristics[9] for devices with multiple and single-channel TFTs, to elucidate the effect of grain boundary defects on the performance of such TFT devices. In Fig. 4, MNC TFTs exhibited a lower slope, indicating a lower effective trap state density ($N_t \sim 1.81 \times 10^{11}$) than SC TFTs ($N_t \sim 2.12 \times 10^{11}$). This result is also consistent with the aforementioned comparison of the performance of MNC with that of SC TFTs.

In conclusion, the size of the active region in multiple-nanowire-channel TFTs is close to the size of one poly-Si grain (~ 30 nm), resulting in fewer poly-Si grain boundary defects and more efficient NH_3 plasma passivation than the SC TFTs. Furthermore, extracting the effective trap state density (N_t) further verifies the effect of geometry on the electrical performance when the dimensions of the device approach the nanoscale regime. Therefore, MNC TFTs exhibit low leakage current in the off state, a high ON/OFF current ratio, a low subthreshold slope, an absence of DIBL, and favorable output characteristics. The fabrication of MNC TFTs is easy and involves no additional processes. Such TFTs are thus highly promising for use in future high-performance poly-Si TFT applications.

TABLE I. Device parameters of SC TFTs with $L/W = 0.5\ \mu$m/1 μm, and MNC TFTs with $L/W = 0.5\ \mu$m/67 nm$\times 10$. All parameters were extracted at $V_d = 2$ V, except for the field-effect mobilities, which were extracted at $V_d = 0.05$ V.

	Mobility (cm^2/V s)	V_{th} (V)	SS (mV/decade)	I_{on}/I_{off}	DIBL (V/V)
Single-channel	34.01	−0.11	360	5.90×10^7	0.40
Multiple-channel	32.50	0.23	110	4.73×10^8	0

The authors would like to acknowledge the National Science Council of the Republic of China, Taiwan for financially supporting this research under Contract No. NSC 92-2215-E-009-013. The National Nano Device Laboratory is appreciated for its technical support.

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