Schottky-Barrier S/D MOSFETs With High-K Gate Dielectrics and Metal-Gate Electrode

Shiyang Zhu, *Member, IEEE*, H. Y. Yu, *Student Member, IEEE*, S. J. Whang, J. H. Chen, Chen Shen, Chunxiang Zhu, *Member, IEEE*, S. J. Lee, *Member, IEEE*, M. F. Li, *Senior Member, IEEE*, D. S. H. Chan, *Senior Member, IEEE*, W. J. Yoo, Anyan Du, C. H. Tung, *Senior Member, IEEE*, Jagar Singh, Albert Chin, *Senior Member, IEEE*, and D. L. Kwong, *Senior Member, IEEE*

***Abstract*—This letter presents a low-temperature process to fabricate Schottky-barrier silicide source/drain transistors (SSDTs) with high-κ gate dielectric and metal gate. For p-channel SSDTs (P-SSDT) using PtSi sourece/drain (S/D) , excellent electrical performance of $I_{\rm on}/I_{\rm off} \sim 10^7 - 10^8$ and subthreshold slope of 66 mV/dec have been achieved. For n-channel SSDTs (N-SSDTs) using $DySi_{2-x}$ S/D , $I_{\rm on}/I_{\rm off}$ can reach $\sim 10^5$ at $V_{\rm ds}$ of 0.2 V with two subthreshold slopes of 80 and 340 mV/dec. The low-temperature process relaxes the thermal budget of high-κ dielectric and metal-gate materials to be used in the future generation CMOS technology.**

***Index Terms*—High-κ, metal gate, MOSFET, Schottky.**

I. Introduction

THE SERIES resistance of ultrashallow sourece/drain (S/D) junctions is a serious issue for future CMOS transistor scaling. Schottky-barrier silicide S/D (SSDT) structure has been suggested as a potential solution, due to the sharp silicide/silicon interface and low sheet resistance of silicide [1]–[5]. SSDT is particularly attractive when a metal-gate/high-κ gate stack is employed, as it avoids the use of a high-temperature annealing process required for implanted S/D junctions and poly gate, hence, eliminating the thermal stability issues associated with high-κ gate stack [6]. In this letter, we successfully demonstrate bulk SSDTs with HfO_2 high-κ dielectric, HfN metal gate, and PtSi (for pMOS) and $DySi_{2-x}$ (for nMOS) silicided S/D using a simplified low temperature process. The process can be easily extended to ultrathin body (UTB) silicon-on-insulator (SOI) structure to further improve the SSDT performance.

Manuscript received January 5, 2004. This work was supported by the Singapore A-STAR under Grant EMT/TP/00/001,2. The review of this letter was arranged by Editor A. Chatterjee.

S. Zhu is with the Department of Electrical and Computer Engineering, Silicon Nano Device Laboratory, National University of Singapore, 119260 Singapore, and also with the Department of Microelectronics, Fudan University, Shanghai, 200433 China.

H. Y. Yu, J. H. Chen, C. Shen, C. Zhu, S. J. Lee, D. S. H. Chan, and W. J. Yoo are with the Department of Electrical and Computer Engineering, Silicon Nano Device Laboratory, National University of Singapore, 119260 Singapore.

S. J. Whang is with the Jusung Engineering Co, Ltd., Gyeonggi 464-892 Korea.

M. F. Li is with the Department of Electrical and Computer Engineering, Silicon Nano Device Laboratory, National University of Singapore, Singapore 119260 and also with the Institute of Microelectronics, 117685 Singapore (e-mail: elelimf@nus.edu.sg).

A. Du, C. H. Tung, and J. Singh are with the Institute of Microelectronics, 117685 Singapore.

A. Chin is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, 300 Taiwan, R.O.C.

D. L. Kwong is with the Department of Electrical and Computer Engineering, University of Texas, Austin, TX 78712 USA.

Digital Object Identifier 10.1109/LED.2004.826569

II. MOS Device Fabrication

Si (100) wafers of both n– and p-type with resistivity of 4–8 $\Omega \cdot$ cm were used as the starting substrate. First, ~6-nm HfO_2 film was deposited on Si at 400 °C using $Hf[OC(CH_3)_3]_4$ and O_2 in a metal–organic chemical vapor deposition system, followed by an *in situ* annealing in N_2 ambient at 700 °C.Then HfN(~50 nm) and TaN(~100 nm) were deposited sequentially in a sputtering system with base pressure of 1.5×10^{-7}torr. TaN is used as a capping layer to reduce the gate sheet resistance (~ 10 Ω sq) [7]. The wafers were patterned using photolithography and reactive ion etching procedures. Immediately after dipping in a diluted hydrogen fluoride solution (DHF), the wafers were loaded into the sputtering system again for platinum (~100 nm) (for P-SSDT) or dysprosium (~100 nm)/HfN (~70 nm) stack (for N-SSDT) deposition. Since Dy is easily oxidized during *ex situ* anneal, a capping layer of thermally stable HfN [7] is used to prevent Dy oxidization. Silicidation of Pt or Dy was performed by forming gas anneal at 420 °C for 1 h. Then unreacted Pt was removed by hot diluted Aqua Regia etch. The HfN capping layer and unreacted Dy were etched by DHF and a diluted HNO_3 solution sequentially.

Although PtSi has flat surface, the surface of $DySi_{2-x}$ film is quite rough. This is because $DySi_{2-x}$, as well as other rare earth (RE) silicides, is not formed through layer-by-laye, but islanded-preferred during the solid-state reaction with substrate Si [8]. No improvement to the $DySi_{2-x}$ film morphology was found by using other capping layers such as Pt, Ti, Ta, Ru, and Al, etc. or by *in situ* vacuum anneal without a capping layer. HfN is found to be the most suitable capping layer in our study, due to its easy removal and no contamination in $DySi_{2-x}$.

III. Device Characterization and Discussion

For the PtSi/n-Si Schottky contact, the electron barrier height ($\Phi_{\rm bN}$) was measured to be 0.85 and 0.86 eV from current–voltage (*I–V*) and capacitance–voltage (*C–V*), respectively. The corresponding hole barrier height ($\Phi_{\rm bP} \cong E_g - -\Phi_{\rm bN}$) is about 0.26 eV, close to the reported value [9]. For the $DySi_{2-x}$/p–Si diode, Fig. 1 shows that $\Phi_{\rm bP}$ are 0.66 eV (*I–V*) and 0.88 eV (*C–V*), compared to the reported value of ~0.74 eV for the $DySi_{2-x}$ film formed by ultrahigh vacuum evaporation [9]. The large difference in $\Phi_{\rm bP}$ from *C–V* and *I–V*, and the larger than

0741-3106/04$20.00 © 2004 IEEE

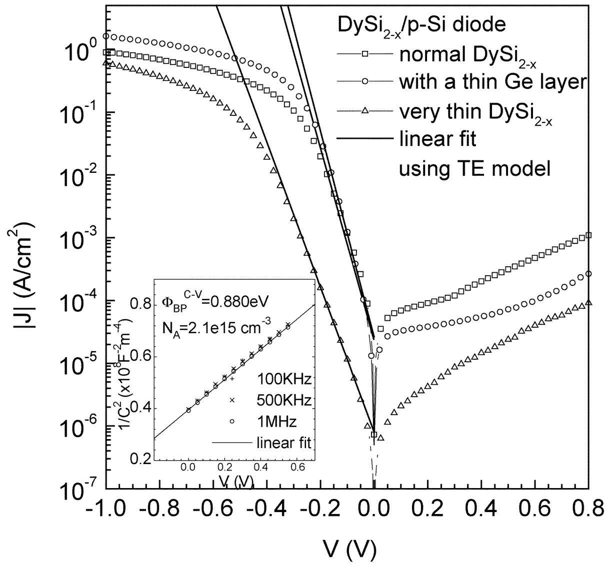

Fig. 1. *I–V* curves of three different $DySi_{2-x}$/p–Si diodes. (1) Normal $DySi_{2-x}$ formed by Dy/Si silicidation at 420 °C for 1 h. (2) Adding an ultrathin intermediate Ge layer (∼1 nm). (3) A very thin $DySi_{2-x}$ with an Al capping layer. The barrier heights $\Phi_{\rm bP}$ and ideality factors deduced from the thermal emission model are (0.66 eV, 1.10), (0.72 eV, 1.05), and (0.82 eV, 1.46), respectively. The inset is the *C–V* curves of diode 1. The deduced $\Phi_{\rm bP}$ and $\rm N_A$ are 0.88 eV and 2.1×10^{15} $\rm cm^{-3}$, respectively. Other two diodes have the similar *C–V* results within the experimental error.

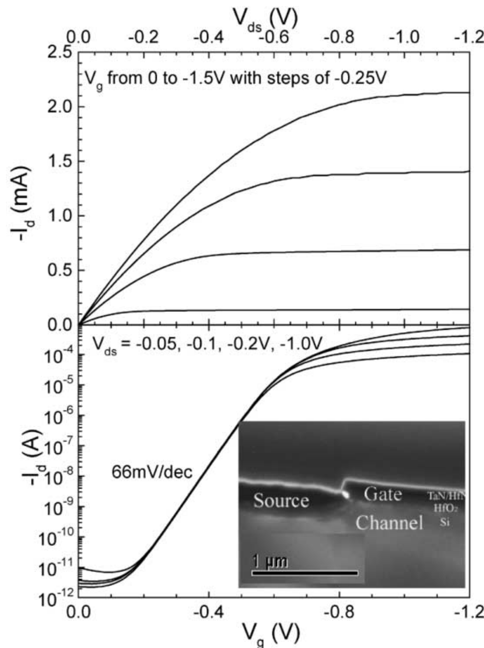

Fig. 2. I_d–$V_{\rm ds}$ and I_d–V_g curves of P-SSDT with PtSi S/D. The channel width and length are 400 and 4 μm. Equivalent oxide thickness (EOT) of HfO_2 gate dielectric is 2.0 nm, $V_t = -0.56$ V. The inset is the XTEM image of the device structure. A “hole” between S/D and channel acts as a sidewall spacer.

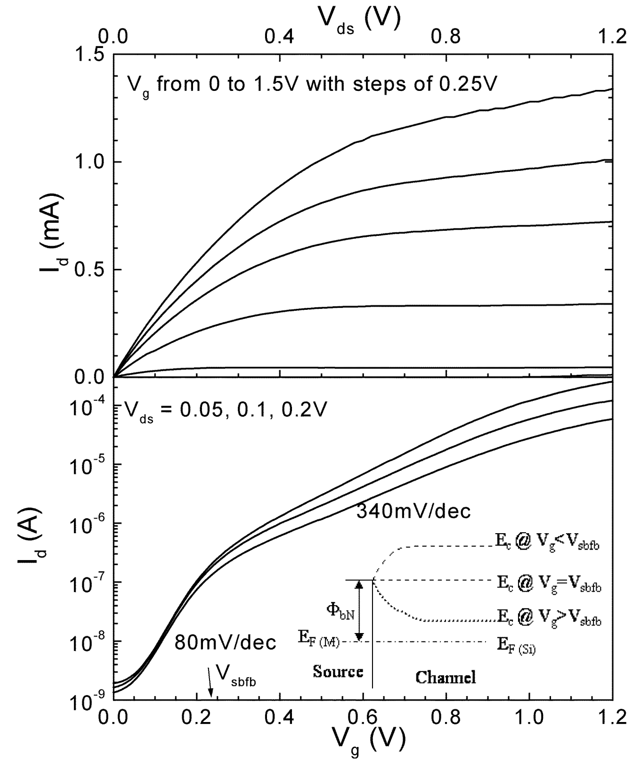

Fig. 3. I_d–V_g and I_d–V_g curves of N-SSDT with $DySi_{2-x}$ S/D. The channel width and length are 400 and 4 μ m. EOT is 1.5 nm, $S = 80$ mV/dec at $V_g < 0.23$ V, and 340 mV/dec at $V_g > 0.23$ V, $V_t = 0.56$ V. The inset is the schematic band diagram of Schottky barrier at source/channel. If the device is already turned on before V_g reaches $V_{\rm sbfb}$, it shows one subthreshold slope as conventional device. Otherwise, it shows two subthreshold slopes because the slope reduces dramatically when $V_g > V_{\rm sbfb}$.

unity ideality factor (n) imply significant barrier height inhomogeneity of the $DySi_{2-x}$/Si interface [10], associated with the rough surface and interface of $DySi_{2-x}$/Si as observed by atomic force microscopes and cross-sectional transmission electron microscope (XTEM) measurements. Fig. 2 and the inset show the *I–V* characteristics of P-SSDT and the device structure. The drain current at small $V_g(I_{\rm off})$ is between 1–10 pA for devices with drain area of 1×10^{-4} $\rm cm^2$, close to the theoretical value of the reverse current of the PtSi/n-Si diode with barrier height of 0.86 eV (∼3.8 pA). $I_{\rm on}$ depends on process parameters more sensitively. In our simplified one-mask process, a “hole” between the S/D and gate is formed during DHF dipping because HfN can be etched by DHF while TaN cannot. The “hole” acts as a spacer to separate the S/D and the gate. The “hole” size can be controlled by DHF dipping time. For the $W/L = 200/2.5-\mu$m devices, the $I_{\rm on}$ at $V_g = V_{\rm ds} = -2.5$ V increases from 3.5 to 6.2 mA by reducing the DHF dipping time from 105 to 60 s. Our P-SSDTs have a $I_{\rm on}/I_{\rm off}$ ratio $\sim 10^8$ at $V_g = V_{\rm ds} = -1.0$ V, with the subthreshold slope of 66 mV/dec. Their performance is similar to or even slightly better than the best reported data for SiO_2/poly-Si gate P-SSDT [11]. N-SSDT has ∼three orders of magnitude larger $I_{\rm off}$ than P-SSDT. Fig. 3 shows that the $I_{\rm on}/I_{\rm off}$ ratio at a small $V_{\rm ds}$ (0.2 V) is about 10^5, close to the recently reported value of N-SSDT on SOI [12]. $I_{\rm off}$ increases significantly at large $V_{\rm ds}$ due to the quick increase of the $DySi_{2-x}$/p–Si diode leakage current with the increase of the reverse bias (see Fig. 1). The transfer I_d–V_g curves of N-SSDT show two different subthreshold slopes ∼80 mV/dec at $V_g < 0.23$ V ($V_{\rm sbfb}$: source-body flatband voltage) and ∼340 mV/dec at $V_g > 0.23$ V. This behavior, as well as the large $I_{\rm off}$ observed in N-SSDT, can be explained by the relatively low hole barrier height $\Phi_{\rm bP}$ of the $DySi_{2-x}$/p–Si contact as compared to the electron barrier height $\Phi_{\rm bN}$ of the PtSi/n-Si contact in P-SSDT. As shown in the inset of Fig. 3, the tunneling

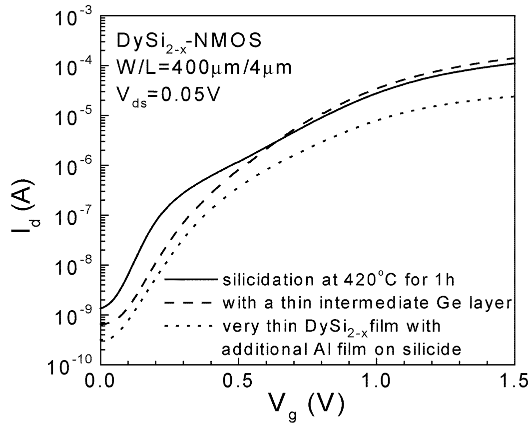

Fig. 4. Transfer curves of N-SSDTs with $DySi_{2-x}$ S/D formed at different conditions, (also see Fig. 1). The device with very thin $DySi_{2-x}$ has lower $I_{\rm off}$ and $I_{\rm on}$. The $I_{\rm on}/I_{\rm off}$ ratio at $V_{\rm ds} = 50$ mV is improved about 4 to 5 times by adding a very thin (~1 nm) Ge intermediate layer.

current $(J_{\rm TN})$ in N-SSDT through the electron Schottky barrier $\Phi_{\rm bN} \cong E_g - \Phi_{\rm bP} = 0.38$ eV between source and channel dominates in the $V_g > V_{\rm sbfb}$ region, resulting in two slopes below threshold [5], [13]. It exhibits only one subthreshold slope if $V_{\rm sbfb}$ is larger than the threshold voltage $(V_{\rm th})$, which requires $\Phi_{\rm bN} < E_g/2 - (kT/q)\ln(N_A/n_i)$ (~0.26 eV in our case) and this condition is not satisfied for $DySi_{2-x}$/Si Schottky junction. On the other hand, PtSi–Si contact meets the requirement of $\Phi_{\rm bP} < E_g/2 - (kT/q)\ln(N_D/n_i)$ (~0.27 eV) for P-SSDT. Therefore, only one subthreshold slope of 66 mV/dec is observed in P-SSDT.

Low barrier height is a key issue for SSDT. RE silicides have the lowest electron barrier height among the known silicides [9]. However, their barrier height is not low enough to meet the N-SSDT requirement. Even worse, the large barrier height inhomogeneity of the RE silicide/Si contact causes $I_{\rm off}$ (~ 25 μA/cm^2) larger than the theoretical value of a uniform barrier height (~ 1.1 μA/cm^2 for $DySi_{2-x}$/p–Si diode with $\Phi_{\rm bP} = 0.74$ eV). Improving the RE silicide quality and reducing its barrier height are big challenges for N-SSDT. We found that adding a very thin (~1 nm) deposited amorphous Ge intermediate layer can improve the $DySi_{2-x}$ film morphology significantly, because the amorphous Ge may suppress the crystallization of $DySi_{2-x}$ during its growth. The better diode performance is shown in Fig. 1 with $\Phi_{\rm bP}$ of 0.72 eV, n of 1.05, and about half order of magnitude lower reverse current than the normal ones. In Fig. 4, the transistor performance is also improved. The $I_{\rm on}/I_{\rm off}$ ratio at $V_{\rm ds} = 0.05$ V increases about 4 to 5 times. Very thin $DySi_{2-x}$ film has quite smooth surface, which can be formed by low temperature (300 °C, 1 h) or short time (400 °C, 1 min) anneal. In this case, an additional metal (such as Al) film on the $DySi_{2-x}$ is necessary to reduce the series resistance. Fig. 1 shows that $\Phi_{\rm bP}$ and n are 0.82 eVand 1.46, respectively. Fig. 4 shows that $I_{\rm off}$ at small V_g and $V_{\rm ds}$ is reduced by 8 to 9 times. The value of ~ 2.0 μA/cm^2 is close to the theoretical prediction. However, $I_{\rm on}$ is also reduced due to the large S/D series resistance. Further improvement of the electrical performance of N-SSDT needs $\Phi_{\rm bN}$ to be reduced to less than 0.2 eV with quite smooth interface. The use of UTB-SOI also helps due to the reduction of the Schottky contact area.

In conclusion, N- and P-SSDTs with high-κ dielectric and metal gate were demonstrated for the first time using a low temperature process. The transistors have comparable electrical performance to the best data of SSDT reported so far.

REFERENCES

[1] M. P. Lepselter and S. M. Sze, "SB-IGFET: An insulated-gate field-effect transistor using Schottky barrier contacts for source and drain," *Proc. IEEE*, vol. 56, pp. 1400–1401, 1968.

[2] M. Nishisaka, S. Matsumoto, and T. Asano, "Schottky source/drain SOI MOSFET with shallow doped-extension," in *Proc. Int. Conf. Solid State Devices and Materials*, 2002, pp. 586–587.

[3] J. P. Snyder, C. R. Helms, and Y. Nishi, "Experimental investigation of a PtSi source and drain field-emission transistor," *Appl. Phys. Lett.*, vol. 67, pp. 1420–1422, 1995.

[4] H.-C. Lin, M. F. Wang, F. J. Hou, H. N. Lin, C. Y. Lu, J. T. Liu, and T. Y. Huang, "High-performance P-channel Schottky-barrier SOI FinFET featuring self-aligned PtSi source/drain and electrical junctions," *IEEE Electron Device Lett.*, vol. 24, pp. 102–104, Feb. 2003.

[5] J. Kedzierski, P. Xuan, E. H. Anderson, J. Bokor, T. J. King, and C. H. Hu, "Complementary silicide source/drain thin-body MOSFETs for the 20-nm gate length regime," in *IEDM Tech. Dig.*, 2000, pp. 57–60.

[6] C. S. Kang, H. J. Cho, K. Onishi, R. Choi, R. Nieh, S. Goplan, S. Krishnan, and J. C. Lee, "Improved thermal stability and device performance of ultrathin (EOT< 10 Å) gate dielectric MOSFETs by using Hafnium Oxynitride (HfO_xN_y)," in *Symp. VLSI Tech. Dig.*, 2002, pp. 146–157.

[7] H. Y. Yu, J. F. Kang, J. D. Chen, C. Ren, Y. T. Hou, S. J. Whang, M. F. Li, D. S. H. Chan, K. L. Bera, C. H. Tung, A. Du, and D. L. Kwong, "Thermally robust high quality HfN/HfO_2 gate stack for advanced CMOS devices," *IEEE Electron Device Lett.*, vol. 25, pp. 70–72, Jan. 2004.

[8] B. Z. Liu and J. Nogami, "A scanning tunneling microscopy study of dysprosium silicide nanowire growth on Si(001)," *J. Appl. Phys.*, vol. 93, pp. 593–599, 2003.

[9] Z. Xu, *Properties of Metal Silicides*, K. Maex and M. Van Rossum, Eds. London, U.K.: IEEE-Inspec, 1995, p. 217.

[10] R. T. Tung, "Electron transport at metal-semiconductor interfaces: general theory," *Phys. Rev. B, Condens. Matter*, vol. 45, pp. 13 509–13 523, 1992.

[11] L. E. Calvet, H. Luebben, M. A. Reed, C. Wang, J. P. Snyder, and J. R. Tucker, "Suppression of leakage current in Schottky barrier metal-oxide-semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 91, no. 2, pp. 757–759, 2002.

[12] M. Jang, J. Oh, S. Maeng, W. Cho, and S. Lee, "Characteristics of erbium-silicided n-type Schottky-barrier tunnel transistors," *Appl. Phys. Lett.*, vol. 83, no. 13, pp. 2611–2613, 2003.

[13] J. Knoch and J. Appenzeller, "Impact of the channel thickness on the performance of Schottky-barrier metal–oxide–semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 81, no. 16, pp. 3082–3084, 2002.