0.13-μm Low-κ–Cu CMOS Logic-Based Technology for 2.1-Gb High Data Rate Read-Channel

Jyh Chyurn Guo, W. Y. Lien, T. L. Tsai, S. M. Chen, and C. M. Wu

***Abstract*—High-performance analog/digital elements have been successfully fabricated bya 0.13-μm low-κ–Cu logic-based mixed-signal CMOS process in a single chip to enable a 2.1-Gb/s read-channel for hard disk drives that is a record-high data rate supported by fully CMOS solution. The high-performance analog devices demonstrate superior drivability, matching, noise immunity, and reliability by a unique dual-gate oxide module to support the aggressive oxide thickness scaling and maintain promisingly good reliability in all aspects.**

***Index Terms*—Dual-gate oxide, high-performance analog (HPA), read-channel.**

I. Introduction

THE CONTINUOUS advancement of CMOS technology has paved the way for system-on-chip (SoC) circuits and mixed-signal (MS) or radio frequency (RF) elements in a single chip [1], [2]. Hard disk drive (HDD) read-channel integrated circuits, which demand high-density recording and high-speed processing, turn out a good practice for CMOS logic-based SoC technology [1]–[4]. The choice between analog and digital schemes to implement the major functions of read-channels is based on several tradeoffs. A digital implementation can reduce design cycle time and enable easier migration to next-generation technology, but may suffer higher cost in a Si area estate with larger transistor count and higher power. However, the demand of higher performance and faster time-to-market (TTM) has driven the trend toward digital read-channel architecture [1]. In this topology, the analog signal containing HDD data is sampled and digitized by a fast analog-to-digital converter (ADC). The equalization is done by the analog filter and some by the digital filter, and the detector is implemented digitally. The migration to a more digital-intensive read-channel design enables a faster fabrication process, higher circuit speed, and faster TTM attributed to less redesign effort. In this paper, we will report a successful practice on a 2.1-GB/s read-channel by using aggressively scaled I/O–analog devices of $T_{\rm OX} = 37$ Å (physical oxide thickness) and $L_g = 0.24$ μm (physical gate length) combined with a high-speed logic core of $T_{\rm OX} = 17$ Å and $L_g = 0.08$ μm, both under overdrive at 2.5/1.2 V, respectively. Noise and reliability are two major challenges for the high data rate read-channel at the speed beyond 1 Gb/s, and the whole suite of issues move from a second-order effect to the major concern such as interconnect delay, noise coupling, voltage-controlled oscillator (VCO) jitters, etc. We will prove a high-performance analog (HPA) device's advantages in terms of lower flicker noise, better matching, better time-dependent dielectric breakdown (TDDB) and hot carrier injection (HCI) lifetimes, and comparable negative bias temperature instability (NBTI).

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J. C. Guo is with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, 300 Taiwan, R.O.C. (e-mail: jcguo@mail.nctu.edu.tw).

W. Y. Lien, T. L. Tsai, S. M. Chen, and C. M. Wu are with the Taiwan Semiconductor Manufacturing Company, Hsinchu, 300 Taiwan, R.O.C.

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II. HPA Device Performance

To enable the high data rate read-channel circuits, active devices of high speed, good matching, and noise immunity are required. Besides, passive elements (resistors and capacitors) of superior linearity and matching are desired to ensure the proper function of the high-speed mixed-signal circuits used in the read-channel.

A. HPA Device Offering and Performance—Active and Passive

As mentioned, fast ADC is required for digital-intensive read-channel design and the figure-of-merit (FoM) $=$ Speed $*$ Accuracy^2/Power $= 1/{\rm C_{OX}Avt^2}$ [5] suggests the advantage offered by $T_{\rm OX}$ scaling and provides the guideline for HPA device optimization. Table I summarizes the HPA device portfolio with the key performance parameters and comparison with the standard I/O. Apparently, the aggressive $T_{\rm OX}$ scaling from 50 Å to 37 Å for 2.5-V analog–I/O devices contributed the superior drivability of $I_{\rm DSAT} = 740/320$ μA/μm (saturation current) for standard threshold voltage (STD-V_T) n/pMOS devices, respectively, which is an increase of around 20%/12% compared to the standard 2.5-V I/O with $T_{\rm OX} = 50$ Å. The appropriate scaling of gate length (L_g) by 0.02 μm can compensate for the increase of gate capacitance loading due to the much thinner oxide (37 Å versus 50 Å) and achieve somewhat faster gate delay. Table II indicates the benefit provided by 2.5-V HPA devices in terms of I/O circuit performance in which pull-up/pull-down currents are boosted by 20% to 29%/32% to 43%, and the input-rising/output-falling delays are reduced by 9% to 31%/12% to 19%, corresponding to four-corner (TC: typical; BC: fast corner; WC: slow corner; LT: fast corner at -40 °C) simulation. Regarding the logic core devices of $T_{\rm OX} = 17$ Å, $I_{\rm DSAT}$ as high as 800–380 μA/μm have been realized for 80–85-nm n/pMOS devices under overdrive at 1.2 V, which is an enhancement of around 36% to 40% over the normal operation at 1.0 V. It is noted that the adoption of a unique 37-Å recipe into the dual-gate oxide module can successfully realize 2.5-V HPA, maintain the core performance, and extend the use of the existing Spice model

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TABLE I
HPA 37-Å DEVICE PORTFOLIO AND THE COMPARISON WITH 50Å I/O DEVICE

Device Offering	HPA 37A			50A IO		Core	
V_T Options	Std-V_T		Low-V_T	Std-V_T		Std-V_T	
Device Type	NMOS	PMOS	NMOS	NMOS	PMOS	NMOS	PMOS
V_{DD} (v)	2.5			2.5V		1.0/1.2	
T_{OX} (A)	37			50		17	
$L_{NOM(TEM)}$ (μm)	0.24	0.24	0.24	0.26	0.26	0.08	0.085
V_T@C.C. (V)	N/A	N/A	N/A	0.48	-0.51	0.25	-0.29
V_T@$G_{M,MAX}$ (V)	0.5	-0.5	0.08	N/A	N/A	N/A	N/A
I_{DSAT}@V_{DD} (μA/μm)	740	320	1050	620	285	590/800	270/380
$I_{OFF(MAX)}$@V_{DD} (nA/μm)	0.2	0.2	5×10^4	0.1	0.1	10	10
R.O. Delay (ps/stage)	28		N/A	29		13.8	

TABLE II
2.5-V I/O CIRCUIT PERFORMANCE SIMULATION RESULTS: HPA 37-Å VERSUS 50Å I/O COMPARISON

Driver	Pull-up				Pull-down			
Corner	BC	TC	WC	LT	BC	TC	WC	LT
Current	124.9%	119.7%	106.3%	128.6%	138.6%	132.5%	134.9%	143.4%

Delay	Rising Edge Progation				Falling Edge Progation			
Corner	BC	TC	WC	LT	BC	TC	WC	LT
Input	96.2%	91.0%	**69.2%**	96.7%	102.7%	101.9%	102.8%	101.4%
Output	96.2%	97.2%	97.4%	94.9%	88.0%	87.9%	**81.4%**	88.4%

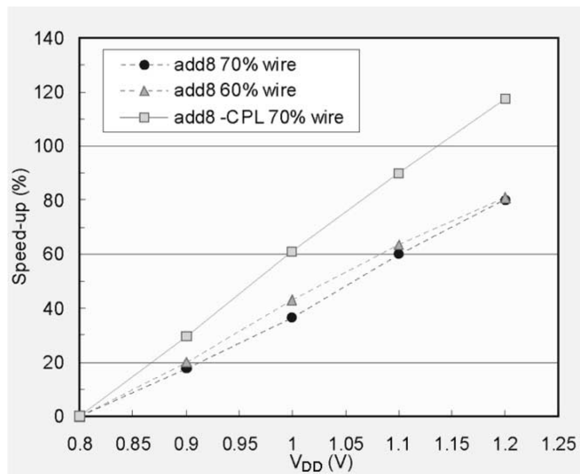


Fig. 1. Logic core supply voltage effect on read-channel data rate calculated by simulation with normal and enhanced logic circuit architectures.

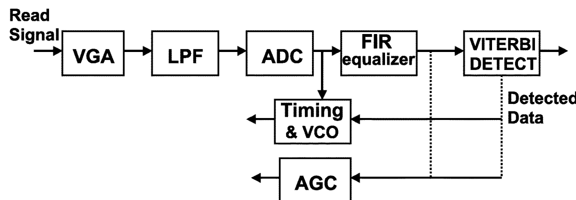


Fig. 2. PRML functional circuit diagram adopted by read-channel integrated circuit.

for logic core. Fig. 1 illustrates the data rate simulated for read-channel circuit in which the overdrive from 1.0–1.2 V can boost the data rate from 1.3/1.5–1.7/2.1 Gb/s, corresponding to normal/enhanced logic circuit architectures. In this paper, the complementary-pass logic (CPL) is employed as the enhanced circuit architecture to increase the speed with minimum power. Fig. 2 demonstrates the brief functional diagram of partial-response maximum likelihood (PRML) [6] generally adopted by a read-channel integrated circuit to better our understanding of a logic device/circuit performance's impact on read-channel data rate. First, the input signal, a kind of analog signal containing HDD data, is sampled and digitized by a fast ADC. The read-back signal is first adjusted by a variable gain amplifier (VGA), which is driven by automatic gain control (AGC). The low-pass filter (LPF) is used to attenuate the high-frequency noise before sampling. The ADC provides the digital signals for equalization by an adaptive filter. The adaptive equalizer is used to increase the transfer rate and recording density, and the digital finite-impulse response (FIR) filter is a major part of the adaptive equalizer in HDD PRML read-channel. CPL just serves as a high-speed logic circuit topology of choice to implement the FIR. It is noted that low-K–Cu did some help to reduce the wire delay and enhance the speed. Besides the high-speed transistors, passive elements of high linearity and good matching required for the read-channel circuits are summarized in Table III. Linear MOScap is a kind of N^+ polygate-based capacitor with improved voltage linearity realized by an extra heavy dose N^+ implant on N-well illustrated in Fig. 3(a). The capacitance–voltage (*C*–*V*) characteristics measured from our linear MOScap shown in Fig. 3(b) indicate the unit area capacitance density of around 7.3 fF/μm^2, which is equivalent to an electrical oxide thickness of 47 Å. The decrease of capacitance under positive/negative biases is corresponding to the depletion of N^+gate/N^+-well, respectively. Regarding the voltage linearity, the first order of voltage coefficient (VCC1), as small as 5700 ppm/V, has been achieved to meet the specification of 20 000 ppm/V. An interdigitated metal–oxide–metal (ID MoM) capacitor is an offering free of extra masks but a smart utilization of low-K–Cu interconnect coupling capacitance. Just following the specification defined in Table III, we can meet the per-unit area capacitance target of 0.2/1.0 fF/μm^2 corresponding to a single layer/five layers by using a 0.13-μm low-K–Cu interconnect with minimum M2 rule of width/space $= 0.2/0.21$ μm. Due the fact that the ID MoM capacitance is a kind of parasitic capacitance by nature, the sensitivity of HPA design's criterion with respect to low-κ–Cu back-end-of-line (BEOL) process variation and the uniformity control achievable becomes a general concern. Fig. 4 illustrates the capacitance density histogram plots representing the statistical distribution collected from three lots with more than 580 dies. The ID MoM capacitors used in this paper are five-layer structures with finger number fixed at 179 but with various finger widths in the range of 80–640 μm. Fig. 4(a)

TABLE III
PASSIVE ANALOG ELEMENT PERFORMANCE AND COMPARISON WITH THE TARGET

Components	Feature	HPA Target	Si Performance
Triple Well	Isolated P-well to improve noise immunity	R_S=1000ohm/sq	
Linear MOScap	N^+ well implant to improve linearity	C_0 > 5fF/μm^2	7.03~7.29fF/μm^2 (-3~+3V)
	1st order of linearity w.r.t voltage	V_{CC1} < 0.2% (20,000ppm/V)	0.057% (5,700ppm/V)
ID MoM	Multi-layer inter-digitated metal cap.	0.2fF/μm^2 per layer	0.2004fF/μm^2
		1.0fF/μm^2 +/-30%	1.002fF/μm^2 +/-3.3%
Resistors	N-well	400~1700 ohm/sq	Diffusion : 525+131 ohm/sq
			Under STI:1200+/-340
	Non-silicided N^+ diffusion	50~200 ohm/sq	66+/-13 ohm/sq
	Non-silicided P^+ diffusion	100~300 ohm/sq	104+/-21 ohm/sq
	Non-silicided Poly	100~600 ohm/sq	N^+PO : 124+/-25 ohm/sq
			P^+PO : 300+/-60 ohm/sq
	Silicided N^+, P^+ OD, Poly	< 20 ohm/sq	7.44~8.08 ohm/sq

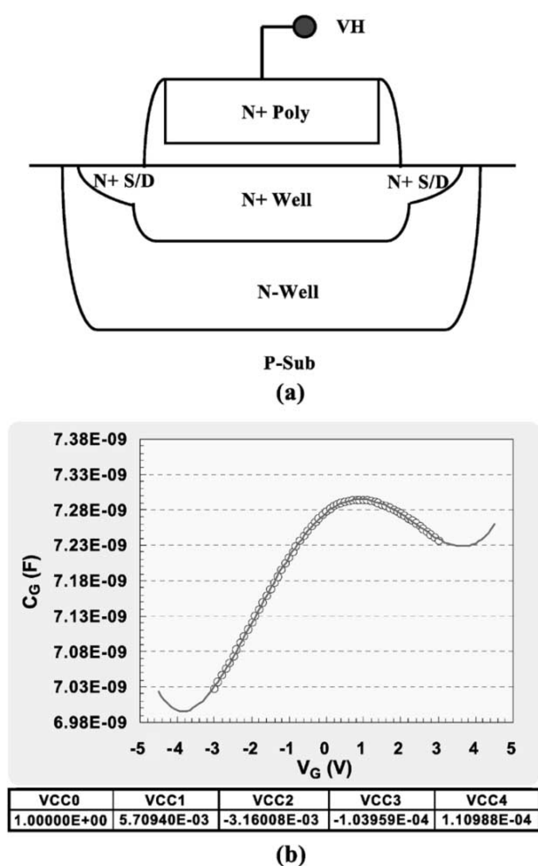


Fig. 3. (a) Linear MOScap structure with N^+ gate on N-well in which an extra heavy dose N^+ implant was performed to improve the voltage linearity. (b) *C–V* characteristics and the extracted voltage coefficients in the first, second, third, and fourth orders denoted as VCC1, VCC2, VCC3, and VCC4.

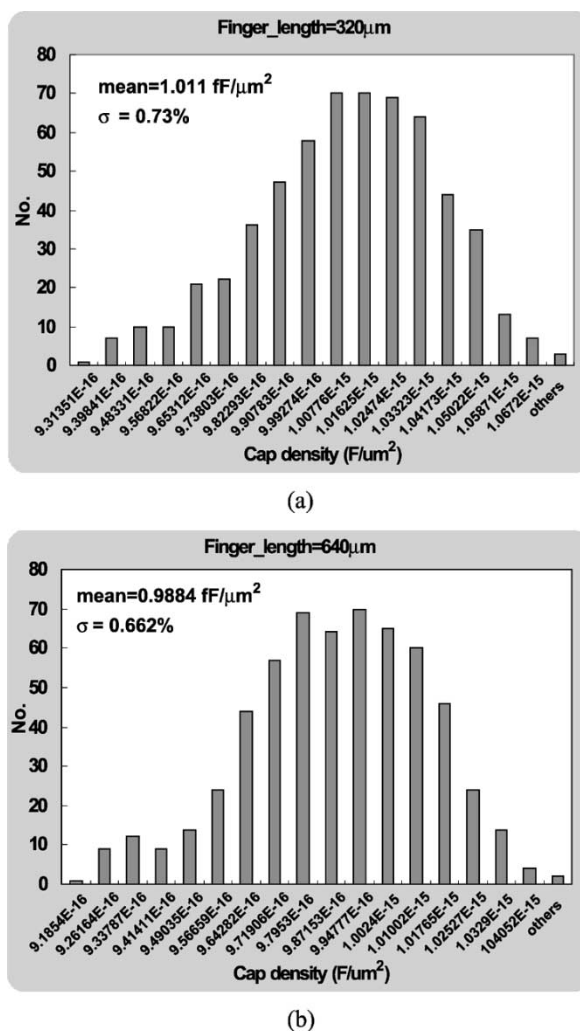


Fig. 4. (a) ID MoM capacitors' area capacitance density histogram collected from three lots with 588 dies metal finger width $= 320$ μm. (b) Metal finger width $= 320$ μm. Finger number is fixed at 179.

and (b) indicates the result measured from the structures with finger widths of 320 and 640 μm, respectively, in which the mean values are 1.0111 and 0.9884 fF/μm^2 and the standard deviations by one σ are 0.73% and 0.66%, respectively. The comparatively small deviation, i.e., $3\sigma < 3\%$, provides ten times larger margin from the general specification, i.e., 30%, and it indicates the uniformity control is excellent. Regarding the impact of unavoided low-κ–Cu BEOL process variation on the uniformity control of unit area capacitance density for the ID MoM with various stack metal/intermetal dielectric layer numbers (1 – 5), a Monte Carlo simulation has been done to investigate the metal thickness and width variation effect on metal R_S (sheet resistance) and the coupling capacitance. The simulated results reveal interesting and important findings that the

TABLE IV
METAL R_S AND COUPLING CAPACITANCE VARIATION OF LOW-K–Cu ID MOM CAPACITOR BY USING MONTE CARLO SIMULATION

ID MoM Stack Layer #	Metal R_S-3σ	ID MoM Cap.-3σ
1 Metal	32.9 %	18.5 %
2 Parallel Metal Layers	32.9 %	13.0%
3 Parallel Metal Layers	32.9 %	10.6%
4 Parallel Metal Layers	32.9 %	9.1%
5 Parallel Metal Layers	32.9 %	8.1%

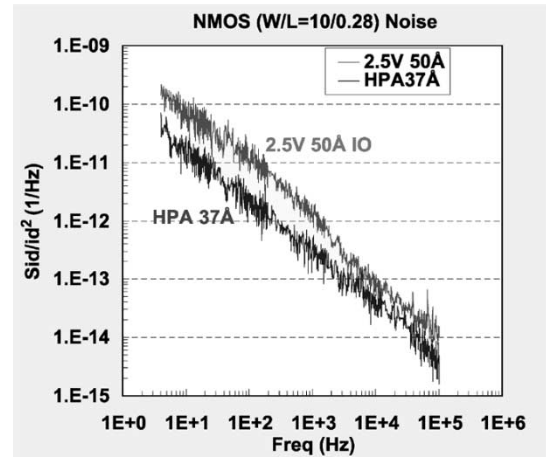
TABLE V
HPA 37-Å DEVICE MISMATCH AND THE COMPARISON WITH THE 50-Å I/O DEVICE

V_{DD}		2.5V				
Devices		HPA37A			50A IO	
		Std-V_T		Low-V_T	Std-V_T	
		NMOS	PMOS	NMOS	NMOS	PMOS
Avt_gm	x-couple	7.4104	3.9508	**5.8393**	9.24	5.99
(mV-um)	parallel	8.0283	3.913	**6.3593**	9.05	5.07
Aidsat	x-couple	0.5428	0.7259	**0.2982**	0.73	0.87
(%-um)	parallel	0.6039	0.71	**0.3753**	0.72	0.76
Abeta	x-couple	1.0744	0.8452	**0.8755**	1.27	1
(%-um)	parallel	0.81	0.6908	**0.8316**	1.24	0.85

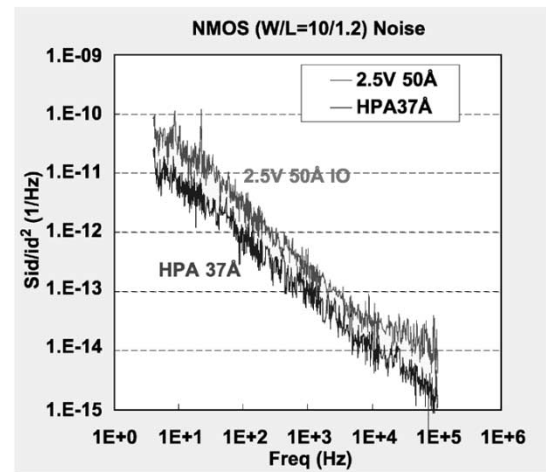
more stack layers were built (one layer to five layers), the better uniformity represented by tighter distribution with smaller standard deviation (3σ) can be achieved. The exact numbers calculated by Monte Carlo simulation are given by Table IV, in which the basic assumptions are the metal thickness variation of $\pm30\%$ and metal width variation of $\pm10\%$. The deviation of metal R_S by 3σ is maintained at a constant of around 32.9% for all structures with stack layer numbers of one to five, while the deviation of coupling capacitance is reduced by increasing the stack layer number from $3\sigma = 18.5\%$ for a single layer to $3\sigma = 8.1\%$ for five layers, which is more than 50% reduction. Monte Carlo simulation results suggest the advantage introduced by the multilayer stack structure like ID MoM in terms of promisingly good uniformity control over the coupling capacitance.

B. HPA Device Matching and Noise—Analog Applications' Concern

Besides the drivability and speed, matching and noise are two important factors to be verified for HPA devices. Table V illustrates mismatch in terms of $A_{\mathrm{vt-gm}}$, A_{idsat}, and A_{beta} representing the slopes of the standard deviation of V_T, I_{DSAT}, and β's mismatch versus $1/(WL)^{1/2}$. The advantages of HPA 37-Å devices featured by obviously less mismatch has been identified as comparable to the standard 50Å I/O, which is around 25%/50%, 35%/20%, and 53%/23% less in mismatch in terms of $A_{\mathrm{vt-gm}}$, A_{idsat}, and A_{beta}. It is noted that low-V_T nMOS as one of device offerings required for read-channel provides further reduction of mismatch, which is expected by dopant fluctuation theory. Regarding the benchmark on noise performance shown in Fig. 5, HPA 37-Å devices reveal around one order lower noise spectrum level than 50-Å I/O for a nominal device with mask length of $0.28\ \mu\mathrm{m}(L_{\mathrm{MASK}} = 0.28\ \mu\mathrm{m})$ and around half an order lower for a longer device with a mask length of $1.2\ \mu\mathrm{m}(L_{\mathrm{MASK}} = 1.2\ \mu\mathrm{m})$ in the frequency range of 4–100 kHz. The lower noise presented by HPA devices suggests a better oxide–Si interface achieved by the unique dual-gate oxide module and will be supported by better TDDB and HCI lifetimes in the following section. Regarding the substrate noise



(a)



(b)

Fig. 5. HPA 37-Å nMOS noise spectrum and comparison to the 50-Å 2.5-V I/O. (a) $L_{\mathrm{MASK}} = 0.28\ \mu$m. (b) $L_{\mathrm{MASK}} = 1.2\ \mu$m.

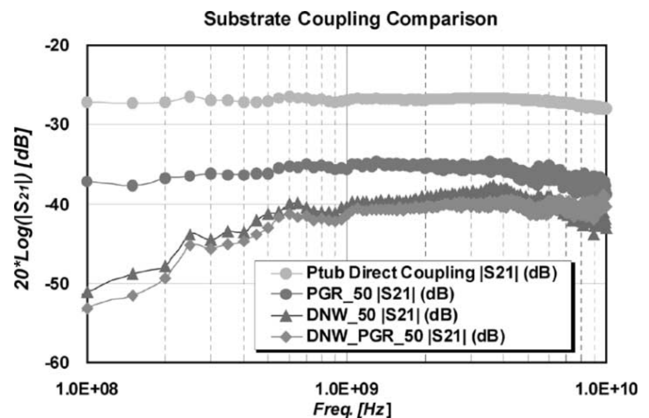


Fig. 6. P^+ guard ring, deep N-well, and both combination effect on substrate coupling noise measured by S_{21}.

isolation as a critical technique for MS and RF chips by using Si technology [7], [8], triple well shown in Table III is introduced to improve the noise isolation capability. Three kinds of isolation methods have been implemented as shown in Fig. 6, wherein P^+ guard ring, deep N-well, and both in combination are used. Conventionally, the *S*-parameter S_{21} is used as the in-

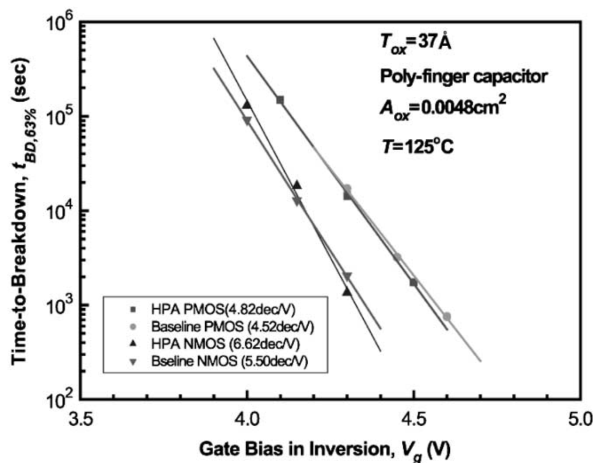


Fig. 7. Gate oxide medium-time-to-breakdown $\tau_{\mathrm{BD},63\%}$ measured from HPA 37-Å n/pMOS and the comparison to standard I/O 37-Å n/pMOS.

TABLE VI
ANALOG/I/O 37-Å OXIDE TDDB: HPA 37-Å AND THE COMPARISON WITH STANDARD I/O 37-Å OXIDE

Device Type	Oxide Recipe	γ	slope (dec/v)	$\tau_{0.1\%}$ (yrs)	$\tau_{0.01\%}$ (yrs)
NMOS@PW	HPA 37A	15.24	6.62	90.3	10.8
	Regular 37A	12.68	5.5	29.5	6.4
PMOS@NW	HPA 37A	11.1	4.82	48.7	13
	Regular 37A	10.4	4.52	11.1	2.7

dicator to quantify the isolation capability. We see from Fig. 6 that the use of a P$^+$ guard ring can improve isolation by around 10 dB over all frequencies from 0.1–10 GHz, and the use of deep N-well by MeV implant offers even better isolation particularly at lower frequencies, which is more than 20 dB below 1 GHz and around 15 dB above 1 GHz.

III. HPA AND CORE DEVICE RELIABILITY

It is recognized that reliability is actually the major challenge to HPA and logic core devices adopting the aggressively scaled oxide subject to operation under overdrive. In this paper, an extensive reliability test has been done, and quite promising results will be demonstrated in this section.

A. TDDB for 2.5-V HPA and 1.2-V Core Devices

Fig. 7 illustrates the medium time-to-breakdown ($T_{\mathrm{BD},63\%}$) measured from the 2.5-V n/pMOS capacitors with polygate finger type and source/drain tied together and the total gate oxide area of 0.0048 cm^2. The TDDB test has been done by stress voltages specified in the range of 4–4.65 V and acceleration by high temperature at 125 °C. The results from HPA 37-Å and standard 37-Å I/O devices are put together in Fig. 7 for rigorous and fair comparison. We see that even a subtle difference at the slope of $T_{\mathrm{BD},63\%}$ versus gate bias will lead to obvious deviation at $\tau_{0.1\%}$, i.e., the 0.1% lifetime extracted by extrapolation to 0.1% cumulative failure. Table VI shows that 37-Å oxide working under overdrive at 2.75 V can successfully pass TDDB with $\tau_{0.1\%}$ (0.1% lifetimes) as long as 90.3/48.7 years for HPA n/pMOS devices respectively, i.e., around 8/4

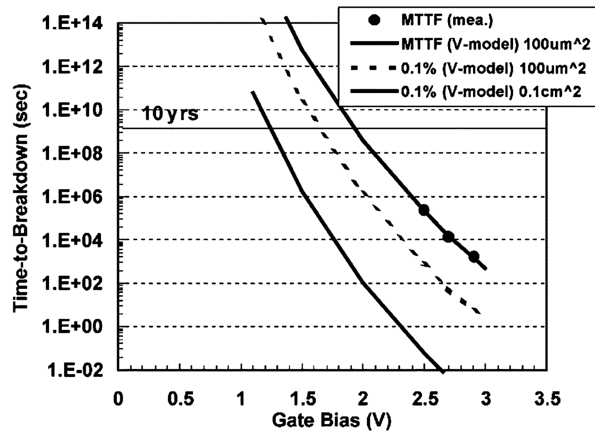


Fig. 8. Core 17-Å pMOS TDDB lifetimes versus gate bias and the comparison of MTTF and $\tau_{0.1\%}$ (0.1% lifetime).

TABLE VII
LOGIC CORE 17-Å pMOS TDDB LIFETIME AT 0.1 cm^2, 125 °C, CALCULATED BY POWER LAW FOR GATE BIASES OF 1.1 V, 1.2 V, AND 1.26 V

C013LV 17Å PMOS TDDB Lifetime@0.1cm^2, 125°C (yrs)		
Acceleration Model	Power Law Model	
Failure spec.	0.10%	0.01%
1.1V	1820	275
1.2V	97.7	14.8
1.26V	19	2.88

times higher than the generally accepted specification, i.e., ten years associated with dc operation. However, the margin is obviously degraded for standard I/O oxide to around two times for nMOS, but nearly zero for pMOS. As for 17-Å core devices under overdrive at 1.2 V, pMOS TDDB turns out a tougher issue, and the better oxide/Si interface offered by the 37-Å oxide recipe in this paper does help on core 17-Å TDDB and assure the pass under overdrive at 1.2 V+5% proven by Fig. 8 We would like to call attention to the important information shown in Fig. 8 in which lifetimes subject to three different definitions are drawn for comparison to reveal three scaling factors in terms of area, bias, and cumulative failure rate. Table VII summarizes the core 17-Å pMOS TDDB lifetimes (area $=$ 0.1 cm^2, temp $=$ 125 °C) under three different gate biases (1.1, 1.2, and 1.26 V $=$ 1.2 V $+$ 5%) and two different failure rate criteria (0.1% as standard specification , while 0.01% as a specially rigorous specification for reference only). We see that this core 17-Å pMOS fabricated by the HPA dual-gate oxide module can sustain gate overdrive up to 1.26 V with $\tau_{0.1\%}$ (failure rate $= 0.1\%$) maintained higher than ten years, i.e., the standard specification, but the gate overdrive will be limited by 1.2 V for the specially rigorous specification, i.e., $\tau_{0.01\%}$

B. NBTI for HPA pMOS Devices

PMOS NBTI is another critical reliability factor for analog circuit applications and a particular concern comes out due to possible tradeoff between NBTI and TDDB performance. Stress voltage and temperature conditions are two key parameters governing NBTI lifetimes in terms of mean-time-to-failure (MTTF) represented by the medium of the statistical distribution and

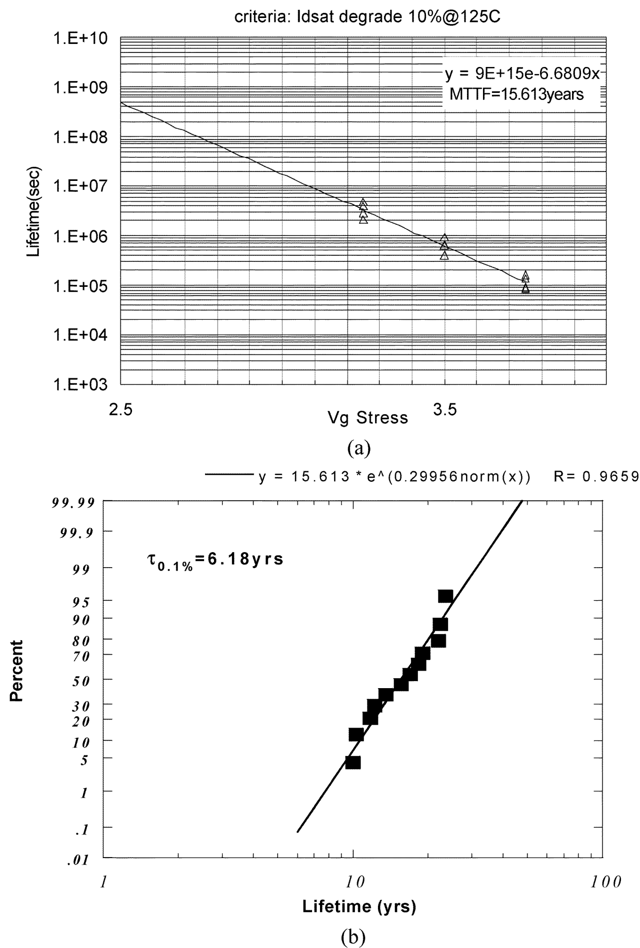


Fig. 9. (a) HPA 37-Å pMOS NBTI lifetimes defined by 10% $I_{\rm DSAT}$ degradation subject to gate stress biases of 3.25, 3.5, and 3.75 V. (b) HPA 37-Å pMOS NBTI lifetime cumulative plot in which $\tau_{0.1\%}$ corresponding to 0.1% failure is as long as 6.18 years.

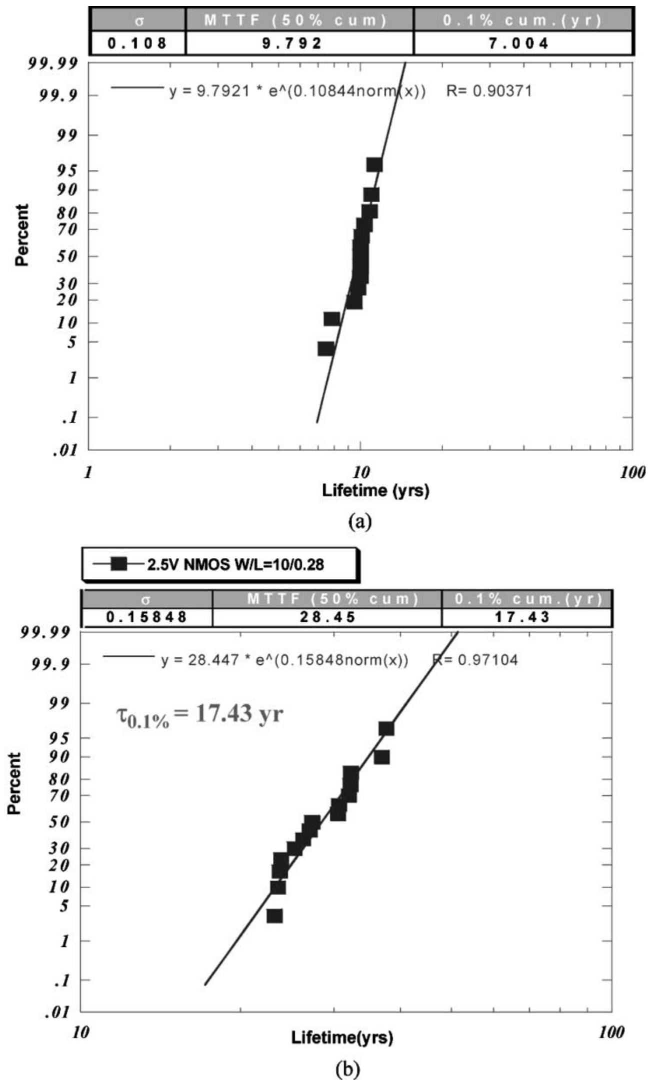


Fig. 10. (a) HPA 37-Å STD-V_T nMOS HCI lifetime cumulative plot in which $\tau_{0.1\%}$ corresponding to 0.1% failure is as long as seven years. (b) HPA 37-Å low-V_T nMOS HCI lifetime cumulative plot in which $\tau_{0.1\%}$ corresponding to 0.1% failure is as long as 17.43 years.

0.1% lifetime by extrapolation to 0.1% cumulative failure. In this paper, electrical stress has been performed with gate bias at 3.25, 3.5, and 3.75 V and thermal acceleration has been done by 125 °C. Fig. 9(a) indicates the lifetimes defined by 10% $I_{\rm DSAT}$ degradation subject to the mentioned gate biases (i.e., 3.25, 3.5, 3.75 V) and thermal acceleration under 125 °C. The good linearity exhibited in Fig. 9(a) validates the power-law model proposed for the pMOS NBTI lifetime, and the cumulative plot shown in Fig. 9(b) is used to extract the 0.1% lifetime noted by $\tau_{0.1\%}$. We see that NBTI lifetime as long as 6.18 years can be achieved corresponding to superior TDDB lifetime of 48.7 years. The experiment suggests that HPA 37-Å oxide can meet the TDDB ($\tau_{0.1\%}$@0.1 cm^2, 125 °C $>$ 10 years) and NBTI ($\tau_{0.1\%}$@125 °C $>$ 5 years) criteria simultaneously.

C. HCI for HPA nMOS

In this paper, two kinds of HPA nMOS devices have been developed for 2.5-V analog circuit applications. One is the STD-V_T nMOS (standard V_T), and the other is the low-V_T nMOS. The V_T target for nMOS is 0.5 V by $G_{\rm m,max}$ (maximum transconductance extrapolation method), while the target for low-V_T nMOS is quite low, nominal value at 0.08 V and allowing deviation of $3\sigma = 0.08$ V. Attributed to quite low channel doping (boron) concentration associated with the low-V_T nMOS, better matching has been demonstrated in the previous section, and longer HCI lifetime is expected. Fig. 10(a) illustrates the cumulative failure plot for STD-V_T nMOS in which a 0.1% lifetime extracted corresponding to 2.5 V and room temperature ($\tau_{0.1\%}$@2.5 V, 25 °C) by $1/V_{\rm DD}$ model (time-to-failure α $\exp^{(\beta/{\rm VDD})}$) can achieve seven years, which is more than one order better than the dc HCI lifetime specification of 0.4 yeasr. The dc lifetime of 0.4 years is equivalent to ac lifetime of ten years for the analog circuits in which a duty cycle of 25 is assumed. It is noted that the dc lifetime specification of 0.4 years is two times the general specification of 0.2 yearsm and such kind of rigorous specification comes from the special request of analog circuit design. As for low-V_T nMOS, the HCI lifetime turns out to be obviously better than that of STD-V_T nMOS, which around 17.4 years as shown in Fig. 10(b), i.e., more than double that of STD-V_T nMOS. The results match our expectation, and we attribute the superior HCI lifetime to two major factors. One

is the better oxide/Si interface, and the other is the reduced channel doping concentration.

IV. Conclusion

Manufacturable logic-based HPA process has been developed for high-end read-channel integrated circuits. The excellent performance in terms of speed, matching, and noise has been demonstrated and promisingly good reliability has been maintained simultaneously.

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Jyh Chyurn Guo was born in Taiwan, R.O.C. in 1960. She received the B.S.E.E. and M.S.E.E degrees from the National Tsing-Hua University (NTHU), Hsinchu, Taiwan, in 1982 and 1984, respectively, and the Ph.D. degree in electronics engineering from the National Chiao-Tung University (NCTU), Hsinchu, in 1994. The subject of her Ph.D. dissertation was "A new parameter extraction technique and modeling for miniaturized MOSFETs."

She joined NCTU's electronics engineering faculty in 2003, and before that she has been working in the semiconductor industry with a focus on device design and VLSI technology development. In 1984, she joined the Electronics Research and Service Organization/Industrial Technology Research Institute (ERSO/ITRI), where she was engaged in diversified semiconductor integrated circuit technologies. From 1984 to 1990, she was with the high-voltage bipolar/CMOS/DMOS integrated circuit project and responsible for high-voltage and power device simulation and design. Since 1991, she had been with the submicrometer project in ERSO/ITRI and working on the process simulation and device design for high-speed SRAM technology. From 1994 to 1998, she was with Macronix International Corporation where she was engaged in the high-density and low-power Flash memory technology development and led a team responsible for Flash memory device design and reliability analysis. In 1998, she joined Vanguard International Semiconductor Corporation, where she served as a Department Manager responsible for advanced DRAM device design with a major focus on 0.18–μm 64-M DRAM development. In 2000, she joined Taiwan Semiconductor Manufacturing Company, where she served as a Program Manager in charge of 0.1-μm logic CMOS FEOL technology development. Since 2001, she has been engaged in HPA and RF CMOS technology development, and led a team focusing on 0.13–μm CMOS-based mixed-signal and RF device design. She has authored or coauthored around 30 technical papers and has been granted about ten international patents in her professional field. Her current research interests are RF CMOS and HPA device design and modeling, novel nonvolatile memory technology, and circuit technology for SoC.

W. Y. Lien was born in Taiwan, R.O.C., in 1963. He received the Ph.D. degree in power mechanical engineering from National Tsing-Hua University, Hsinchu, Taiwan, in 1995.

He joined the Logic Technology Division, Taiwan Semiconductor Manufacturing Company Ltd., Hsinchu, in 1995. He has done extensive research in DRAM, mixed signal and RF processes of CMOS technology, and 3-D electromagnetic simulation on RF passive components.

T. L. Tsai received the M.S. and Ph.D. degrees in materials science and engineering from Cornell University, Ithaca, NY, in 1992 and 1996, respectively.

From 1996 to 2000, he was a Senior Staff Engineer with the Semiconductor Product Sector, Motorola. In 2000, he joined Taiwan Semiconductor Manufacturing Company Ltd., Hsinchu, Taiwan, R.O.C., and is currently a Technical Manager.

S. M. Chen received the B.S. and M.S. degrees in electronics engineering from National Cheng Kung University (NCKU), Tainan, Taiwan, R.O.C., in 2000 and 2002, respectively.

His recent research work is in the field of RF devices.

C. M. Wu received the B.S. degree in electron physics, the M.S. degree in electronic engineering, both from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., and the Ph.D. degree in electrical engineering from Columbia University, New York, NY in 1972, 1976, and 1979, respectively.

After a two-year postdoctoral research stint at Columbia University, he joined the Microelectronic Center, Xerox, CA, in 1981 as a Technical Staff Member on MOS devices. He joined Sharp Microelectronic Center in 1985 as Device Engineering Manager in charge of SPICE modeling, test vehicle design and SRAM cell development, and program management. He joined Taiwan Semiconductor Manufacturing Company Ltd., Hsinchu, in 1995, where he is currently serving as a Senior Program Director in research and development. His research interest is in SoC foundry process definition and knowledge management.