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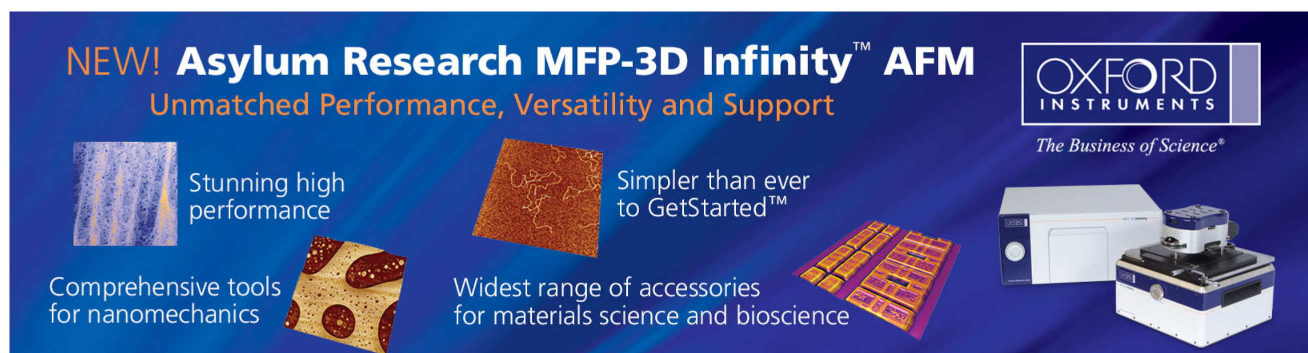

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A distributed charge storage with GeO_2 nanodots

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In this study, a distributed charge storage with GeO_2 nanodots is demonstrated. The mean size and aerial density of the nanodots embedded in SiO_2 are estimated to be about 5.5 nm and $4.3 \times 10^{11}\ cm^{-2}$, respectively. The composition of the dots is also confirmed to be GeO_2 by x-ray absorption near-edge structure analyses. A significant memory effect is observed through the electrical measurements. Under the low voltage operation of 5 V, the memory window is estimated to ~ 0.45 V. Also, a physical model is proposed to demonstrate the charge storage effect through the interfacial traps of GeO_2 nanodots. © *2004 American Institute of Physics.*
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Due to the high cost, large volume, and high power consumption of the magnetic-core memory, the electronic industries urgently needed a new kind of memory device to replace the magnetic-core memory in the 1960s. In 1967, Kahng and Sze invented the first floating-gate (FG) nonvolatile semiconductor memory at Bell Labs.[1] To date, the stacked-gate FG device structure continues to be the most prevailing nonvolatile-memory implementation, and is widely used in both standalone and embedded memories. The invention of FG memory impacts more than the replacement of magnetic-core memory, and creates an era of portable electronic systems. The most widespread memory array organization is the so-called flash memory, which has a byte-selectable write operation combined with a sector "flash" erase.

Although a huge commercial success, conventional FG devices have their limitations. The most prominent one is the limited potential for continued scaling of the device structure. This scaling limitation stems from the extreme requirement put on the tunnel oxide layer. On the one hand, the tunnel oxide has to allow quick and efficient charge transfer to and from the FG. On the other hand, the tunnel oxide needs to provide superior isolation under retention and disturbed conditions in order to maintain information integrity over periods of up to a decade. When the tunnel oxide is thinner for the first consideration, the retention characteristics may be degraded. And when the tunnel oxide is made thicker to take the isolation into account, the speed of the operation will be slower. There is, therefore, a tradeoff between speed and reliability and the thickness of the tunnel oxide is compromised to about 8–11 nm, which is barely reduced over more than five successive generations of the industry.[2] To overcome the scaling limits of the conventional FG structure, two candidates are mostly mentioned, SONOS[3–5] and nanocrystal nonvolatile memory devices.[6–8] As for SONOS, the nitride layer is used as the charge-trapping insulator. The intrinsic distributed storage takes an advantage of the SONOS device over the FG device, its improved endurance, since a single defect will not cause the discharge of the memory.[5] Tiwari *et al.*[6] for the first time demonstrated the Si nanocrystal floating gate memory device in the early 1990s. Also, the nanocrystal memory device can maintain good retention characteristics when tunnel oxide is thinner and lower the power consumption.[6–8] In this contribution, a GeO_2 nano-dot memory device with 4.5-nm-thick tunnel oxide and a low operating voltage of 5 V is proposed. Insulating nano-dots are utilized as the storage elements rather than the semiconducting counterparts. The concepts of SONOS and nanocrystal memories are combined and explored. A significant memory effect due to the charge trapping in the GeO_2 dots is observed.

First, the 6 in. Si wafer was cleaned with standard RCA recipes, followed by a thermal oxidation process to form 4.5-nm-thick dry SiO_2 layer as a tunnel oxide in an atmospheric pressure chemical vapor deposition (APCVD) furnace. Right after the growth of tunnel oxide, poly-$Si_{0.8}Ge_{0.2}$ was formed on the oxide immediately by low pressure chemical vapor deposition. The deposition of $Si_{0.8}Ge_{0.2}$ was kept at 550 °C and the pressure was controlled to be 460

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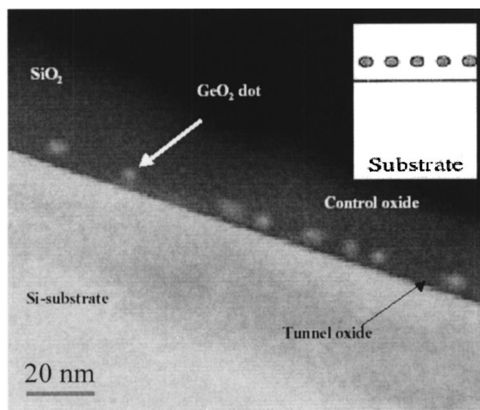

FIG. 1. The cross-sectional TEM micrograph of an oxide/GeO_2 nano-dots/oxide stacked structure.

mTorr. The flow rate of the reaction gas of SiH_4 and GeH_4 was 60 and 8 sccm, respectively, and the Ge fraction was analyzed to be around 0.2 by Auger electron spectroscopy. Subsequently, the $Si_{0.8}Ge_{0.2}$ layer was oxidized in an APCVD reactor at 950 °C and the Ge atoms would be segregated downward until they reach the tunnel oxide surface.[9–11] The Ge dots grew based on the Ostwald ripening mechanism,[12] in which the larger dots grew at the expense of the smaller dots. After the Si elements of the $Si_{1-x}Ge_x$ layer are completely oxidized, the Ge nanocrystals tend to be oxidized into GeO_2 nano-dots as the oxidation process is not ceased. From the analysis of transmission electron microscopy (TEM), the control oxide capped on the GeO_2 nano-dots was estimated to be about 40 nm and the GeO_2 nano-dots were confirmed via x-ray absorption near-edge structure (XANES). Finally, the Al electrode was patterned and sintered. Electrical measurements were performed on the metal-insulator-semiconductor structures with GeO_2 nano-dots embedded between tunnel and control oxide.

A cross-sectional TEM micrograph of an oxide/GeO_2 nano-dots/oxide stacked structure is shown in Fig. 1. It is clearly observed the GeO_2 nano-dots are embedded between the tunnel oxide and control oxide, oxidized from the $Si_{1-x}Ge_x$ layer, and are separated from each other. The inset schematically shows the gate stack arrangement in this study. The mean size and aerial density of the dots are estimated to be about 5.5 nm and 4.3×10^{11} cm^{-2}, respectively, by TEM.

To confirm the existence of the composition of the GeO_2 nano-dots, x-ray absorption near-edge structure (XANES) is performed.[13–15] In XANES, a core electron is excited to higher bound or quasibound states, which contain information about coordination geometry and electronic aspects of the absorbing atom. Among most of the XANES studies, the standard materials with known valence are utilized as references, and compared with the unknown samples. Therefore, the measurements are frequently qualitatively analyzed, not quantitatively. In this work, we used Ge powder, GeO_2 powder, and $Si_{0.8}Ge_{0.2}$ epitaxial layer on Si as the standard materials and our investigated sample with nano-dots observed as the unknown sample. The x-ray source is extracted from the National Synchrotron Radiation Research Center. As shown in Fig. 2, the shift of absorption edge (roughly the center of the intensity jump) is an index of the Ge oxidation state. The obvious edge shift from the Ge edge and the high

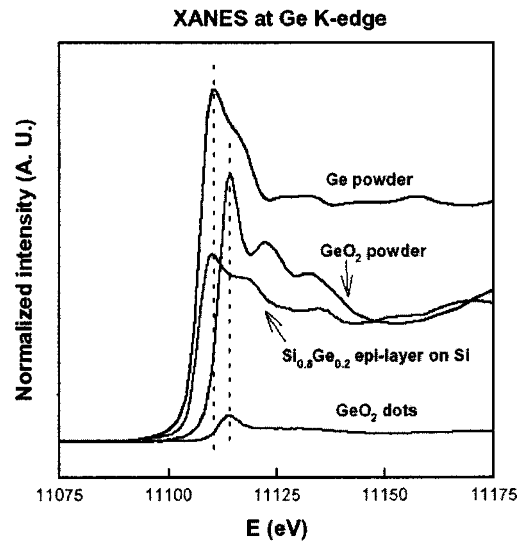

FIG. 2. The XANES spectra of the investigated sample and standard samples.

degree of similarity between the XANES results of the sample with nano-dots and GeO_2 standard reveal that Ge is oxidized. Its oxidation state is very close to GeO_2.

Figure 3 shows the capacitance–voltage ($C-V$) hysteresis after the bidirectional bias sweeps between 5 V and (-5) V. It is found that a low operating voltage, 5 V, causes a significant threshold-voltage shift up to ~0.45 V, which is sufficient to be defined as "1" or "0" for the logic-circuit design. It is worth noting that the hysteresis is counterclockwise, which is due to substrate injection from the electrons of the deep inversion layer and holes of the deep accumulation layer of the Si substrate.[16]

Figure 4 demonstrates the band diagrams of the operation of the distributed charge storage with GeO_2 nano-dots. The "write" and "erase" operation with different gate polarities of the memory device are exhibited. When the device is written or programmed, the electrons directly tunnel from the Si substrate through the tunnel oxide, and are trapped in the GeO_2 nano-dots. When the device is erased, the electrons may tunnel back to the deep accumulation layer of Si substrate. The control oxide is utilized to prevent the

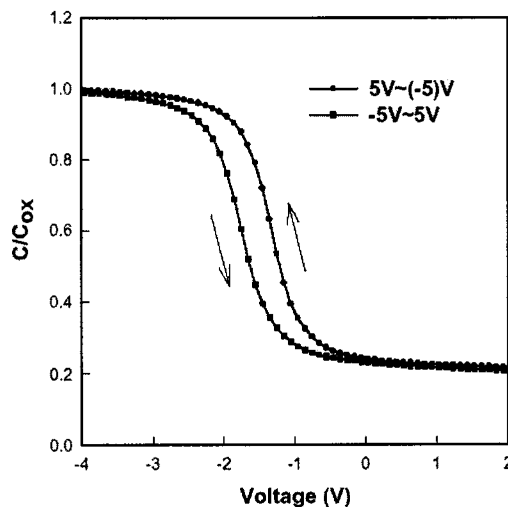

FIG. 3. The capacitance–voltage hysteresis after the bidirectional bias sweeps between 5 and (-5) V.

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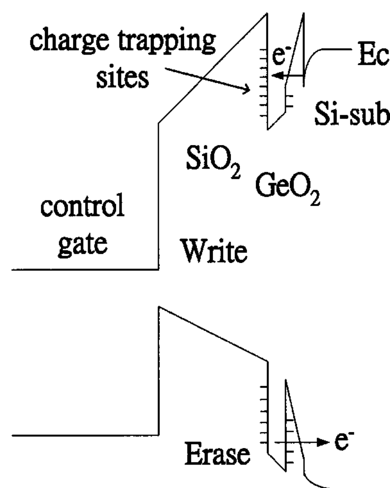

FIG. 4. The band diagrams of the operation of the distributed charge storage with GeO_2 nano-dots.

carriers of gate electrode from injecting into the GeO_2 nano-dots by Fowler–Nordheim tunneling. It is believed that during the oxidation process of the Ge nanocrystals into GeO_2 nano-dots, there are defects or traps created in the interfaces between GeO_2 dots and tunnel and control oxide. When the device is under programming, the injected electrons will be captured in the interfacial traps of the GeO_2 dots and contribute to a threshold voltage shift (memory window). It is concerned about whether the storage of GeO_2 nano-dots is as reliable as other insulating thin films. The reliability issues such as endurance and retention of the memory device should be taken into account and are currently under investigation.

In summary, a distributed charge storage with GeO_2 nano-dots is shown. The mean size and aerial density of the dots are estimated to be about 5.5 nm and 4.3×10^{11} cm^{-2}, respectively. The composition of the GeO_2 dots is confirmed by the XANES measurements. In electrical analyses, a significant memory effect is observed with a threshold voltage shift of 0.45 V under 5 V operation. Also, a physical model is proposed to explain the charge storage via the interfacial traps of GeO_2 nano-dots. Further works about the research on the reliability issues are currently under investigation.

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