Briefs

Efficient Improvement of Hot Carrier-Induced Degradation for 0.1-μm Indium-Halo nMOSFET

Wen-Kuan Yeh and Jung-Chun Lin

***Abstract*—The effect of post-thermal annealing after indium-halo implantation on the reliability of sub-0.1-μm nMOSFETs was investigated. We found that the control of annealing time is more efficient than that of annealing temperature with respect to improving the hot carrier-induced device degradation. The best results of device performance were obtained with post-annealing treatment performed at medium temperatures (e.g., 900 °C) for a longer time.**

***Index Terms*—Hot carrier-induced device degradation, indium halo (In-halo), post-thermal annealing (PA).**

I. Introduction

The reduction of threshold voltage ($V_{\rm th}$) with decreasing channel length is widely used as an indicator of the short-channel effect (SCE) in evaluating CMOS technologies [1]. As MOSFETs are scaled down to 0.1 μm and below, this adverse $V_{\rm th}$ roll-off effect becomes one of the major limitations for deep-submicrometer device performance. Thus, a means to suppress the SCE with low $V_{\rm th}$ is a key issue for sub-0.1-μm MOSFETs because this is essential to the manufacturability of low-power systems [2]. Engineering channel dopant profiles obtained by localized halo implantation have been extensively used in deep-submicron CMOS technologies and have become indispensable for sub-0.1-μm CMOSFETs [3], [4]. Owing to low diffusion constant, indium (In) has been successfully used in fabricating abrupt and shallow halo profiles for deep-submicron nMOSFETs [5]. Unfortunately, interstitial Si caused by the In ion implantation results in the increase of leakage current, and the degradation of device performance [6], [7]. Thus, post-thermal annealing (PA) treatments after In-halo implantation are proposed to solve these problems. In this brief, the effect of PA on the hot carrier effect was investigated for the 0.1-μm devices with respect to B-halo and In-halo nMOSFET. This intriguing findingshows that a device's subthreshold characteristic, as well as hot carrier-induced device degradation, can be improved by PA at a lower temperature with long-time annealing without degrading a device's performance.

II. Experiments

A sub-0.1-μm CMOSFET was fabricated with 2-nm nitride gate oxide using dual–gate twin-well process. After poly-Si gate formation, arsenic (at 2–5 KeV, 1–3 $\times 10^{14}$ cm^{-2}) ion implantation was used to form n^+ source/drain extension. The halo structures were obtained using boron (at 15–20 KeV, 2×10^{13} cm^{-2}) and indium (at 120–180 KeV, 2×10^{13} cm^{-2}) implantations with a 20 ° tilted angle in respectively. After extension and In-halo implantation, various PAs were employed using a rapid thermal process (at 900–1050 °C). Then arsenic (at 40–60 KeV, 3–5 $\times 10^{14}$ cm^{-2}) ion implantation followed by annealing at 1000 °C were employed to form n^+ deep source/drain junction. Finally, wafers were processed through a $CoSi_2$ salicidation process and a standard backend flow to completion. To investigate the hot-carrier-effect (HCE) of transistor, device stressing and measurements were made on a probe station at various drain voltages (V_D = 1.2–2.0 V) and gate voltages (V_G = 0–1.8 V) with a stressing time ranging from 0 to100 min.

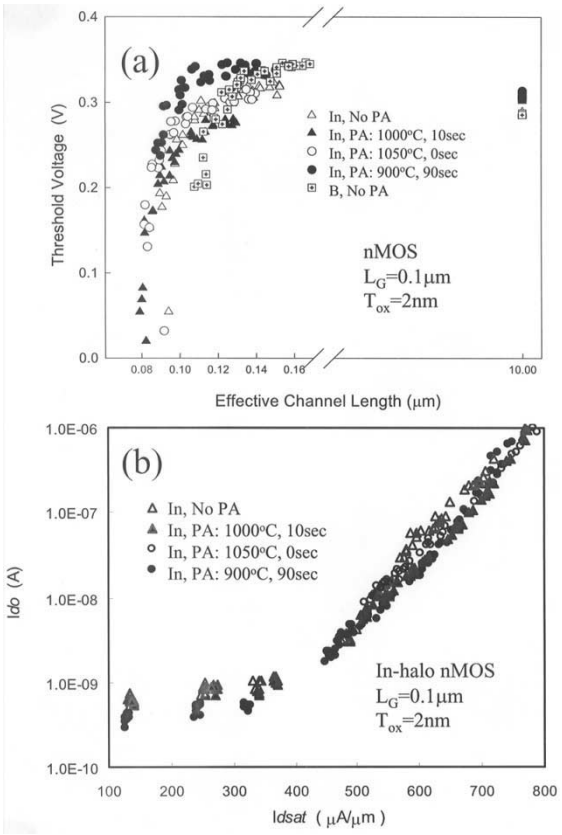

Fig. 1. (a) $V_{\rm th}$ roll-off characteristics as a function of effective channel length. (b) $I_{\rm dsat}$ versus $I_{\rm do}$ for nMOSFET with different PA.

III. Result and Discussion

As shown in a previous study [8], in comparison with B-halo structure, the margin of a device's punchthrough can be improved with In-halo structure because of the localized junction profile. Thus, In-halo is able to suppress the nMOSFETs subthreshold slope "collapse" down to sub-0.1-μm channel length, as shown in Fig. 1(a). Since a large amount of Si interstitial, which is generated by As-extension implantation and enhanced by In-halo implantation, can react with In dopant more efficiently, resulting in a more pronounced deactivation, and causing an accelerated $V_{\rm th}$ rolloff for short-channel devices [9]. Thus, PA was proposed to remove these Si interstitial and suppress the transient enhanced diffusion (TED) phenomenon. However, the junction depth will increase after 1000 °C rapid thermal annealing (RTA) resulting in a device's $V_{\rm th}$ rolloff. In this brief,

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W.-K. Yeh is with the Department of Electrical Engineering, National University of Kaohsiung, Kaohsiung, Taiwan, R.O.C. (e-mail: wkyeh@nuk.edu.tw).

J.-C. Lin is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan, R.O.C.

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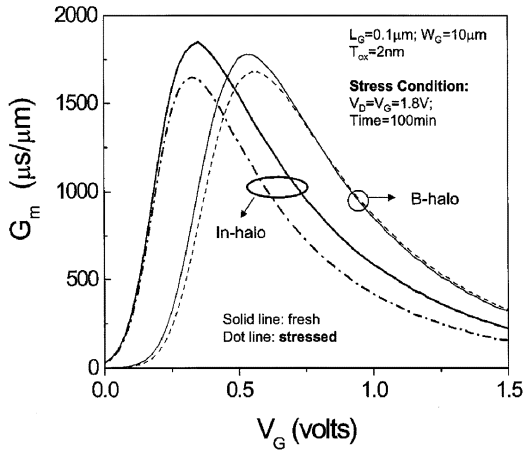

Fig. 2. Transconductance (G_m) as a function of gate voltage (V_G) for B-halo and In-implanted halo nMOSFET before and after hot carrier stress.

higher saturated $V_{\rm th}$ and apparent reversed chort-channel-effect (RSCE) happened on In-halo nMOSFET using 900 °C with 90 s annealing, improving the In-halo device,s SCE. It is believed that the Si interstitial can be removed by using a medium-temperature annealing for an appropriate longer time without degrading the device's SCE. With this thermal treatment, a device's $I_{\rm do}$ can be reduced even at sub-0.1-μm channel length, as shown in Fig. 1(b). Owing to a low diffusion constant [10], the In-halo sample forms an abrupt and shallow extension/halo profile improving the device SCE even at sub-0.1 μm channel length. Although the localized In-halo dopant located only around extension junction without degrading the devices driving capacity [8], the hot carrier effect of In-halo device was still a problem, and became more serious as device dimension was decreased. In comparison with B-halo nMOSFET, the hot carrier-induced transconductance degradation of In-halo nMOSFET becomes more serious after hot carrier stress, especially at a higher gate voltage, as shown in Fig. 2. For In-halo nMOSFET, the abrupt and shallow junction profile increases drain junction electric field and enhances high impact-ionization rate of channel carrier, thus aggravates the hot-carrier effect. The subthreshold characteristic of B-halo as well as In-halo nMOSFETs before and after hot-carrier stress was shown in Fig. 3(a). B-halo device shows lesser junction leakage than In-halo device does. According to the results of Yu *et al.* [3], B-halo nMOSFET shows normal recombination–generation junction leakage happen, while a high localized dose of In-halo nMOSFET indicates that the drain-to-halo (body) band-to-band tunneling current starts to present. Owing to higher doping concentration of In around the edge of source/drain extension region with abrupt and shallow junction profile, the n^+ junction breakdown field was large apparently. Thus, the band-to-band tunneling leakage can be considerable contributor to the device's off-state leakage current $(I_{\rm do})$ resulting in higher device's $I_{\rm do}$ with In-halo structure. The swing degradation indicates the creation of interface traps resulting in a threshold voltage shift [10]. The gate-induced drain leakage (GIDL) in both nMOSFETs at a negative gate bias of $V_G = -0.5$ V was also increased. It has been reported that GIDL is a direct result of the generation of interface states [11]. Thus, the largest degradation in $I_{\rm Dsat}$ coincides with the largest increase in interface state density. In comparison with B-halo nMOSFET, the In-halo nMOSFET subthreshold characteristic shows larger $I_{\rm do}$ and GIDL. Although the substrate current may be a contribution on drain leakage, the amount of $I_{\rm sub}$ is lower than total drain leakage, as shown in the inset in Fig. 3(a). It is presumably that the GIDL is the possible dominate factor on drain leakage creation at negative gate voltage. Furthermore, both devices' subthreshold

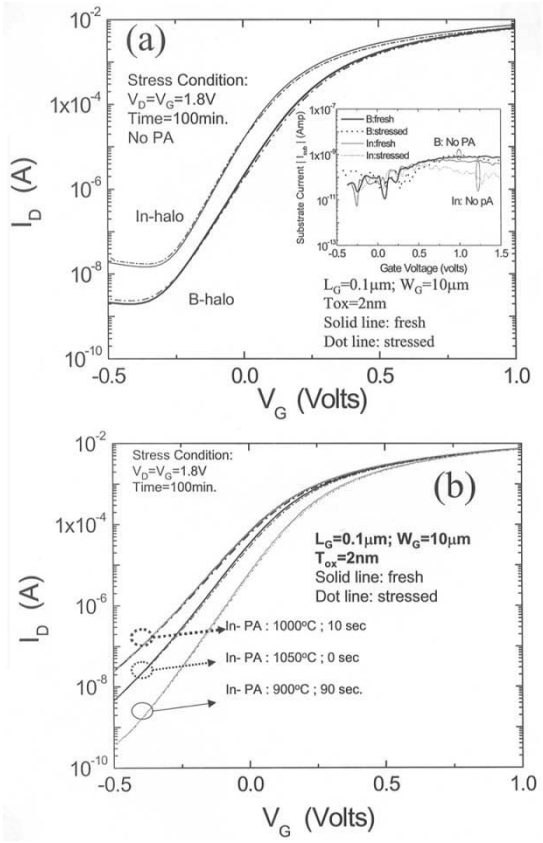

Fig. 3. Subthreshold characteristic for nMOSFET with B-implanted and In-implanted halo structures before and after hot carrier stress. (a) Without and (b) with PA. The insert in (a) shows $I_{\rm sub}$ versus V_G for both nMOSFETs before and after hot carrier stress.

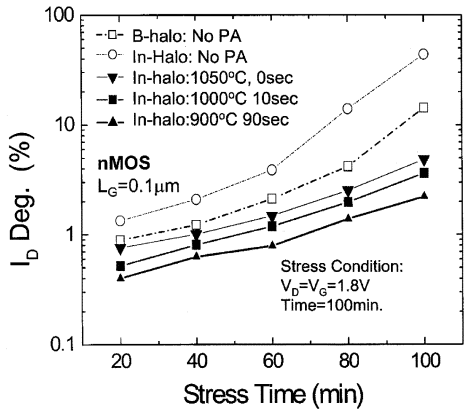

Fig. 4. Hot carrier-induced saturated drain current $(I_{\rm dsat})$ degradation versus stress time for nMOSFET with B-implanted and In-implanted halo structures under various post annealing.

characteristic was aggravated after hot carrier stress; thus the PA was necessary to improve these devicess characteristic. With appropriate PA, the In-halo devices subthreshold characteristic can be improved and GIDL can be suppressed apparently, as shown in Fig. 3(b). In this brief, the best device's subthreshold swing and lowest $I_{\rm do}$ were obtained at 900 °C with longer time annealing. Because the Si interstitial was removed efficiently with an appropriate PA, the subthreshold characteristic of In-halo nMOSFET can be improved without degrading the device's characteristics even at sub-0.1–μm channel length. The hot carrier-induced saturated drain current $(I_{\rm dsat})$ degradation of B-halo and In-halo nMOSFETs with various PA

treatments was shown in Fig. 4. According to the interstitial diffusion model [12], energies (E_a) to move dopant atoms from one interstitial site to another was required. Owing to the existence of Si interstitial caused by In ion bombardment, the E_a was reduced. Thus, the channel-carrier mobility and the channel-carrier impact-ionization rate was increased. In this brief, the hot carrier-induced $I_{\rm dsat}$ degradation of In-implanted nMOSFETs was more serious than that of B-implanted nMOSFETs. Although In diffusion was also increased after higher temperature annealing, the device's threshold voltage was not degraded especially at 900 °C annealing with longer time [Fig. 1(a)]. It is believed that the number of Si interstitial is the dominant factor in reducing the ion bombardment, and the Si interstitial and drain junction field can be reduced with a PA at 900 °C for a longer time. Thus, the $I_{\rm dsat}$ degradation of all In-implanted devices can be reduced with appropriate PA and lower than that of B-implanted devices. For In-halo nMOSFET, very low drain degradation ($<3\%$) can be obtained by PA at medium temperature with enough annealing time.

IV. Conclusion

In this brief, PA impact on devices characteristic as well as hot- carrier-induced reliability of In-halo structure was inspected. The Si interstitial caused by In-halo implantation can be removed by PA with enough annealing time. For In-halo nMOSFETs, hot carrier-induced device degradation can be improved by post annealing, especially at medium temperature with a long time annealing without degrading devices performance.

Acknowledgment

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Rate Equation of Current Degradation of the Spindt-Type Field Emitter Array

Chenggang Xie and Lawrence Dworsky

***Abstract*—The degradation rate of the emission current of the Spindt-type field emitter arrays in the display environment has been measured. The relative degradation rate is found to be a function of the square of emission current and proportional to the anode bias (voltage). A life model is presented that leads to development of an analytical rate equation of emission current degradation. Based on this model, there is a steady-state level at which the emission current is stable. The steady-state emission current depends on anode bias, background pressure in the package and cleanliness of anode and cathode surfaces. Experimental results are consistent with the rate equation derived from the model. Since the model does not include any material and process that make the cathode, it could probably apply to any field emission cathodes.**

***Index Terms*—Contamination, current degradation, electron emission, field emission display.**

I. Introduction

Inadequate display lifetime is one of the most critical problems slowing down the introduction of the field emission display (FED) into the commercial display market. For display applications, a time-independent current–voltage (*I–V*) relationship of the cathode is desired. In this work, we investigate the effect of operating conditions, such as anode bias, gate voltage, and current on the degradation of the Spindt-type field emitter arrays used in displays. A life model is proposed based on the assumption that the emission surface consists of high-emission and low-emission areas. An analytic rate equation of emission current degradation is derived from the model and is compared with the preliminary experimental results.

II. Experimental Setup

The field emission cathode used in this study is a Spindt-type field emitter array [1]. The tip material is molybdenum (Mo). Details of the emitter structure have been described elsewhere [2]. The display consists of a phosphor-coated anode facing the cathode and separated by 0.7 mm. The size of the displays used in the study is 2.5 in diagonal. The cathode contains about 11.5 million emitters. The displays are vacuum-sealed with bar-shape getters. The base pressure inside the displays is about 1×10^{-5} torr when the displays are turned off. An operating FED is itself actually an ion vacuum pump. When a display is first turned on, the pressure surges as accelerated electrons strike the anode and then falls below its original level as the ionized gasses accelerate toward and stick to the cathode. These displays are normally operated at an anode voltage of 3000 V. Typically, the displays are burnt in for 25 h before any data is taken. For life testing, emission current is monitored at all times at a fixed gate voltage. Fig. 1 is the life curve of a "dirty" FED at an anode voltage of 3000 V with 1-μA initial current per subpixel. The operating conditions, such as anode bias, emission current and gate voltage are varied to study their impact on the emission current degradation.

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C. Xie is with Motorola Labs, Motorola, Inc., Tempe, AZ 85284 USA (e-mail: cxie@motorola.com).

L. Dworsky, retired, was with Motorola Labs, Motorola, Inc., Tempe, AZ 85284 USA. He is now at 12780 E. Sahuaro Drive, Scottsdale, AZ 85259 USA.

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