The Understanding of Strain-Induced Device Degradation in Advanced MOSFETs with Process-Induced Strain Technology of 65nm Node and Beyond

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Abstract- In this paper, the origin of the strained-induced degradation in the MOSFETs with process-induced strain has been investigated by the I_D-RTN (Drain Current Random Telegraph Noise)technique. The process-induced strain on devices will make worse the device reliability, as reported in [1-2]. First, the I_D-RTN has been employed to study the reliability of two different types of strain devices, i.e., the CESL strain and SiC S/D strain on nMOSFETs. Both CESL and SiC S/D nMOSFETs exhibit poorer reliability compared to bulk devices. However, their impacts to the much worse degradation are different. Results demonstrated that, for the strain in CESL device, it introduced extra mobility scattering in the vertical direction, while in SiC S/D device, the tensile strain along the channel causes an increase of trap generation via the horizontal field only. The CESL process introduces an additional compressive strain vertical to the channel such that it shows much worse reliability than the SiC S/D ones.

Indexed terms: Random Telegraph Noise, Strained-silicon, MOSFET

Introduction- Recent developments [2] in CMOS have a consensus that uniaxial strain is easier to fabricate and also provide flexibility in designing n- and p-MOSFETs individually. Whatever the strain technology we used, the device exhibits much worse reliability comparing to conventional ones [3]. In seeking for solutions to enhance the device driving current, we need to consider a trade-off between reliability and current enhancement capability. Therefore, to understand the process-induced reliability becomes essential toward a better design of the devices. As noted in [2], the I_D-RTN technique provides a way to understand the device trapping behavior, which can be used to understand the physics mechanism underlying the origins of reliability.

In this paper, by applying I_D-RTN method on the strained n-MOSFET with different process-induced strains, we will be able to systematically explore the physics underlying the origins of the strain induced degradation. Then, the correlation between those different strains (physical strain) and the electrical reliability can be found.

1. Device Preparation

The devices were fabricated by the advanced 65 nm CMOS technology. Two sets of the devices have the same dimension (W/L=0.2/0.12μm). The first set is bulk-Si and strained n-MOSFET with nitride-cap layer with <100> channel on (100) substrate (CESL). The second set is bulk-Si and strained n-MOSFET with Si:C S/D with <100> channel on (100) substrate in Fig. 1. All the devices have 14 Å (physical thickness) gate oxide with SION process.

2. Results and Discussion

A. Basic Measurements of RTN

Because of the slow oxide trap, the carrier from source to the drain could be captured and emitted as shown in Fig. 2(a). Fig. 2 (b) shows the I_D-RTN waveform with three major parameters (capture time, τ_c, emission time, τ_e, and current amplitude ΔI_D[4]). First, measurement has been done and no process induced traps existing in the fresh devices. Then, the hot carrier stress was applied to the devices and produced the oxide traps which made two-level fluctuation of drain current in our stress condition. Fig. 3 shows the I_D-RTN spectra for the bulk nMOSFET, from which the RTN fluctuation was increased as gate bias increases. Also, for both bulk and CESL devices, τ_e and τ_c vary with different gate biases, which can be evaluated in a certain time period as shown in Fig. 4. The capture time, τ_c of the slow trap in the CESL is larger than the bulk, which implies that the trap is deeper in CESL than that in the bulk. While the magnitudes of emission time τ_e do not show much difference. Also, the trapping and de-trapping events happen more frequently in CESL so that the capture time over the emission time decreases more quickly in CESL than bulk Fig. 5(a). This also assures that the HC stress produces more damage in the Si/SiO_2 for the CESL and the trap's location is deeper in the CESL than the bulk, Fig. 5(b). The drain current fluctuation $\Delta I_D/I_D$ rolls-off because of the increasing of carrier concentration. Further, the variation of the RTN amplitude $\Delta I_D/I_D$ is proportional to the normalized conductance change g_m/I_D (i.e., $\Delta I_D/I_D \propto g_m/I_D$, Eq.(3) in Table 1) in the bulk device [6]; while the variation in CESL changes rapidly (Fig.6). The RTN is neither influenced by the change of carrier's number fluctuation ΔN_s nor by the mobility $\Delta \mu$ [4]. Here, the $\Delta I_D/I_D$ roll-off quickly in CESL reveals that there is carrier scattering induced. This becomes an additional mobility degradation factor of the CSEL device after the HC-stress.

B. RTN in the Strained CSEL and SiC S/D nMOSFETs

Similarly, experiments have been demonstrated on the SiC S/D nMOSFETs and its comparison with bulk ones, Fig. 7. The drain current degradation and the two-level I_D fluctuations are also observed in Figs. 8 and 9 respectively. The SiC S/D has larger impact ionization rate near the drain region and induces more current degradation than the bulk ones [7-8]. The capture and emission of electrons are examined for SiC and the bulk devices. They are about the same order for the electrons τ_c and τ_e. Both emission mechanisms are about the same for the two traps (Fig. 10). Fig. 10 shows the $\Delta I_D/I_D$ of the RTN amplitude which is proportional to the normalized conductance change for both devices. This implies that the slow oxide trap in SiC S/D follows the same mechanism to induce the two-level I_D fluctuation as that of bulk devices. However, in Fig. 11, $\Delta I_D/I_D$ is proportional to the normalized conductance change g_m/I_D for both devices, which means that SiC behaves differently from the CSEL devices.

C. The Origins of the Worse Reliability in Strained Devices

Fig. 12 shows the comparison of I_D degradation for devices before and after the HC-stress. The CESL device *shows larger drain current degradation* than the SiC ones, as a result of *an extra degradation factor*. Fig. 13 illustrates the strain direction for the CESL and SiC S/D respectively. For the CESL nMOSFET, the capping layer in the nMOSFET provides the tensile strain along the channel direction and also the compressive strain along the vertical direction. The SiC on S/D inducing the tensile strain along the channel region only. Under strong inversion, for comparable N_S, $\Delta I_D/I_D$ should be proportional to the mobility [9]. From Fig. 11, the $\Delta I_D/I_D$ roll-off more quickly in the CESL compared to the bulk nMOSFET while the SiC S/D and bulk nMOSFETs show comparable trend. Because the process induced extra vertical compressive strains in the dielectric (Fig. 13), the CESL gives rise to more scattering and degrade the Si/SiO2 interface quality after the HC stress; the SiC S/D device with the tensile strain along the channel induces an increase of trap generation via the horizontal field only. In short: (1) the strain techniques can enhance the device performance while on the contrary they show poor hot carrier reliabilities (2) the vertical strain which would cause more scattering can change the carrier mobility and may make worse the device reliability than the SiC S/D device ones.

In summary, the enhanced hot carrier degradation was found in uniaxial-strained devices. The correlation between physical strain and the electrical reliability has been proposed. It is believed that the SiC S/D provides a one-dimensional strain to the channel, while CSEL provides two-dimensional strains to the channel such that the latter one induces larger I_D degradation. This can be verified that the lateral degradation comes from the generated interface traps caused by the tensile strain, while the more enhanced degradation in CSEL comes from the extra compressive strain in the vertical direction.

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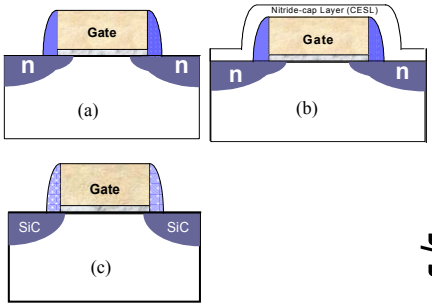

Fig. 1 The cross-sectional views of the experimental strained devices:.(a) Bulk n-MOSFET (b) CESL strained N-MOSFET (c) SiC S/D strained n-MOSFET.

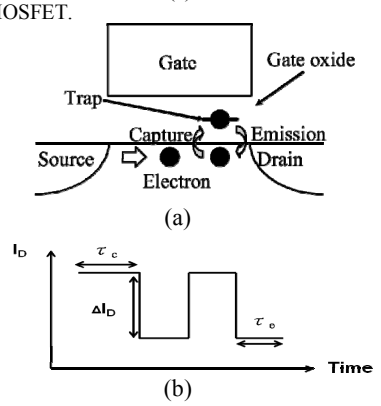

Fig. 2 (a) Carrier trapping and de-trapping by the slow oxide trap near the drain side. (b) Illustration of the three parameters of the RTN measurement: capture time, τ_c, emission time, τ_e, and the amplitude of current fluctuation ΔI_D.

$$\frac{d\ln\left\langle\frac{\tau_c}{\tau_e}\right\rangle}{dV_G}=-\frac{qZ_{eff}}{kT} \quad \text{Eq. (1) [4]}$$

$$\frac{\Delta I_D}{I_D}=-\frac{1}{W_{eff}\times L_{eff}}\left(\frac{1}{N_{eff}}\pm\alpha\mu\right) \quad \text{Eq. (2) [4]}$$

$$\frac{dI_D}{I_D}=\frac{g_m}{I_D}\frac{q}{W_{eff}L_{eff}C_{ox}}\left(1-\frac{x_T}{t_{ox}}\right) \quad \text{Eq. (3) [6]}$$

Table 1 Model equations used in this work.

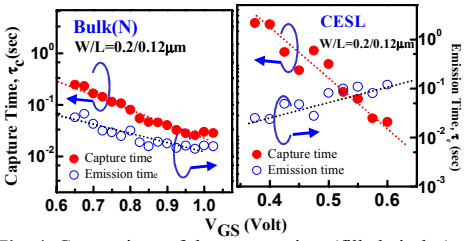

Fig. 4 Comparison of the capture time (filled circles) and emission time (open circles) for devices after the stress. (left) Bulk-Si, (right) CESL n-MOSFET.

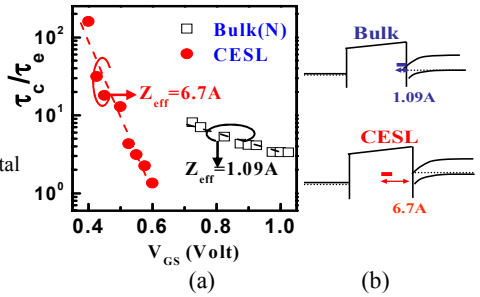

Fig. 5 nMOSFETs. (a) Plot of τ_c/τ_e versus gate voltage. (b) The effective depth location for the two traps.

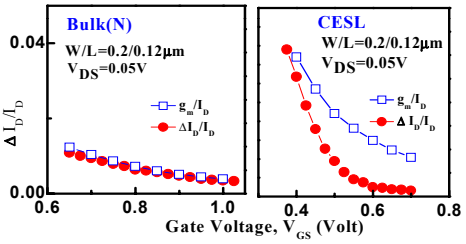

Fig. 6 Normalized RTN amplitude versus gate voltages. (left) Bulk-Si (right) CESL n-MOSFET. The open squares are the normalized conductance change g_m/I_D. Note that CSEL device shows a drastic change of the drain current fluctuation.

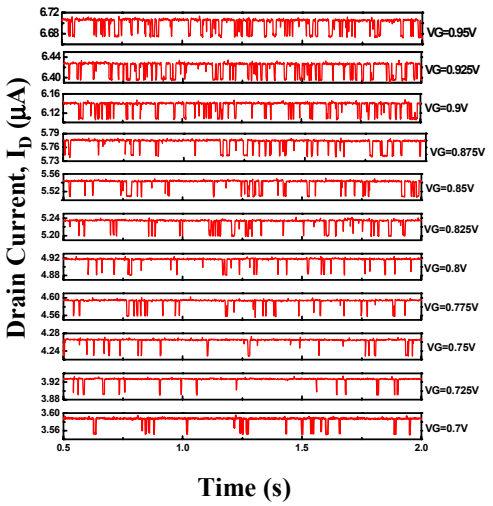

Fig. 3 Drain current waveforms of the Bulk-Si device at various gate biases..

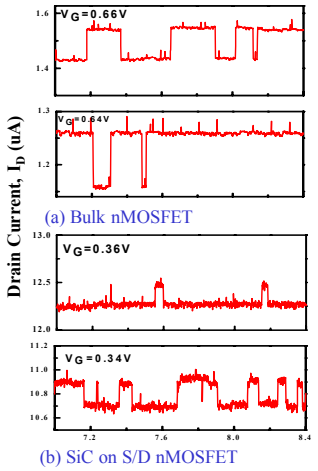

Fig. 7 Drain current waveforms: (a) Bulk-Si (b) SiC S/D n-MOSFET.

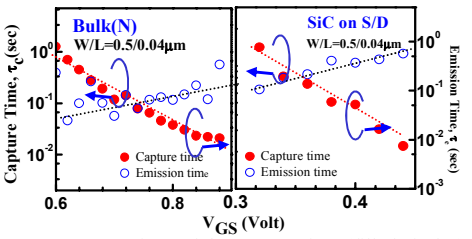

Fig. 8 Comparison of the capture time (filled circles) and emission time (open circles) for devices after the stress. (left) Bulk-Si (right) SiC S/D n-MOSFET.

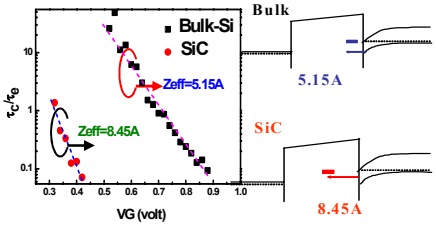

Fig. 9 nMOSFETs. (a) Plot of τ_c/τ_e versus gate voltages. (b) The effective depth location for the two traps.

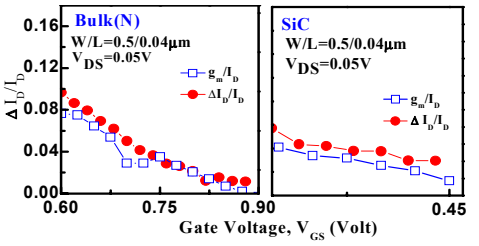

Fig. 10 Normalized RTN amplitude versus gate voltages. (left) Bulk-Si (right) SiC n-MOSFET. The open squares are the normalized conductance change g_m/I_D.

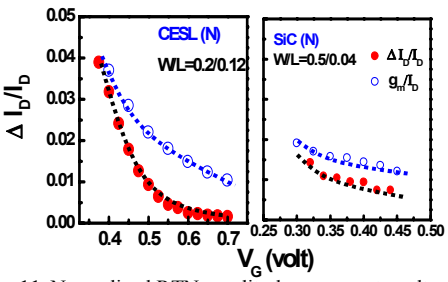

Fig. 11 Normalized RTN amplitude versus gate voltages. (left) Bulk-Si (right) CESL n-MOSFET. Note that these results show that CSEL exhibits a different drain current fluctuation compared to the SiC ones.

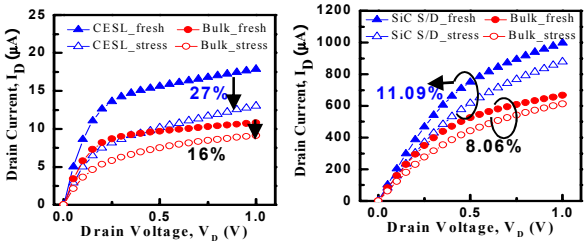

Fig. 12 Comparison of drain current degradation results for CESL (left) SiC on S/D nMOSFETs (right). CSEL device shows much larger degradation than the SiC S/D ones.

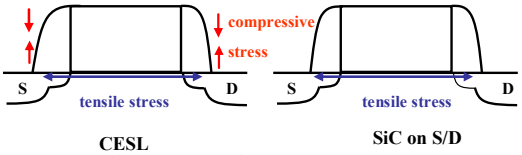

Fig. 13 Illustration of the various strains for CESL nMOSFET (left) and SiC on S/D nMOSFET (right).