A BENDING N-WELL BALLAST LAYOUT TO IMPROVE ESD ROBUSTNESS IN FULLY-SILICIDED CMOS TECHNOLOGY

Yong-Ru Wen[1], Ming-Dou Ker[1, 2], and Wen-Yi Chen[1]

[1] Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan
[2] Department of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan

ABSTRACT

Ballast technique has been reported as a cost effective method to improve ESD robustness of fully-silicided devices without using silicide block. In this work, a new ballast technique, the bending N-Well (BNW) ballast structure, is proposed to enhance ESD robustness of fully-silicided NMOS. With a deep N-Well to cover the fully-silicided NMOS with BNW ballast structure, ESD robustness of the NMOS can be further improved by enhancing the turn-on uniformity among the multi-fingers of the NMOS.

INTRODUCTION

In order to enhance the operating speed, silicidation of CMOS devices has become a standard process step in advanced CMOS technologies. Unfortunately, silicidation also reduces ballast resistance of ESD protection devices, which causes ESD current to concentrate within the shallow silicided surface of ESD devices. This results in low ESD robustness of fully-silicided CMOS devices [1], [2]. To restore the lowered ballast resistance, silicide blocking (SB) is an essential and useful technique to improve ESD robustness of fully-silicided NMOS. As the layout top-view and device cross-sectional view of an ESD protection NMOS shown in Fig. 1, the SB can prevent silicidation from being formed on the selected area. By using the SB on ESD protection devices, the ESD robustness of CMOS ICs can be restored without affecting the operating speed of internal circuits [3], [4]. However, additional process steps and mask layer for the SB increase the cost for production. To maintain enough ballast resistance for ESD protection NMOS without using the SB, several ballasting designs have been proposed [5]-[9]. In addition to the lowered ballast resistance of fully-silicided NMOS, asymmetry of parasitic substrate resistances (Rsub) among fingers of ESD protection NMOS has been recognized as another factor to limit ESD robustness of ESD protection NMOS [10], [11]. As shown in the device cross-sectional view of an NMOS in Fig. 1, different distances from the base regions of parasitic n-p-n bipolar junction transistors (BJTs) to the grounded P+ guard ring result in different parasitic Rsub values of parasitic BJTs. The asymmetry of Rsub leads to non-uniform triggering of ESD protection NMOS during ESD stresses. Accordingly, reducing the asymmetry of Rsub among fingers of fully-silicided NMOS is another design target of this work.

BALLAST RESISTANCE TO ESD PROTECTION NMOS

Fig. 2 shows the layout top view and cross-sectional view of NMOS with the traditional N-Well ballast structure [2]. The shallow trench isolation (STI) structure in the N-Well ballast structure blocks the silicidation in the drain side. To improve the ESD robustness of fully-silicided NMOS, an N-Well covers the drain side to increase the ballast resistance and to preserve the driving capability of the NMOS. With the high sheet resistance of N-Well, the N-Well ballast structure has been reported to effectively increase ESD robustness of CMOS ICs [5]-[6], [12].

Besides the N-Well ballast structure to increase ballast resistance,

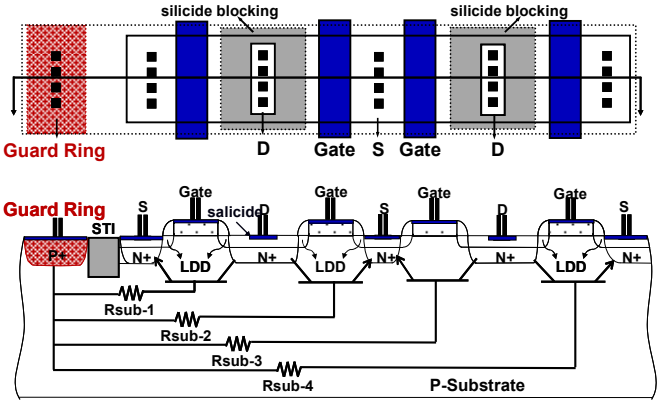


FIGURE 1. THE LAYOUT TOP-VIEW AND THE DEVICE CROSS-SECTIONAL VIEW OF NMOS WITH SILICIDE BLOCKING.

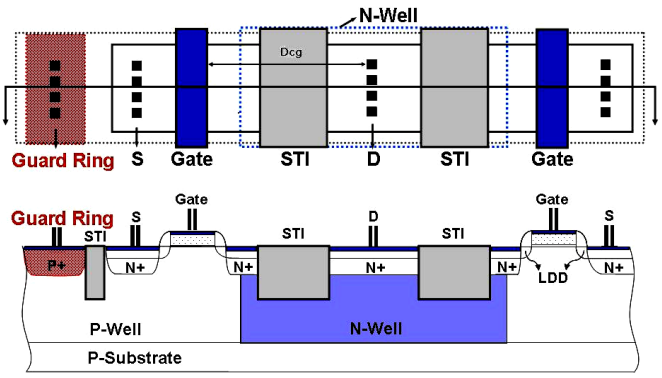


FIGURE 2. THE LAYOUT TOP-VIEW AND THE DEVICE CROSS-SECTIONAL VIEW OF FULLY-SILICIDED NMOS WITH THE N-WELL BALLAST STRUCTURE.

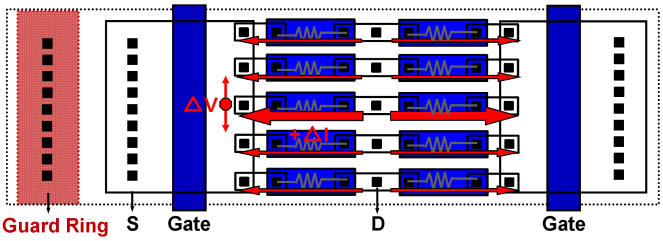
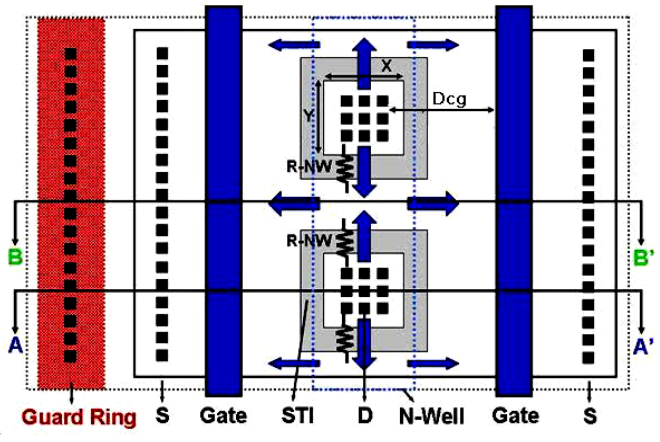


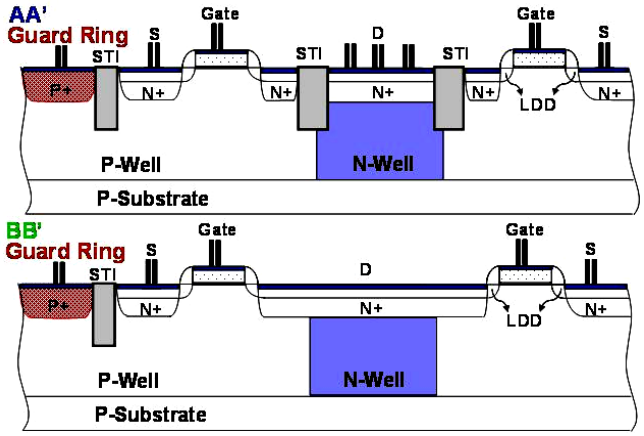
FIGURE 3. MECHANISM OF CURRENT DEFOCUS TO IMPROVE ESD CURRENT UNIFORMITY IN FULLY-SILICIDED ESD PROTECTION NMOS (REDRAWN AFTER [7]).

several techniques exploiting the current defocus have been proposed [7]-[9]. The idea of current defocus is illustrated in Fig. 3 [7]. ESD current is first divided into segments by using techniques such as the poly back-end ballast (BEB) or active-area segmentation (AAS) method [7], [8]. During ESD stresses, local current crowding (ΔI)

leads to locally increased voltage (ΔV) due to the ballast resistance along the crowded current path. This voltage difference (ΔV) forces ESD current to redistribute, which improves ESD robustness by enhancing the uniformity of current distribution.



(a)

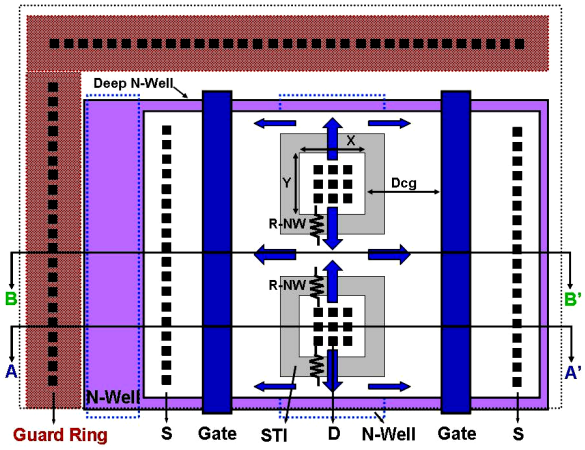


(b)

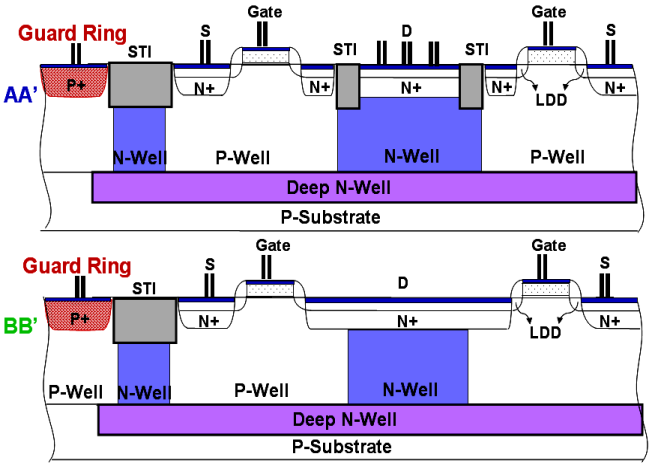
FIGURE 4. (A) THE LAYOUT TOP-VIEW AND (B) THE DEVICE CROSS-SECTIONAL VIEW OF NMOS WITH THE BENDING N-WELL BALLAST RESISTOR STRUCTURE.

NEW PROPOSED DEVICE STRUCTURES

With the purpose of increasing ballast resistance without using the SB, the bending N-Well ballast resistor (BNW) structure is proposed in this work. Figs. 4(a) and 4(b) respectively show the layout top view and the device cross-sectional view of an ESD protection NMOS with the BNW structure. Along the AA' cross-section, the drain (D) diffusion region is split by a STI ring and covered with the N-Well. N-Well is intentionally drawn in halfway of the STI region, leaving the reverse biased N-Well/P-Well junction along AA' line. Along the BB' cross-section, the N-Well connects to a diffusion region which is adjacent to the drain-side STI rings. During positive ESD stresses at the drain side with source relatively grounded, the ESD current flowline is shown as the blue arrorws in Fig. 4(a). The direction of the ballast resistor (R-NW) in the BNW structure is lengthwise as that in the traditional N-Well ballast structure is widthwise. Because the lengthwise N-Well ballast design does not enlarge overall layout length or width of the device but the widthwise N-Well ballast design does, fully-silicided NMOS with BNW design can be more compact than that with the traditional N-Well ballast structure. For example, the distance from drain contact to poly gate edge (Dcg) of a traditional N-Well ballast structure is 2.38μm, and it can be as small as 0.89μm in the BNW structure.



(a)



(b)

FIGURE 5. (A) THE LAYOUT TOP-VIEW AND (B) THE CROSS-SECTIONAL VIEW OF NMOS WITH THE BENDING N-WELL BALLAST RESISTOR STRUCTURE COVERED WITH DEEP N-WELL.

Besides the ballast resistance from N-Well, the small silicided N+ active area between two drain-side STI rings provides the function of current segmentation. As a result, when ESD current starts to localize, current defocus can help improve ESD current uniformity and enhace ESD robusntess of the fully-silicided NMOS with the BNW structure at the same time.

To further improve the turn-on uniformity among fingers of the ESD protection NMOS, Figs. 5(a) and 5(b) respectively show the layout top view and the device cross-sectional view of the BNW structure covered with deep N-Well. With the deep N-Well, the electrical short circuit from body regions (P-Well) to P+ guard rings at left and right sides through the P-Substrate is blocked. Base regions of parasitic n-p-n BJTs are grounded through P+ guard rings at up and down sides. This mitigates asymmetry of parasitic base resistors (Rsub) between fingers, which can enhance turn-on uniformity among multi-finger ESD protection NMOS during ESD stresses.

EXPERIMENTAL RESULTS

The TLP-measured secondary breakdown currents (It2) and Human-Body-Model (HBM) ESD levels were measured to investigate the ESD robustness of fully-silicided NMOS devices. I-V curves of NMOS devices were measured using a transmission line pulse (TLP) system with a pulse width of 100ns. The ESD failure criterion of devices is that the leakage current is greater than 1mA under the drain bias of 1.0V with gate grounded (GGNMOS). Fig. 6 shows the TLP-measured I-V curves of fully-silicided NMOS with the traditional N-Well ballast structure and the BNW structure with or without deep N-Well. Devices studied in this work were fabricated in a 55-nm CMOS process.

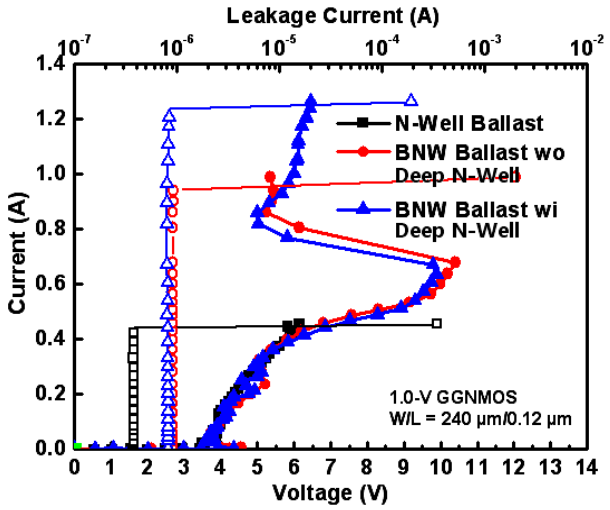


FIGURE 6. THE TLP-MEASURED I-V CURVES OF THE TRADITIONAL N-WELL BALLAST STRUCTURE AND THE BENDING N-WELL BALLAST RESISTOR STRUCTURE IN A 55-NM CMOS PROCESS. THE LEAKAGE TEST VOLTAGE FOR ALL DEVICES IS 1.0V.

From the measurement data shown in Fig. 6, It2 of fully-silicided NMOS with the traditional N-Well ballast structure is 0.44A. With the current defocus to alleviate current localization during ESD stresses, the It2 of the fully-silicided NMOS with the BNW structure was increased to 0.93A when Dcg was drawn with 1.61µm. Further enlarging the Dcg spacing to 2.33µm can improve It2 to 1.15A, which may come from the higher voltage difference (ΔV in Fig. 3) to redistribute the localized ESD current. With the deep N-Well to alleviate the asymmetry of parasitic Rsub between fingers, the measured It2 for fully-silicided NMOS with the BNW structure and 1.61-µm Dcg is 1.24A. The It2 per area of a GGNMOS with N-Well ballast, the BNW ballast without deep N-Well, and the BNW ballast with deep N-Well are 0.32, 0.52, and 0.69 mA/µm^2, respectively.

From the TLP measurement results, a large turn-on resistance is observed and increases with increasing TLP current level. Moreover, there is a second snapback around the current level of 0.6A. The observed second snapback is related to the second snapback inside the N-Well [5]. While the TLP pulse energy increases step by step, the N+/P-Well junction breaks down and triggers on the parasitic n-p-n BJT. At high current region, velocity saturation of electrons in the ballast N-Well results in the substantially increased turn-on resistance. As the build-up electric field is large enough, the second snapback happens. This phenomenon also happens in NMOS with the N-Well ballast structure, but the measured NMOS failed before the onset of second snapback. With the current defocus, fully-silicided NMOS with the BNW structures can sustain higher It2 values so that the second snapback phenomenon can be observed.

Scanning electron microscopy (SEM) image of the ESD-stressed fully-silicided NMOS with the BNW strucutre is shown in Fig. 7. Metamorphosed silicide was uniformly found over the drain of the device.

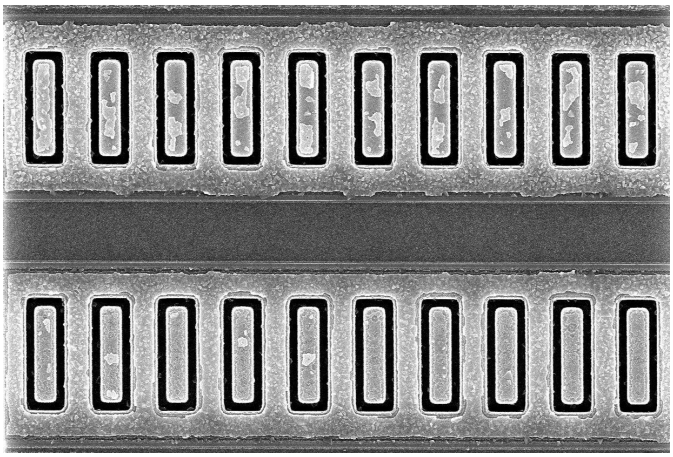
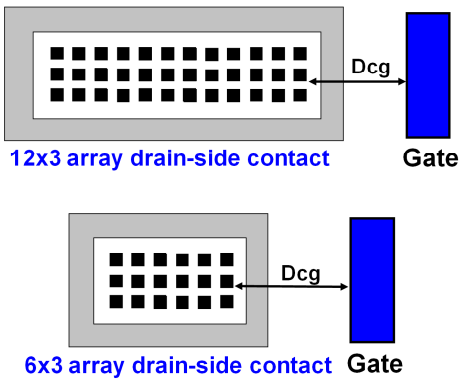


FIGURE 7. SEM IMAGE OF THE ESD-STRESSED FULLY-SILICIDED NMOS WITH BNW STRUCTURE.

Comparisons between the traditional slicide-blocked multi-finger GGNMOS, the fully-silicided GGNMOS with the traditional N-Well ballast structure, or with the proposed BNW structure (without deep N-Well) are summarized in Table I. Different drain-side contact

TABLE I
DIFFERENT ARRANGEMENTS OF DRAIN-SIDE CONTACT ARRAY TO IT2, HBM ESD LEVEL, AND IT2 PER AREA.

	Silicide Blocking	Contact Array	X (µm)	Y (µm)	Dcg (µm)	W/L (µm/µm)	It2 (A)	HBM (kV)	Area (µm^2)	It2/Area (mA/µm^2)
Traditional Multi-Finger NMOS	Yes	--	--	--	2.15	120/0.12	0.860	2.0	839	1.03
		--	--	--	2.15	240/0.12	1.677	3.0	1512	1.11
N-Well Ballast	No	--	--	--	2.38	240/0.12	0.44	0.8	1404	0.32
BNW Ballast without Deep N-Well		6x3	1.32	0.6	1.91	240/0.12	0.67	1.8	1540	0.43
		6x5	1.32	1.08	1.91	240/0.12	0.73	2.4	1540	0.47
		12x3	2.28	0.6	0.89	240/0.12	0.70	2.2	1540	0.46
		12x3	2.28	0.6	1.61	240/0.12	0.93	2.8	1791	0.52
		12x3	2.28	0.6	2.33	240/0.12	1.15	3.2	2027	0.57



array arrangements were used to investigate the corresponding ESD robustness. Measurement results showed that ESD robustness of the GGNMOS with the BNW structure increases as the contact array expands. Measurement results also showed that the Dcg parameter is crucial to ESD robustness of fully-silicided NMOS with the BNW structure. Though fully-silicided NMOS devices with the BNW structure showed the lower It2/Area ratios compared with traditional silicide-blocked NMOS devices, fully-silicided NMOS devices with the BNW structure are still attractive because process steps and mask layers for the silicide blocking are not needed in these devices.

CONCLUSION

To improve the ESD robustness of fully-silicided NMOS, the bending N-Well ballast resistor structure has been proposed and verified in a 55-nm CMOS process. Experimental results have confirmed that fully-silicided NMOS with the new proposed BNW structure has better ESD robustness than that with the traditional N-Well ballast structure. The insertion of deep N-Well can mitigate the asymmetry of parasitic base resistance between fingers of the fully-silicided NMOS with the BNW structure, which further improves the ESD robustness of the NMOS. Without using the silicide blocking, the new proposed BNW structure in this work provides a cost effective ESD design solution to nano-scale CMOS technologies.

ACKNOWLEDGEMENT

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