Use of Random Telegraph Signal as Internal Probe to Study Program/Erase Charge Lateral Spread in a SONOS Flash Memory

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Abstract—A novel random telegraph signal (RTS) method is proposed to study the lateral spread of injected charges in program/erase of a NOR-type SONOS flash memory. The concept is to use RTS to extract an interface trap position and to detect a local potential variation near the trap due to injection of program/erase charges. By using this method, we find that CHISEL program has a broader charge distribution than CHE program. A mismatch of CHE program electrons and band-to-band erase holes is observed directly from this method.

I. INTRODUCTION

Two-bit/cell SONOS flash memory has been realized by storing bit charges in two sides of the channel by CHE program and band-to-band hot hole erase [1]. The control of program and erase charge lateral distributions of each bit is a major research thrust to improve cell endurance and scalability [2,3]. Attempts have been made in the past to characterize a trapped charge distribution in a SONOS cell. An inverse modeling approach is used to extract a program charge distribution from measured I-V characteristics [4]. Besides, a modified charge pumping (CP) technique [5] is employed to probe the lateral profile of programmed charges at the source and drain junctions separately. However, the inverse I-V modeling suffers from some limitations, for example, knowledge of precise device doping profile and lack of a unique solution. On the other side, the CP method is based on an assumption that interface traps have a uniform distribution along the channel [6], which is not correct in a buried diffusion bit-line SONOS cell. In addition, a charge pumping current is hardly sensed in a small area SONOS device.

In this work, we will use RTS arising from charge emission and capture at an oxide trap to investigate program/erase charge lateral spread. First, we determine the trap position from RTS without the need to know doping profile. Second, because RTS is very sensitive to a local potential change near the trap, we can use oxide traps as internal probes to detect a potential change due to program/erase charges. Finally, by using this technique, we find that CHISEL program has a broader charge distribution than CHE program and a mismatch of CHE program electrons and band-to-band erase holes is observed.

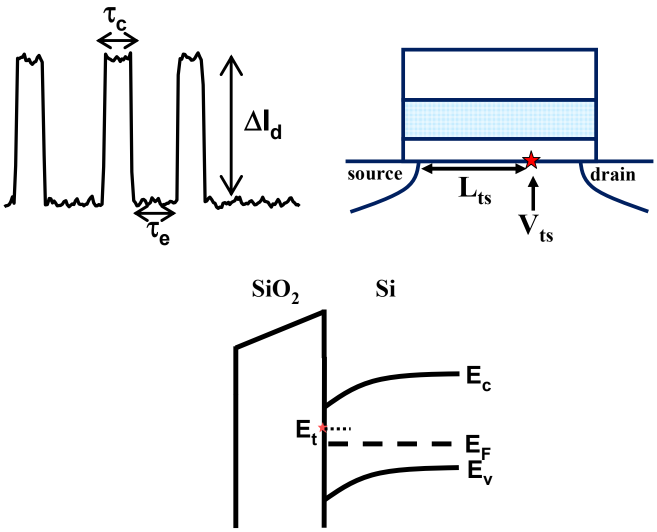

Fig. 1 Illustration of an interface trap induced RTS and the energy band diagram.

II. MEASUREMENT RESULT

Experiments were performed on SONOS flash cells with an ONO thickness of 8.5nm (top oxide), 7nm and 5.8nm, respectively. The cell size is W/L=0.11µm/0.1µm. The CHE program condition is V_{gs}=8V and V_{ds}=3.7V. The band-to-band hot hole (BTBH) erase is performed at V_{gs}= -4V and V_{ds}=5V.

A. Extraction of a Trap Position

An oxide trap position in the channel can be extracted in a way similar to the method in [7]. The RTS capture time τ_c, as illustrated in Fig. 1, can be expressed below,

$$<\tau_c>=1/n_e\sigma v_{th} \tag{1}$$

where σ is the trap cross-section and v_{th} is the thermal velocity. The channel electron concentration n_e is a function of gate overdrive, i.e.V_{gs}-V_{ts}, where V_{ts} is the channel potential at the trap position and is equal to $V_{ts}=(L_{ts}/L)V_{ds}$. L_{ts} is the distance of the trap from the source and L is the channel length, as shown in Fig. 1.

Two different V_{ds} (=0.05V and 0.3V) are used in RTS and capture time (τ_c) measurement. Note that the device is in the linear region at the measurement biases. Since the capture

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time is dependent on an electron concentration near the trap, or in other words, a voltage drop between the gate (V_{gs}) and the channel right below the trap (V_{ts}), the amount of the lateral shift of these two curves (ΔV_{ts}) in Fig. 2 is equal to the difference of the voltages, raised by the two drain voltages, at the point (L_{ts}) of the trap. Therefore, the trap position in the channel can be extracted from $\Delta V_{ts}/\Delta V_{ds}=L_{ts}/L$. In this work, the RTS extraction is conducted in more than 30 un-cycled devices. For simplicity, we only record devices with two-level RTS (i.e., a single trap). The extracted trap position distribution is shown in Fig. 3. With this information, we can choose devices with appropriate trap positions as internal probes to investigate program/erase charge lateral spread.

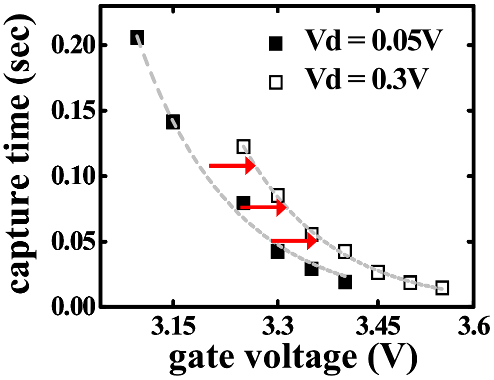


Fig. 2 The gate voltage dependence of average capture time in RTS at two drain voltages, V_{ds}=0.05V and 0.3V. The lateral shift of these two curves corresponds to ΔV_{ts}.

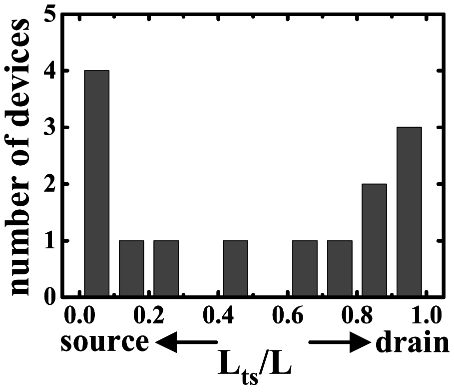


Fig. 3 Cumulative trap position distribution along the channel. L is the channel length and L_{ts} is the distance of a trap to the source.

B. Detection of a local potential change

The ratio of τ_c/τ_e is dependent on the local potential at the trap position, i.e.

$$\langle\tau_c\rangle/\langle\tau_e\rangle = g\exp[(E_t-E_F)/kT] \sim \exp(-q\Delta\varphi_s/kT) \quad (2)$$

where g is a pre-factor, E_t is the trap energy and $\Delta\varphi_s$ is a local potential change at the trap position.

C. CHE and CHISEL Programming

In order to detect a surface potential change near the drain during CHE program, a SONOS cell having a trap at x_t=0.2L from the drain edge is used. Fig. 4 shows the average emission time (τ_e) and capture time (τ_c) versus program ΔV_T [8,9]. Fig. 5(a) illustrates the band diagrams during CHE program. The trap energy level increases with respect to the Fermi level as program charge increases. The ratio of (τ_c/τ_e) and the corresponding surface potential change ($\Delta\varphi_s$) from Eq. (2) are plotted in Fig. 5(b). As more electrons are injected into the nitride layer, the conduction band at x_t and the trap level move upward away from the Fermi level. Thus, the τ_c/τ_e ratio becomes larger and larger.

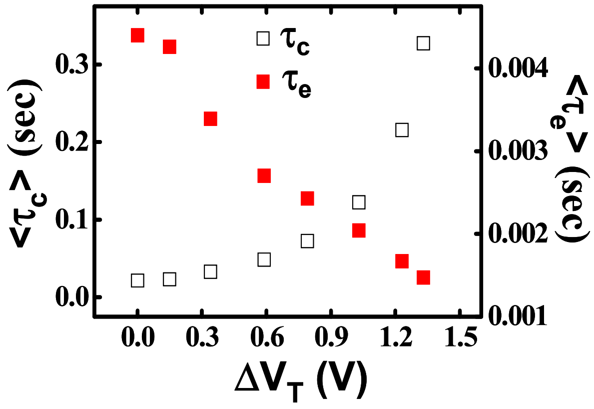


Fig. 4 Average capture time (τ_c) and emission time (τ_e) versus program ΔV_T.

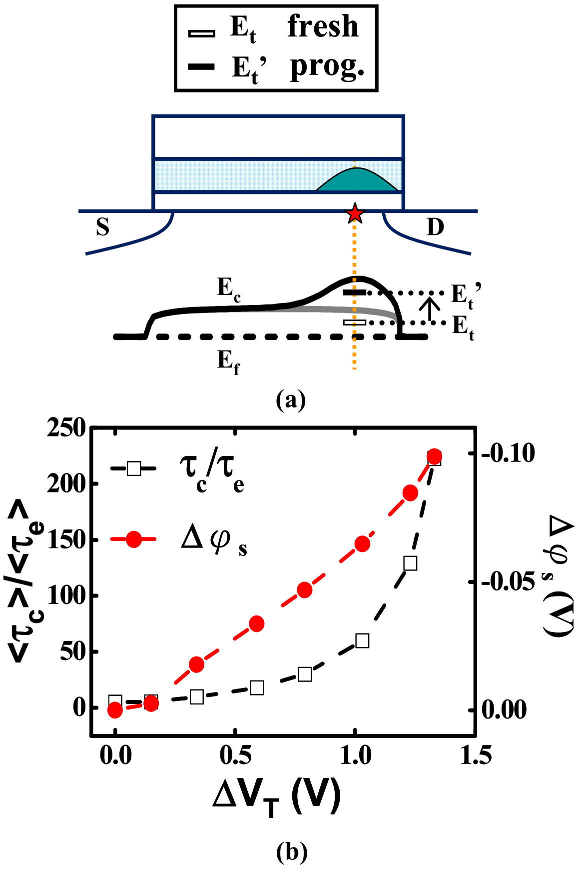


Fig. 5 (a)Band diagrams before and after CHE program. (b) $<\tau_c>/<\tau_e>$ and surface potential change versus program ΔV_T. The local potential change ($\Delta\varphi_s$) at the trap position is calculated from Eq. (2).

Fig. 6 compares the τ_c/τ_e in source side programming and drain side programming. The τ_c/τ_e remains unchanged during source-side programming, as expected, since program charges are near the source junction while the trap is near the drain edge. We also compare the program charge spread by CHE and CHISEL [10] in Fig. 7. The substrate bias is -2V in CHISEL operation. During CHISEL program, holes generated by channel electron impact ionization flow to the substrate and result in secondary impact ionization. The secondary electrons, accordingly, would be accelerated by the drain voltage and inject into the nitride layer. Fig. 7 shows that CHISEL has a broader injected charge distribution than CHE because the τ_c/τ_e and the potential change are larger at the same program ΔV_T.

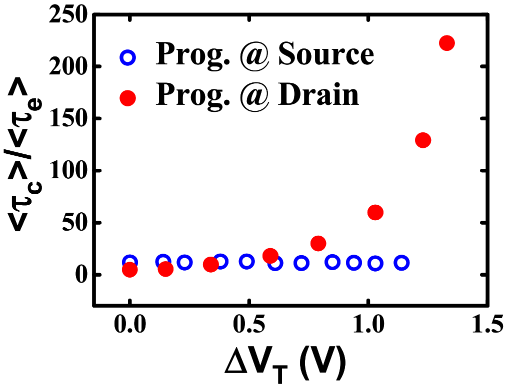


Fig. 6 Comparison of $\langle\tau_c\rangle/\langle\tau_e\rangle$ evolutions in source-side CHE program and in drain-side CHE program. Since the trap is near the drain, $\langle\tau_c\rangle/\langle\tau_e\rangle$ remains unchanged in source-side programming.

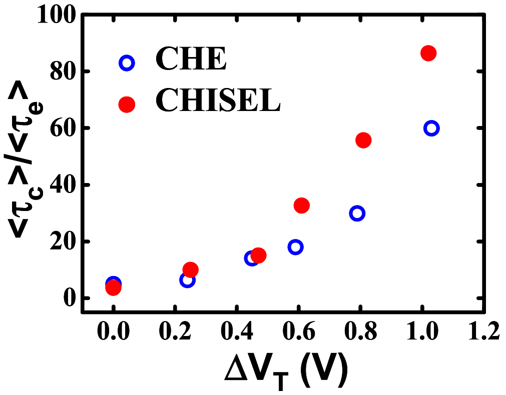


Fig. 7 Comparison of $\langle\tau_c\rangle/\langle\tau_e\rangle$ evolutions by CHE program and by CHISEL program. A substrate bias of -2V is applied in CHISEL injection.

D. BTBH Erase and Program/Erase Charge Mismatch

For comparison, we choose two devices with a respective trap position at 0.05L and 0.3L from the drain. CHE program and BTBH erase are performed. The τ_c/τ_e evolutions during program/erase are shown in Fig. 8 (in the x_t=0.05L cell) and in Fig. 9 (x_t=0.3L cell). The τ_c/τ_e increases as program V_T increases by CHE program and decreases by hot hole erase. For the point near the drain (i.e., x_t=0.05L), the τ_c/τ_e curves in program and in erase match very well, suggesting that program electrons at 0.05L are totally neutralized by erase holes. In contrast, at the point of x_t=0.3L from the drain, the τ_c/τ_e does not return to its original value after a P/E cycle. The larger τ_c/τ_e value during erase implies that program electrons (at 0.3L) are not completely compensated although the cell has been erased to its original V_T.

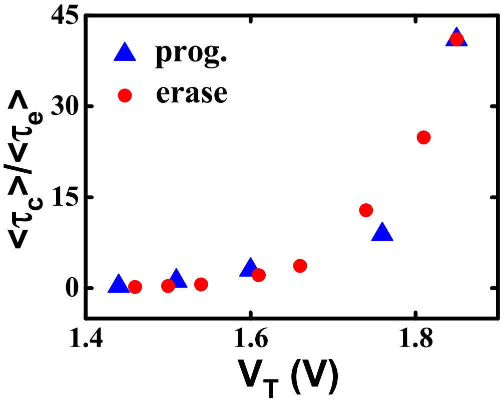


Fig. 8 The $\langle\tau_c\rangle/\langle\tau_e\rangle$ evolutions during CHE program and BTBH erase. The device has a trap at 0.05L from the drain. The $\langle\tau_c\rangle/\langle\tau_e\rangle$ has the same path in P/E.

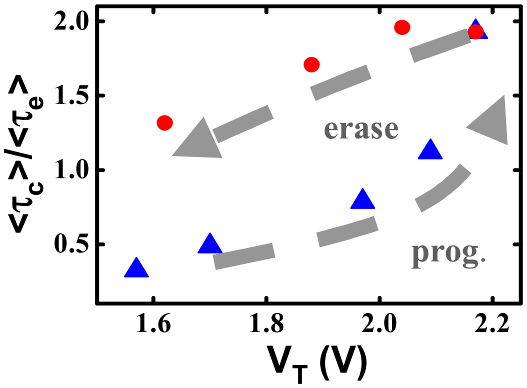
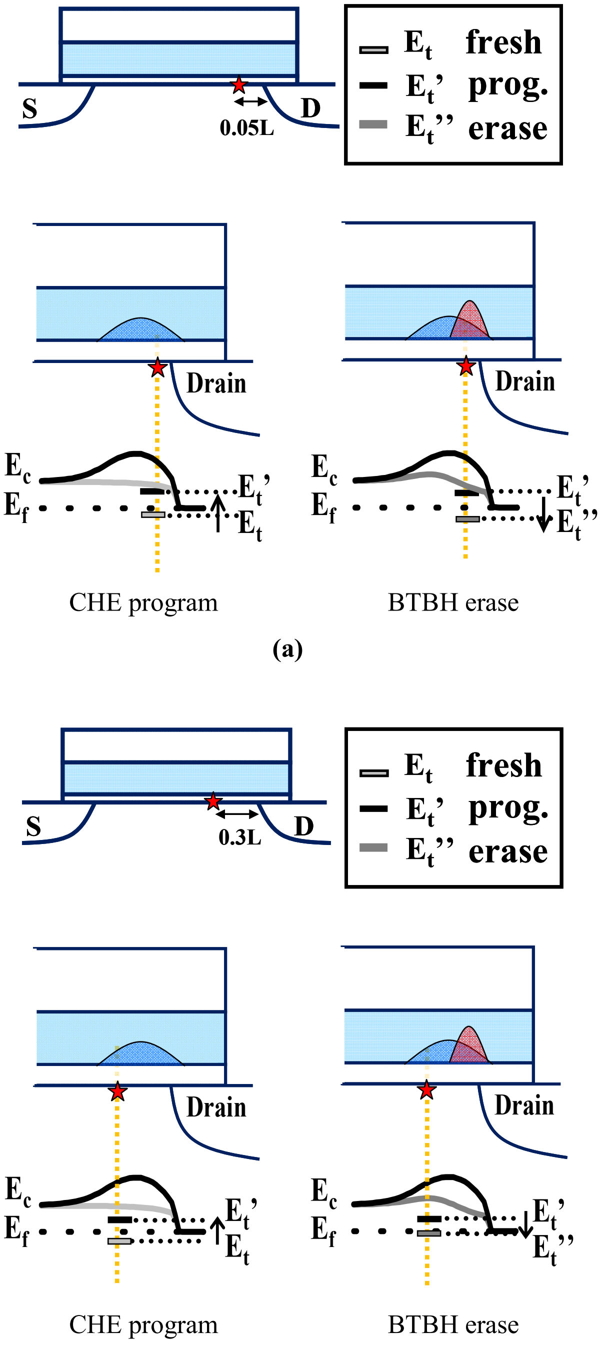


Fig. 9 The $\langle\tau_c\rangle/\langle\tau_e\rangle$ evolutions during CHE program and BTBH erase. The device has a trap at 0.3L from the drain. The erase path of $\langle\tau_c\rangle/\langle\tau_e\rangle$ is different from the program path.

Fig. 10 illustrates the program/erase charge distributions and the band diagrams after program and erase. The trap position is at x_t=0.05L from the drain in Fig. 10(a), and 0.3L from the drain in Fig. 10(b). In Fig. 10(a), the trap level increases with respect to the Fermi level due to program electron injection and decreases due to erase hole injection. In Fig. 10(b), the trap level increases due to program electrons, but is not affected by injected erase holes. The result in Fig. 9 implies that injected holes have a narrower distribution than program electrons.

III. CONCLUSION

We propose a novel RTS method to characterize program and erase charge lateral spread in a SONOS flash memory without the need to know a doping profile. Since the RTS method is very sensitive to a local potential change due to program/erase charges, it can provide a better resolution than a charge pumping method or an inverse I-V modeling approach. An evidence of a mismatch between program electrons and erase holes is shown by this method.



(b)

Fig. 10 Illustration of program/erase charge distributions and the band-diagrams after program and erase. The star represents interface trap position at (a) x_t=0.05L and (b) x_t=0.3L from the drain edge. The program electrons at x_t=0.05L are completely compensated, but some far electrons at x_t=0.3L are not compensated after erase.

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REFERENCES

[1] Boaz Eitan, Paolo Pavan, Ilan Bloom, Efraim Aloni, Aviv Frommer, and David Finzi, "NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," *IEEE Trans. Electron Devices*, vol. 21, pp. 543–545, Nov. 2000.

[2] Arnaud Furnemont, Maarten Rosmeulen, Koen van der Zanden, Jan Van Houdt, Kristin De Meyer, and Herman Maes, "Physical Modeling of Retention in Localized Trapping Nitride Memory Devices" *IEDM Tech. Dig*., pp.397–400, 2006

[3] Yao-Wen Chang, Tao-Cheng Lu, Sam Pan, and Chih-Yuan Lu, "Modeling for the 2nd-Bit Effect of a Nitride-Based Trapping Storage Flash EEPROM Cell Under Two-Bit Operation," *IEEE Electron Device Lett*., vol. 25, pp. 95–97, Feb. 2004.

[4] Luca Larcher, Giovanni Verzellesi, Paolo Pavan, E. Lusky, Ilan Bloom, and Boaz Eitan, "Impact of Programming Charge Distribution on Threshold Voltage and Subthreshold Slope of NROM Memory Cells," *IEEE Tran. Electron Devices*, vol. 49, pp. 1939–1946, Nov. 2002

[5] Shaw-Hung Gu, Tahui Wang, Wen-Pin Lu, Wenchi Ting, Yen-Hui Joseph Ku, and Chih-Yuan Lu, "Characterization of Programmed Charge Lateral Distribution in a Two-Bit Storage Nitride Flash Memory Cell by Using a Charge-Pumping Technique," *IEEE Tran. Electron Devices*, vol. 53, pp. 103–108, Jan. 2006

[6] Chun Chen, and Tso-Ping Ma, "Direct Lateral Profiling of Hot-Carrier-Induced Oxide Charge and Interface Traps in Thin Gate MOSFET's," *IEEE Tran. Electron Devices*, vol. 45, pp. 512–520, Feb. 1998

[7] Phillip Restle, "Individual oxide traps as probes into submicron devices," *Appl. Phys. Lett*., 53, pp. 1862–1864, Nov. 1988

[8] K. Kandiah, M. O. Deighton, and F. B. Whiting, "A Physical Model for Random Telegraph Signal Currents in Semiconductor devices," *J. Appl. Phys*., vol.66, pp. 937–948,July 1989

[9] K. Kandiah, "Random Telegraph Signal Currents and Low-Frequency Noise in Junction Field Effect Transistors," *IEEE Tran. Electron Devices,* vol. 41, pp. 2006–2015,Nov. 1994

[10] Jeff D. Bude, Mark R. Pinto, and R. Kent Smith, "Monte Carlo Simulation of the CHISEL Flash Memory Cell," *IEEE Tran. Electron Devices*, vol. 47, pp. 1873–1881, Oct. 2000