A Frequency Accuracy Enhanced Sub-10μW On-Chip Clock Generator for Energy Efficient Crystal-Less Wireless Biotelemetry Applications

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Abstract

A frequency accuracy enhanced clock generator is proposed for energy efficient crystal-less WBAN system. By applying a self-reference calibration and tracking a remote downlink wireless reference, the robust system clock with ±30ppm accuracy against both 20% voltage variation and 75°C temperature variation is developed to enable over-Mbps uplink data transmission. Furthermore, the clock generator based on hysteresis delay cells consumes 7.6μW in 5MHz and is able to minimize significant always-on clock source power.

Introduction

Severe power requirement and tiny size integration are critical for wireless sensor node (WSN) design in wireless body area network (WBAN) systems. The quartz crystal, as conventional system reference, is a bottleneck due to the existence of bulky external components during heterogeneous process integration with CMOS. In contrast, on-chip CMOS oscillator benefits in minimizing form factor and fabrication cost, but its limited frequency accuracy results in merely sub-Mbps achievable data rate [1-2]. In fact, WBAN system with mega-scale data rate [3] is more energy efficient for real-time body signal monitoring since its burst transmission minimizes system duty-cycle. On the other hand, it is quite essential to diminish clock source power because the always-on operation consumes relatively large proportions of total power, e.g. 68% for [2], in on-off duty senor network. Accordingly, this work addresses on a 5MHz clock generator with enhanced ±30ppm accuracy compatible for over-Mbps data transmission and sub-10μW feature as well.

Proposed On-Chip Clock Generator

Fig.1 shows block diagram of the proposed clock generator with corresponding system architecture. The system clock is generated from a hysteresis delay cell (HDC) based digitally-controlled oscillator (DCO), which is controlled by a PVT calibrator (PVT-CAL) and a remote reference frequency tracker (RRFT) for coarse and fine frequency calibration. Initially, PVT-CAL provides self-calibration ability with ±3% accuracy to enable the operation of downlink (DL) receiver, which merely requires very low complexity architecture [4]. Then, RRFT tracks a DL sinusoidal RF-reference broadcasted from central processing node (CPN) for further ±30ppm calibration to enable uplink (UL) data transmission.

Fig. 2 shows the PVT-CAL block diagram. It generates an internal reference clock by a self-reference (SR) DCO and adjusts HDC-DCO codeword C_{HDC} to align with SR-DCO frequency. The delay ratio estimator estimates the delay ratio R_D of SR-DCO cell (with delay D_{SR}) and a chosen compared cell (with delay D_{COMP}). Their different delay properties against PVT enable R_D to reflect actual D_{REF} delay value. More specifically, Fig. 3(a) shows the relation of D_{REF} and R_D by sweeping three process corners with voltage of 0.9V~1.1V and temperature of 0°C~75°C. So, codeword mapper can approximate D_{REF} by $\underline{D}_{REF}$, which is a second-order polynomial function of R_D as shown in Fig. 3(b), to generate corresponding SR-DCO codeword C_{SR} in 5MHz. The process dependent parameters (PDPs) a_p, b_p and c_p are calculated and stored during first-time post-process testing.

Fig. 4 shows the RRFT block diagram with signal flow and Fig. 5 illustrates its tracking procedure. The tracking engine iteratively adjusts C_{HDC} according to edge counter output N_{ERR} triggered by the IF signal in mixer output which reflects RF frequency error. Instead of directly estimating frequency error from N_{ERR}, a binary-search based tracking procedure is proposed to prevent the influence of glitches in N_{ERR} at low-SNR condition. During *n-th* iteration, HDC-DCO clock is in turn adjusted to frequency $f_{L,n}$ and $f_{H,n}$ for corresponding N_{ERR} accumulation within a same period by appropriate N_{DCO} control. The interval between $f_{L,n}$ and $f_{H,n}$ is denoted as search window S_n and its median frequency $f_{M,n}$ represents the tracking result of *n-th* iteration. The next S_{n+1} is decided by $f_{M,n}$ and the frequency chosen from $f_{L,n}$ and $f_{H,n}$ with less N_{ERR} value. Accordingly, the search window is continuously reduced by half from initial value ±3% to target ±30ppm and $f_{M,n}$ approaches 5MHz via successive iterations.

To provide ultra low power feature, the HDC-DCO with power-of-two structure is proposed in Fig. 6 to generate (2^k-*1*) even different delay values with only *k* delay segments. Each delay segment occupies similar area since HDC cells feature long propagation delays with minimal transistors. Three HDC topologies in [5], i.e. nested HDC, cascaded HDC and On-Off HDC, together with MOS gate capacitance are applied to cover at least 5MHz (200ns) delay range and 30ppm (6ps) tuning resolution. Note that non-monotonic calibration circuit in [5] is eliminated since RRFT search mechanism can be applied to each tuning stage sequentially and separately.

Experimental Results

The proposed clock generator is fabricated in 1P9M 90nm CMOS process. An evaluation platform based on Fig. 1 is set up for verification. The OFDM baseband chipset in [3] is chosen as a mega-scale UL demo case, while DL path is set up by commercial FSK IC. Measured results in Fig. 7 show that system clock has at most -2.1% frequency error against both 20% voltage variation and 75°C temperature variation after PVT-CAL calibration. Fig. 8 shows the simulated and measured results for RRFT tracking. It requires 3.06ms to achieve 23.5ppm accuracy as SNR equals 7dB. The always-on HDC-DCO consumes 7.6μW in 5MHz which is competitive with state-of-the-art low-rate oscillator. Fig. 9 shows clock waveform with 49.69ps RMS jitter. In test environment with voltage and temperature variation rate slower than 41.8°C/s and 0.025V/s, the test chip enables 4.85Mbps UL transmission with 3.45ms active time (T_{ACT}). Fig. 10 and TABLE I are chip micrograph and summary. The comparison in TABLE II shows that our work provides 8X throughput than [6] and therefore achieves great energy saving from 88% system operation time reduction. Accordingly, our proposal is investigated to be an energy efficient solution for crystal-less biotelemetry applications.

References

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[2] S. Drago, et al., "Impulse-Based Scheme for Crystal-Less ULP Radios," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 5, May 2009.

[3] T. W. Chen, et al., "A 0.5V 4.85Mbps Dual-Mode Baseband Transceiver with Extended Frequency Calibration for Biotelemetry Applications," *IEEE JSSC*, vol. 44, no. 11, Nov. 2009.

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[5] M. C. Chen, et al., "A Sub-100μW Area-Efficient Digitally-Controlled Oscillator Based on Hysteresis Delay Cell Topologies," *IEEE ASSCC*, pp. 89-92, Nov. 2009.

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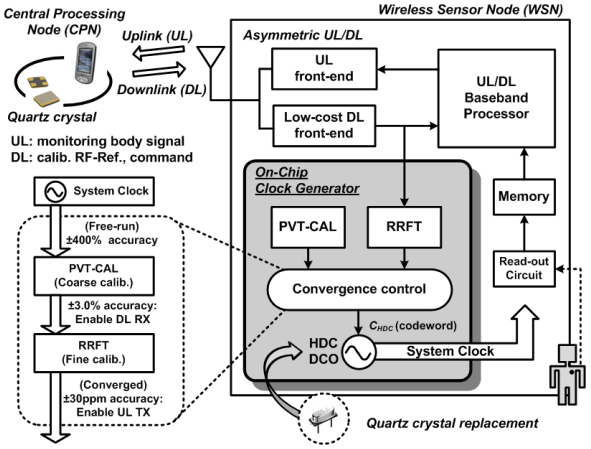


Fig. 1 Proposed clock generator with system architecture.

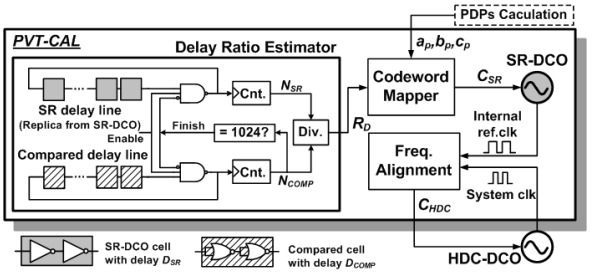
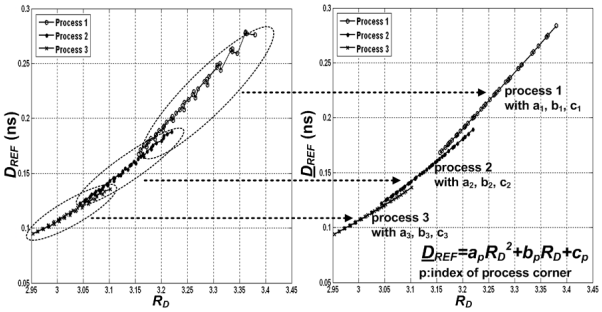
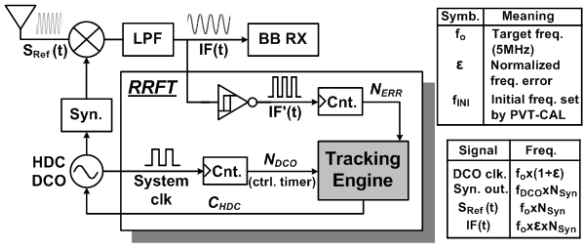


Fig. 2 PVT-CAL block diagram.



(a) (b)

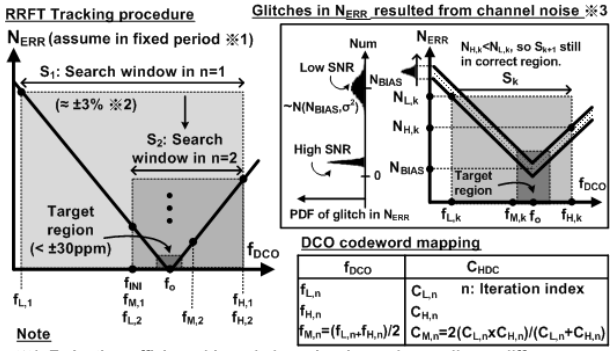
Fig. 3 (a) Relation of D_{REF} and R_D under varied PVT.
(b) Approximation of D_{REF} by $\underline{D}_{REF}$ in codeword mapper.



Symb.	Meaning
f_o	Target freq. (5MHz)
ε	Normalized freq. error
f_{INI}	Initial freq. set by PVT-CAL

Signal	Freq.
DCO clk.	f_ox(1+ε)
Syn. out.	f_{DCO}xN_{Syn}
S_{Ref} (t)	f_oxN_{Syn}
IF(t)	f_oxεxN_{Syn}

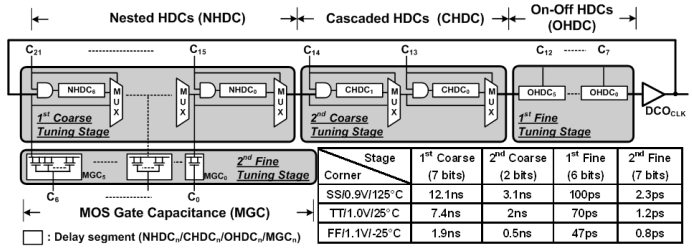
Fig. 4 RRFT block diagram and signal flow.



DCO codeword mapping

f_{DCO}	C_{HDC}
$f_{L,n}$	$C_{L,n}$ n: Iteration index
$f_{H,n}$	$C_{H,n}$
$f_{M,n}=(f_{L,n}+f_{H,n})/2$	$C_{M,n}=2(C_{L,n}xC_{H,n})/(C_{L,n}+C_{H,n})$

Fig. 5 RRFT tracking procedure illustration.



Corner \ Stage	1st Coarse (7 bits)	2nd Coarse (2 bits)	1st Fine (6 bits)	2nd Fine (7 bits)
SS/0.9V/125°C	12.1ns	3.1ns	100ps	2.3ps
TT/1.0V/25°C	7.4ns	2ns	70ps	1.2ps
FF/1.1V/-25°C	1.9ns	0.5ns	47ps	0.8ps

Fig. 6 Power-of-two HDC-DCO architecture and tuning stage resolutions.

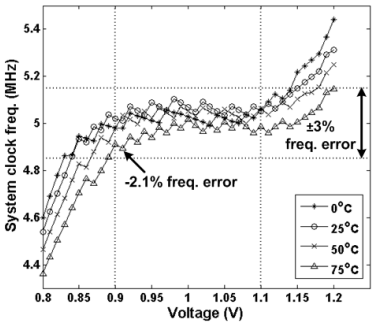


Fig. 7 System clock frequency with PVT-CAL calibration.

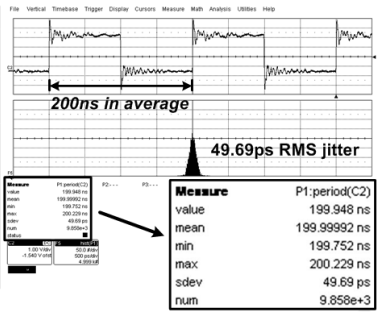
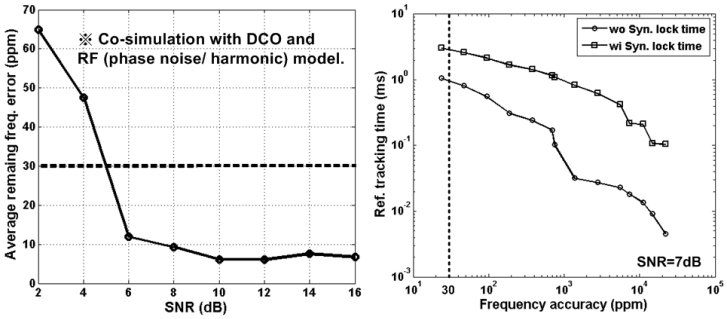


Fig. 9 Output clock waveform.



(a) (b)

Fig. 8 (a) Simulated remaining frequency error by RRFT tracking.
(b) Measured RRFT tracking time for corresponding accuracy.

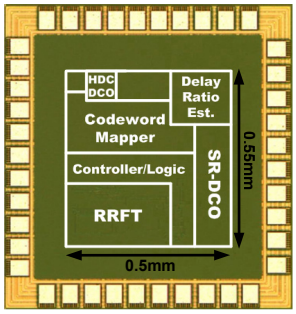


Fig. 10 Chip micrograph.

TABLE I: Chip summary

Technology	Std. 90nm CMOS 1V core, 3.3V I/O	
Core area	0.27mm^2	
Clock freq.	5MHz	
RMS jitter	49.69ps (0.025%)	
Power	(always-on) 7.6μW	
	(calib. mode) 289.5/11.3μW*	
PVT-CAL calib.	Condition	0.9~1.1V 0~75°C
	Accuracy	2.1%
	Time ($T_{PVT-CAL}$)	1.61ms
RRFT calib.	Condition	SNR=7dB
	Accuracy	23.5ppm
	Time (T_{RRFT})	3.06ms

*: wi PVT-CAL/ wi RRFT

TABLE II: Crystal-less system feature comparison

	This work with demo case [3]	[6]	[1] with [2]
Osc. type	HDC-DCO	LC-DCO	Mobility-ref.
Application	WBAN	Implant MICS	ad-hoc WSN
Modulation	OFDM**	FSK	IR-UWB
PVT tolerance	0.9°V~1.1V 0°C~75°C	N/A	1.05V~1.4V -22°C~85°C
Throughput [Mbps]	2.06***	0.25 (data rate)	0.1 (data rate)

**: Compatible for different modulation scheme, not only this demo case.
***: Data rate × [T_{ACT}/ (T_{ACT} +$T_{PVT-CAL}$+ T_{RRFT})]