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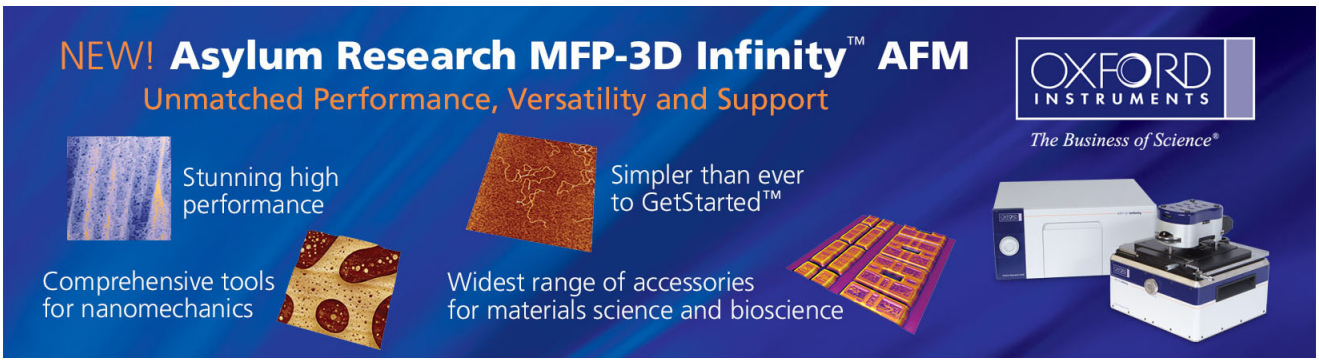

# Turnaround of hysterisis for capacitance–voltage characteristics of hafnium oxynitride dielectrics

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The capacitance–voltage ($C-V$) characteristics of hafnium oxynitride gate dielectrics for silicon metal-oxide-semiconductor (MOS) capacitors with different sweep voltage were investigated. It was found that, for the *p*-type substrate MOS capacitor, the $C-V$ hysterisis has a turnaround characteristic as the applied voltage exceeds $-3.0$ V. The phenomenon is explained by electron trappings at the low electric field and hole trappings, which resulted from the impact ionization, at the high electric field in the dielectrics. © *2004 American Institute of Physics.*
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According to the International Technology Roadmap for Semiconductors (ITRS) projection,[1] the 70 nm node technology will require a gate dielectric with an effective oxide thickness (EOT) of 7–12 Å. Nevertheless, since scaling of $SiO_2$ below 10 Å is not acceptable due to tunneling leakage and nonuniformity, the dielectrics of a high dielectric constant (high *k*) are much requested. High-*k* gate dielectrics with sufficient high dielectric constant, wide energy band gap, good interface quality, excellent process compatibility, and high stability with the Si surface are suitable for the future gate dielectric application.[2] Among high-*k* gate dielectrics, $HfO_2$ and its aluminates, silicates, and oxynitrides[3–6] are the most popular candidates being studied. Unfortunately, for these high-*k* gate dielectrics, hysteresis was generally observed in its capacitance–voltage ($C-V$) characteristics.[7,8] The hysteresis might be due to chemical contaminations, the stress-induced defect formation, mobile ions, [9] inner-interface oxide traps,[10] and border traps.[11] In this work, we investigate a turnaround phenomenon of the $C-V$ hysteresis for the hafnium oxynitride dielectrics on the *p*-type substrate capacitors. The turnaround phenomenon is shown to be due to electron trapping at the low voltage and hole trapping at the high voltage in the gate dielectrics.

Al/TaN/HfON/Si capacitors of an area of $6.36\times10^{-5}$ $cm^2$ were fabricated on 4 in. *p*-type and *n*-type Si wafers. First, the 12-nm-thick $HfO_2$ film was deposited by electron beam evaporation. After the gate dielectric had been formed, the samples were treated by $NH_3$ plasma at 20 W for 5 min in a high density plasma system to form hafnium oxynitride (HfON).[12] A TaN film of 25 nm was then deposited by a sputter. Thereafter, a 500-nm-thick Al film was deposited on the TaN film by a thermal coater. The gate of the capacitor was then defined lithographically and etched. Finally, a 500-nm-thick Al film was also deposited on the backside of the wafer to form the ohmic contact. The EOTs of the samples were estimated to be 4.65 and 4.72 nm from the high frequency (0.1 MHz) capacitance–voltage ($C-V$) curves without deducting the quantum confinement effect for the *p*-type (NMOS) and *n*-type (PMOS) substrate capacitors, respectively. The electrical properties were measured by using a HP4156B semiconductor parameter analyzer and a HP4284A precision *LCR* meter.

Figure 1 shows the $C-V$ hysteresis characteristics of HfON gate dielectrics for *p*-type and *n*-type substrate MOS capacitors swept from 0 V to different voltage $V_s$ (in the accumulation region) and then swept back. The solid lines were 0 V$\Rightarrow V_s$ and then the dashed lines were $V_s\Rightarrow$0 V. In the figure, as $V_s$ increases, the hysteresis continues to increase for the *n*-type substrate capacitors but decreases first and then increases gradually for the *p*-type substrate capacitors. The hysteresis is plotted in terms of the sweep voltage for both *n*-type and *p*-type substrate capacitors in Fig. 2, respectively. It can be seen that, for *p*-type substrate capacitors, a significant turnaround point at $V_s=-3.0$ V exists, while for *n*-type substrate capacitors the hysterisis shows gradual increase with $V_s$. These different hysteresis characteristics indicate that charge trappings during the measure-

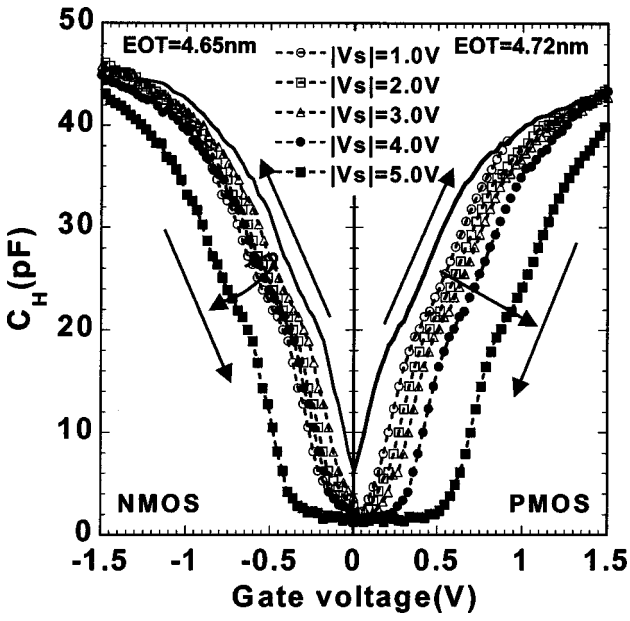


FIG. 1. $C-V$ characteristics of HfON gate dielectrics for *p*-type (NMOS) and n-type (PMOS) substrate capacitors with different sweep voltage. The hysteresis was measured by sweeping the gate voltage from 0 V to different voltage $V_s$ (solid line) and then sweeping back (dashed line).

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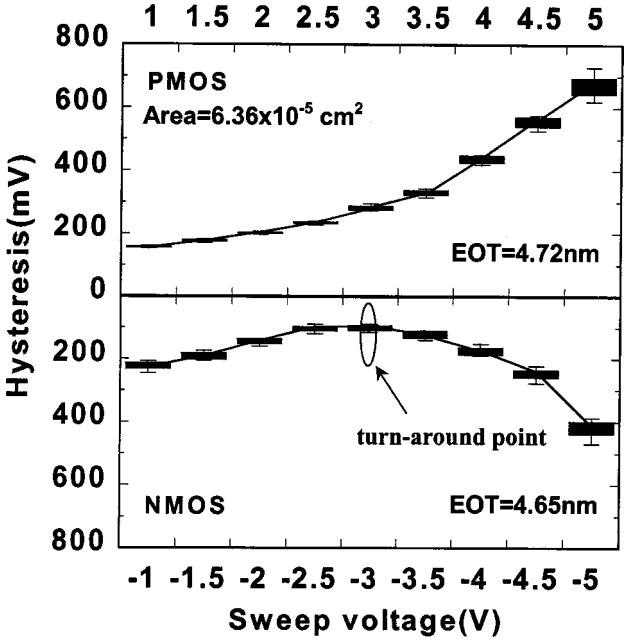


FIG. 2. Hysteresis vs sweep voltage characteristics of HfON gate dielectrics for *p*-type and *n*-type substrate MOS capacitors. Significant turnaround point at $V_s = -3.0$ V is obtained for the *p*-type substrate capacitor.

ment of *p*-type and *n*-type substrate capacitors are different.

Figure 3 shows the charge trapping characteristics of the *p*-type substrate capacitor under constant voltage stress from −2.0 to −4.2 V. The figure shows that initially the capacitor exhibited electron trappings for the stress voltage less than −3.0 V but then presented hole trappings for the stress voltage greater than −3.0 V. We can use the band diagrams of the HfON/Hf-silicate stacked structure in the inset to explain this phenomenon. When the gate was biased at the low voltage, electrons went directly through the HfON dielectrics

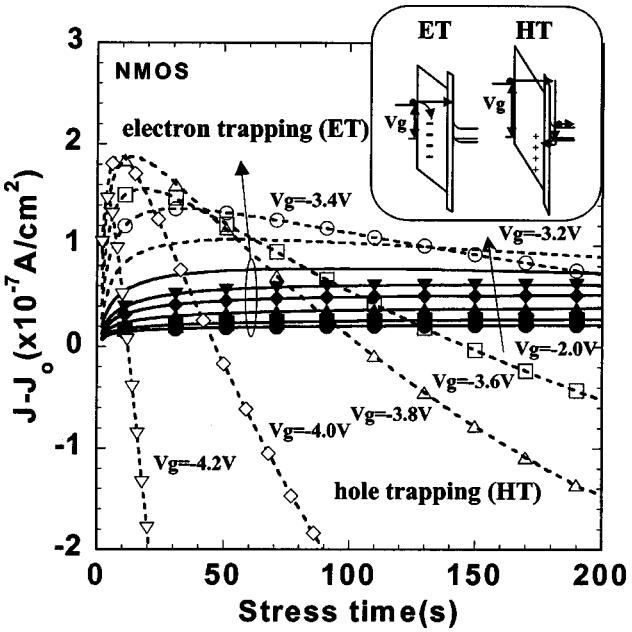


FIG. 3. Normalized gate current density vs stress time characteristics of HfON gate dielectrics for *p*-type substrate (NMOS) capacitors under constant voltage stress ranging from −2.0 to −4.2 V. The inset shows band diagrams of charge transportation for HfON/Hf-silicate stacked structure under stress.

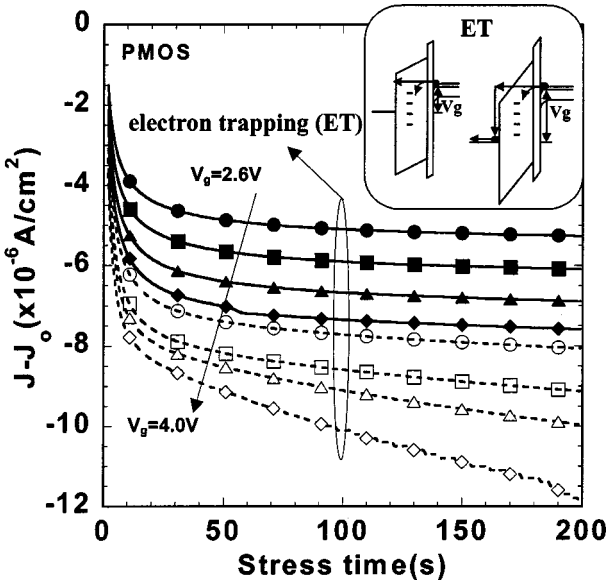


FIG. 4. Normalized gate current density vs stress time of HfON gate dielectrics for *n*-type substrate (PMOS) capacitors under constant voltage stress ranging from 2.6 to 4.0 V. The inset shows band diagrams of charge transportation for HfON/Hf-silicate stacked structure under stress.

and were trapped in the dielectric film. However, as the gate bias was increased, impact ionization might occur ($E_{ox} > 6.45$ MV/cm) which generated electron hole pairs and the holes were back trapped in the HfON dielectrics and/or at the Hf-silicate interface. This led to the hole trapping characteristics in Fig. 3. Figure 4 shows the charge trapping characteristics of the *n*-type substrate capacitor under constant voltage stress over the range of 2.6–4.0 V. Only electron trappings are observed for all the stress voltages. Similar band diagrams of the *n*-type substrate capacitor in the inset can explain this phenomenon. For this case, no impact ionization could occur since electrons went to the gate (TaN) instead of the substrate and no holes were generated as in the previous case.

In this letter, a turnaround phenomenon of the hysteresis for the HfON gate dielectrics treated by the postdeposition $NH_3$ plasma is reported. The turnaround phenomenon is explained by the initial electron trapping at the low electric field and then the hole trapping resulted from the impact ionization at the high electric field in the hafnium oxynitride dielectrics.

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