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Short Communication

High speed performance of 850 nm silicon-implanted AlGaAs/GaAs vertical cavity emitting lasers

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Abstract

In this paper, we report a high speed performance of silicon-implanted vertical surface emitting lasers (VCSELs) with the aperture size 6×6 μm^2. These VCSELs exhibit kink-free current–light output with threshold currents ~1.14 mA, and the slope efficiencies ~0.5 W/A. The eye diagram of VCSEL operating at 10 Gb/s with 6 mA bias and 6 dB extinction ratio shows very clean eye. The rise time is 29 ps and fall time is 41 ps with jitter (p–p) = 21 ps. We have accumulated life test data up to 1000 h at 70 °C/10 mA.

Keywords: VCSEL; Si implant; Implantation-induced disorder; High speed

1. Introduction

Eight hundred and fifty nanometer vertical surface emitting lasers (VCSEL) have became a standard technology for application in local area networks (LANs) [1,2]. The main advantages of VCSELs are the low threshold current, low divergent angle, and circular beam, which lead to simpler packaging and low electrical power consumption. The surface emission from the VCSELs also makes easy the 2-dimensional array integration and allows wafer level testing, in turns leading to low fabrication cost. In addition, the VCSEL's small active volume and high efficiency result in an inherently high modulation bandwidth over a wide temperature range. To date, only two commercial VCSELs are available: proton-implanted VCSEL and oxide-confined VCSEL. Proton-implanted VCSEL has been demonstrated with good reliability and decent modulation speed up to 1.25 Gb/s [1]. However, kink in current versus light output (*L*–*I*) has been always an issue in the gain-guided proton-implant VCSEL [2]. The jitter and noise performance of proton-implanted VCSEL made it difficult to meet 2.5 Gb/s (OC-48) requirement. Compared to proton-implanted VCSEL, oxide confined VCSEL provides better electrical confinement and optical index-guiding which give stable transverse modes and clean current versus light output [3]. Therefore, with lower threshold currents and reduced noise, oxide VCSEL can be used for communication of 2.125 Gb/s and above. However, there are several manufacturing concerns for the oxide VCSEL. First, it is difficult to control the aperture sizes since the oxidation procedure depend strongly on numerous material and processing parameters which can easily and unpredictably changed. In addition, the strain and defects introduced by the oxide layer could cause potential reliability problem [4]. Impurity-induced layer disordering (IILD) has broad and growing use in optoelectronics (lasers, waveguides, etc.), particularly for III–V systems employing Al and Ga. During the disordering process, a coarser layered III–V "alloy" transforms to a smoother stochastic alloy, and higher bandgap, which is capable of forming, as desired, regions that confine carriers and photons [5]. In previous work, we demonstrated a kink free operation of 850 nm AlGaAs/GaAs VCSEL using silicon

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implantation-induced disordering with exceptional reliable performance [6]. In this paper, we demonstrated the high speed performance of 850 nm AlGaAs/GaAs silicon-implanted VCSELs. The lifetime tests of these VCSELs were also performed.

2. Device structure and fabrication

The device schematic is shown in Fig. 1. First, a n-type 35-period-$Al_{0.15}Ga_{0.85}As/Al_{0.9}Ga_{0.1}As$ distributed Bragg reflectors (DBRs) were grown on an semi-insulating GaAs(1 0 0) substrate by metal organic chemical vapor deposition (MOCVD) with the growth temperature equal to 750 °C. Then, a three-quantum-well active region ($Al_{0.26}Ga_{0.74}As/GaAs$) was routinely grown, followed by the growth of 3-period $Al_{0.15}Ga_{0.85}As/Al_{0.9}Ga_{0.1}As$ p-type mirrors and a 5 nm thin GaAs layer. Then the 6×6 μm^2 emitting aperture was defined using silicon implantation. The implantation dose is 5×10^{14} cm^{-3} with the energy 90 keV. The whole structures were finished by subsequent MOCVD re-growth of p-type 22-period-$Al_{0.15}Ga_{0.85}As/Al_{0.9}Ga_{0.1}As$ DBRs and cap layer. After re-growth, mirror-like surface were obtained under microscope indicating good re-growth. During the MOCVD re-growth, the Si implantation region was annealed and induced disordering. A SEM picture of finished device is shown in Fig. 2.

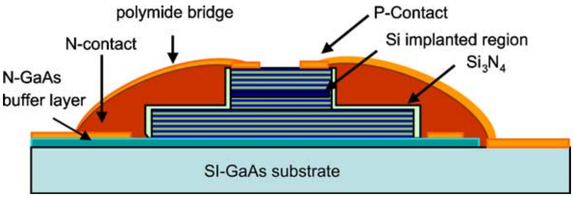

Fig. 1. Schematic diagram of the 850-nm silicon-implanted VCSEL.

3. Results and discussion

Fig. 3 shows the typical Si (6×6 μm)-implant VCSEL light output and voltage versus current (LIV) curves at 20 and 80 °C. This VCSEL exhibits kink-free current–light output performance with threshold current ~1.14 mA, and the slope efficiencies ~0.5 W/A. Using 15 nm offset between cavity resonant and gain peak, the threshold current change with temperature is less than 0.2–0.96 mA and the slope efficiency drops less than ~25 to ~0.375 W/A when the substrate temperature is raised from 20 to 80 °C. This is superior to the proton-implanted VCSEL with similar size and is comparable to that of oxide-confined VCSEL. In addition, more than 90% series resistance of the VCSELs is within 90–95 Ω indicating good re-growth interface. Typically our 10 Gb/s VCSELs have I_{th} ~1 mA, operating current ~6 mA and operation voltage is ~2.2 V. The resistance of our VCSELs is ~95 Ω and capacitance is ~0.1 pF. As a result, the devices are limited by the parasitics to a frequency of approximately 15 GHz.

To measure the high speed characteristics under large signal modulation, microwave probes and lightwave probes were used in conjunction with a 10 Gb/s pattern generator and a 12-GHz photoreceiver. The eye diagrams were taken for back-to-back (BTB) transmission on Si-implanted VCSEL on SMA submount. As shown in Fig. 4 the room temperature eye diagram of our VCSEL biased at 6 mA with data up to 10 Gb/s and 6 dB extinction ratio has a clear open eye pattern indicating good performance of these VCSELs. The rise time T_r is 29 ps and fall time T_f is 41 ps with jitter (p–p) = 21 ps. This confirms again the superior performance of silicon-implanted VCSEL.

The guarantee the device reliability is always a tough work but a natural task for the components supplier in the data communication markets. We have accumulated life test data up to 1000 h at 70 °C/10 mA with exceptional reliability. As shown in Fig. 5 is the light output

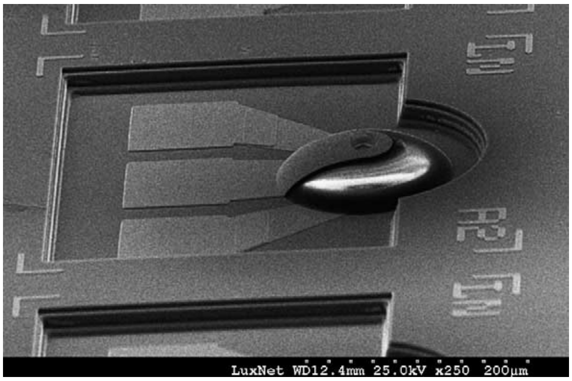

Fig. 2. SEM picture of the 850-nm silicon-implanted VCSEL.

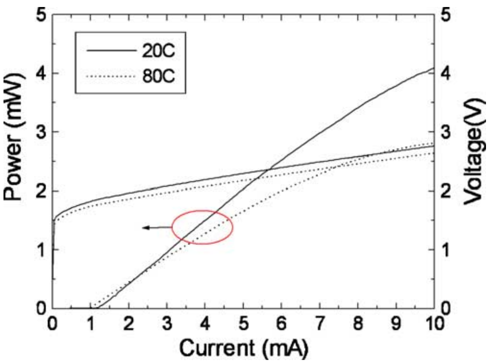

Fig. 3. Power and voltage versus current curves at 20 and 80 °C.

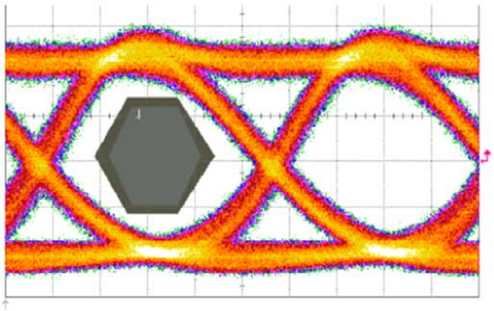

Fig. 4. Eye diagram generated by a 10 Gb/s digital modulation of a silicon-implanted VCSEL biased at 6 mA.

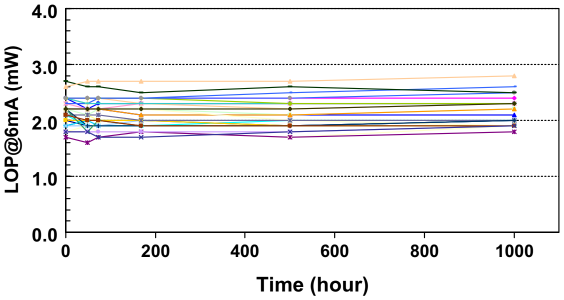

Fig. 5. Life test results of Si-implant VCSEL devices (70 °C/10 mA).

versus time scale for VCSEL chips under HTOL (70 °C/10 mA) test, none of them shows the abnormal behavior.

4. Summary

In conclusion, we report a high speed performance of silicon-implanted VCSELs with the aperture size 6×6 μm^2). These VCSELs exhibit kink-free current–light output with threshold currents $\sim$1.14 mA, and the slope efficiencies $\sim$0.5 W/A. The wide open eye pattern up to 10 Gb/s indicates good performance of our VCSEL which can be attributed to our kink-free *L–I* performance. We have accumulated life test data up to 1000 h at 70 °C/10 mA. All of these advantages—kink-free *L–I*, high speed performance and good reliability make the novel VCSEL promising in the optoelectronic and other commercial applications in the coming days.

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