An Interleaving Energy-Conservation Mode (IECM) Control in Single-Inductor Dual-Output (SIDO) Step-Down Converters with 91% Peak Efficiency

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Abstract

This interleaving energy-conservation mode control for single-inductor dual-output converter uses the superposition technique to yield the optimal average inductor current and 91% peak efficiency. Neither a freewheel stage nor a post-regulator is needed at nominal conditions. The output voltage ripple appears notably minimized over 50% by means of current interleaving at full load. The chip occupies 1.44 mm^2 in 65 nm CMOS and integrates with a 3D architecture for ultra-wide band system.

I. Introduction

For battery-operated mobile systems, it is imperative that a power integrated chip simultaneously contains high efficiency, satisfactory regulation, small volume and robustness. These characteristics are essential in ultra-wide band (UWB) applications, such as the wireless universal serial bus (USB) that has the advantage of speed over other wireless technologies. The single-inductor dual-output (SIDO) converter has the capabilities to provide two high-quality outputs for different function blocks and to reduce the size of footprint area by single inductor. The pseudo-CCM/DCM control [1] in SIDO converters experiences an extra conduction loss due to the high average inductor current level that guarantees the existence of a freewheel stage, which occupies most switching period and results in a large conduction loss at light loads. The comparator-controlled outputs in [2-3] improve the efficiency but sacrifice the regulation performance, which needs to be redeemed by a post-regulator. The converter, with a minimized number of switches, can also improve efficiency [4], but the flexibility is reduced since the outputs must include at least a step-up output to release the inductor current [5]. The proposed SIDO converter with an interleaving energy-conservation mode (IECM) control can improve efficiency and provide two low-ripple step-down outputs with a compact 3D package at the same time.

II. The Behavior of the Proposed IECM Control

Fig. 1 shows the architecture of the proposed SIDO converter with IECM control. The power stage is composed of four power switches, M_{S1}-M_{S4}, for dual step-down outputs to power UWB system with default value of 1.8 V and 1.2 V, respectively. The ECM controller can lower the average inductor current and allow it to be exactly equal to the summation of two output load current for a large reduction in conduction loss. The current balance controller can effectively minimize the output voltage ripple and ESR effect when a current interleaving mechanism is adapted.

A. Energy-conservation mode (ECM) operation

ECM operation depicted in Fig.2 is used enhance efficiency of SIDO converter for supporting multiple low-power modes in UWB system especially the standby and hibernate modes. The time diagram illustrates the inductor charging period of Path-I and Path-III and the discharging period of Path-II and Path-IV. The peak inductor current in each switching cycle is decided by the superposition of the two error signals feedback from the outputs. Aside from this, the swapping from either Path-I to Path-III or Path-IV to Path-II is determined by the error signal I_{EA}. Consequently, the average inductor current of ECM operation, I_{L,avg_ECM}, will be equal to the summation of the two output loads and is lower than that of the pseudo-CCM (PCCM) control, I_{L,avg_PCCM}. That is, the ECM operation would yield a low average inductor current level without the freewheel stage, so as to reduce the conduction loss and enhance the efficiency. Moreover, the output voltage ripple can be reduced through the optimized average inductor current level.

B. Current interleaving mechanism

To further enhance heavy load performance, current interleaving mechanism is utilized with ECM operation for IECM control in Fig.3. The interconnections of the SIDO modules through the control signals of V_{s_i}, V_{s_o}, V_{clk_i}, and V_{clk_o} constitute a power management function for UWB system. Single-phase operation works in multiple low-power modes. Meanwhile, dual-phase operation is set to provide large energy during data transmission. The output voltage ripple can be greatly minimized due to the continuous inductor current by means of current interleaving. The glitches carried out by the ESR can also be cancelled.

III. Circuit Implementation of the IECM Controller

IECM controller contains the ECM controller and the current balance controller depicted in Fig. 4.

A. ECM controller circuit

In ECM controller circuit, I_{EA} and I_{EB} are the error signals from the two outputs. The I_{EAB} is the summation of I_{EA} and I_{EB}. V_{slope} is added to the current sensing signal V_{s_i} to avoid sub-harmonic oscillation, and that generates the summation signal I_{SUM} through a voltage-to-current (V-I) converter. The I_{SUM} intersects I_{EA} and I_{EAB} can determine the energy delivery paths, Path-I ~ Path-IV.

B. Current balance controller circuit

The full-range current sensing circuit helps to decide the duration of the four paths. Transistors M_{Sp} and M_{Sn} can sense the current flowing through the switches M_{S1} and M_{S2} to generate a current sensing signal, V_{s_i}. The low-pass filter in the current adjusting circuit obtains I_{L,avg_ECM} in the SIDO module and generates the adjusting current I_{adj} to modulate I_{EAB} in order to achieve current balance. That is, a precise current matching is automatically derived when the IECM control is activated.

IV. Experimental Results

This proposed SIDO module with the IECM control was fabricated by 65nm CMOS process. Fig. 5 shows the waveform of single-phase operation. The energy delivery sequence of Path-I to Path-IV is verified and the average inductor current is continuously kept equal to the summation of the two output loads. In Fig. 6, the waveform indicates the power management integration of the IECM control with a demand of load arising. The output voltage ripple is greatly reduced and the voltage spike due to ESR effect is nearly eliminated with the dual-phase operation of current interleaving.

Fig. 7 shows the 3D package and the chip micrograph. The staked spiral inductor is placed on top of the power management IC to shorten the distance of the bounding wire. The performance can be enhanced through the alleviation of the bound wire effect. Fig. 8 shows efficiency and the output voltage ripple with different loads. The conduction loss of the power switches can be greatly reduced through ECM operation. The peak efficiency is raised to 91%, where the 80% efficiency is achieved by the commercial products with four power switches. In addition, the output voltage ripple is largely decreased by 36% as compared to the PCCM control. Specifically, a 50% reduction in the output ripple is presented at heavy loads owing to the IECM control of current interleaving. The design specifications are depicted in Table I.

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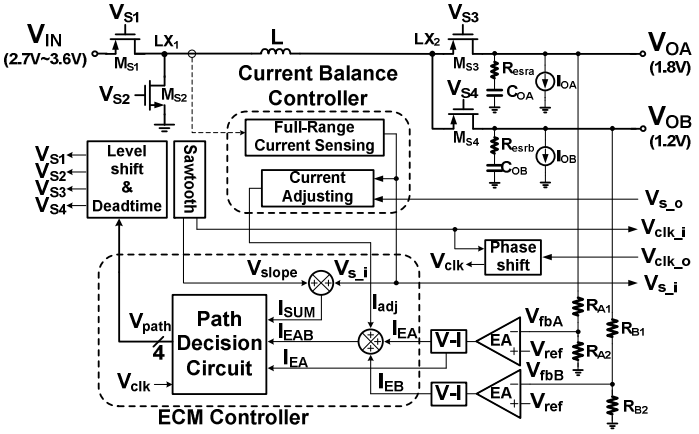

Fig. 1. Block diagram of the proposed SIDO module with IECM control.

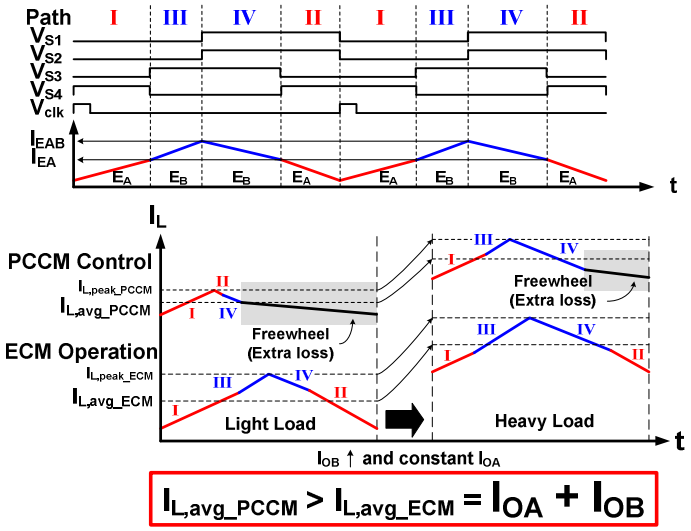

Fig. 2. The methodology and time diagram of the ECM operation.

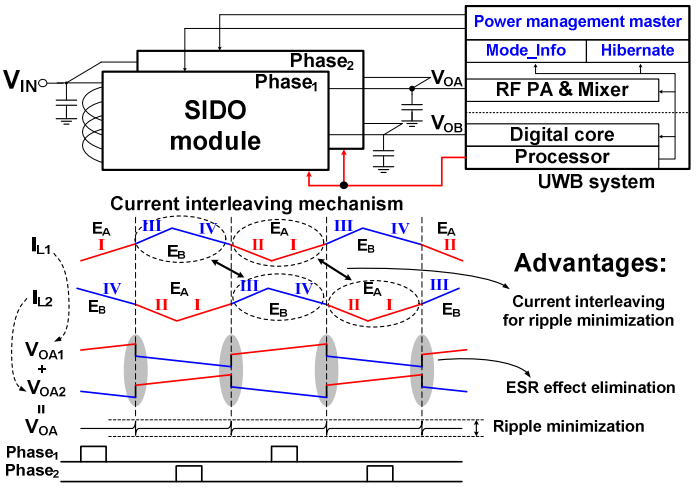

Fig. 3. Current interleaving mechanism of IECM control for UWB.

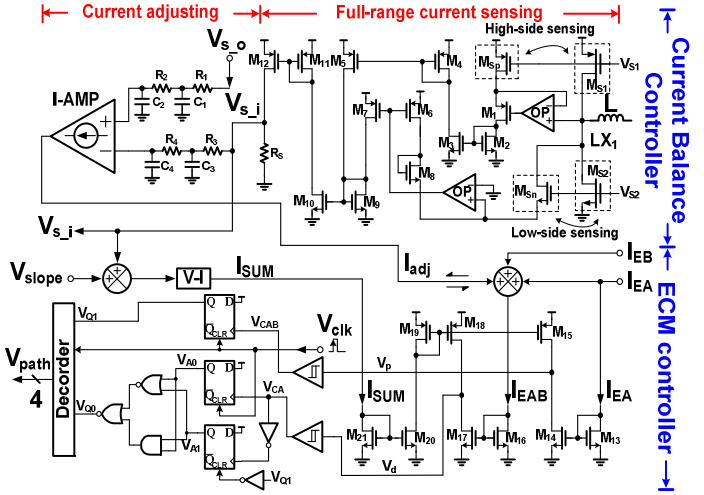

Fig. 4. Circuit implementation of the IECM controller.

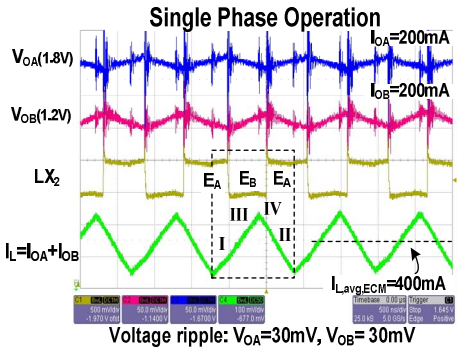

Fig. 5. Measured single phase operation.

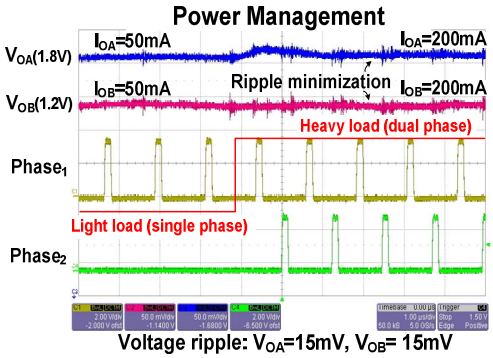

Fig. 6. Measured power management integration.

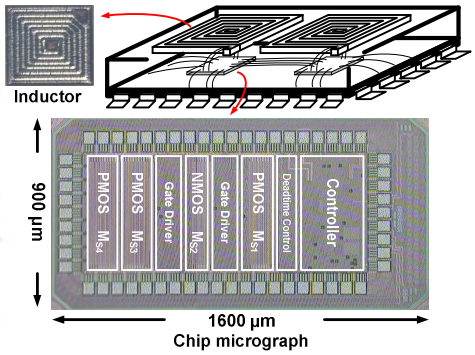

Fig. 7. Chip micrograph and 3D integration.

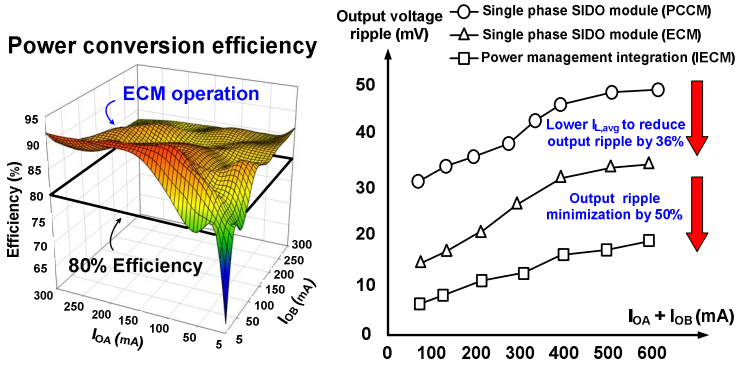

Fig. 8. Measured power conversion efficiency and output voltage ripple.

TABLE I: DESIGN SPECIFICATION OF THE PROPOSED SIDO MODULE

Process	**65nm 1P7M CMOS process**	
Input voltage	**2.7 V ~ 3.6 V**	
Inductor / DCR	**4.7 µH / 250 mΩ (nominal)**	
Switching frequency	**1 MHz (nominal)**	
Chip side (SIDO module)	**1600 µm x 900 µm**	
Outputs	**V_{OA} = 1.8 V**	**V_{OB} = 1.2 V**
Output capacitor / ESR	**4.7 µF / 30 mΩ**	**4.7 µF / 30 mΩ**
Cross Regulation	**100 mA → 300 mA** **300 mA → 100 mA**	**10 mV** **8 mV**
	12 mV **15 mV**	**100 mA → 300 mA** **300 mA → 100 mA**
Output ripple (single phase)	**< 32 mV**	
Output ripple (dual phase)	**< 16 mV**	