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Generally Applicable Self-Masked Dry Etching Technique for Nanotip Array Fabrication

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ABSTRACT

Well-aligned nanotip arrays were fabricated by electron cyclotron resonance (ECR) plasma process using gas mixtures of silane, methane, argon, and hydrogen. The resultant tips have nanoscale apexes (∼1 nm) with high aspect ratios (∼50), which were achieved by simultaneous SiC nanomask formation and dry etching during ECR plasma process. This technique was applied to a variety of substrates such as silicon, polycrystalline silicon, gallium nitride, gallium phosphide, sapphire, and aluminum, indicating its general applicability. High-resolution transmission electron microscopy and Auger depth profile analyses revealed that the SiC cap, with Si:C ratio of 1:1, exhibited 3C–SiC and 2H–SiC structure on Si and GaP, respectively, with heteroepitaxial relationship. This one-step self-masked dry etching technique enables the fabrication of uniform nanotip arrays on various substrates over large area at low process temperatures, thereby demonstrating a high potential for practical industrial application.

Nanoscaled tips have been demonstrating their unique usefulness in different applications such as high-efficiency field emission,[1] near-field optical microscopy,[2,3] high-resolution atomic force microscopy and atomic-resolution scanning tunneling microscopy.[4−6] Sharper tip (i.e., smaller apex of the tip) gives stronger field enhancement for increased field emission current[7] and better spatial resolution in scanning probe microscopy.[8,9] Currently, field emission from micro- and nanotips as well as other one-dimensional nanomaterials have been widely investigated.[10−14] Optimum field emission performance can be obtained by adjusting the size and spacing of the tips or nanostructures so as to maximize the enhancement of the local electric field of individual emitter and the collective emission current from an ensemble of emitters.[15−17] In addition to the applications mentioned above, nanotips are being explored for different purposes in solar cells,[18] optoelectronics[19,20] and bio/chemical sensing devices.[21−23] However, a number of crucial technological hurdles block the way for actual realization of these developmental works. Those include uncontrolled growth of nanotips and incompatibility of the nanofabrication process with the well-established silicon process technology. Accordingly, an efficient nanofabrication process capable of delivering tip morphologies over large areas and on varied substrates and still compatible with existing process technologies will significantly advance research in nanotechnology.

Until now, optical lithography has been playing the major role in fabricating sharp tips but limited to ∼50 nm in radius.[2,11,12] Electron-beam or focused-ion-beam lithography can produce tips with smaller radius. However nanolithography has the physical limitation in tip radius[24] typically about 15 nm, based on Rayleigh criteria. Dry etching of the substrates pretreated with heterogeneous nanomasks is one of the efficient techniques for nanofabrication. Whether in reactive ion etching (RIE) of substrates such as GaN[25] or Si,[26] or in Ar ion beam sputtering of substrates (e.g., Si),[27] nanomask fabrication poses the main challenge toward obtaining nanotips. Nevertheless, the aforementioned processes can be applied successfully only to certain limited substrates.

In this paper, we report a one-step and self-masked dry etching (SMDE) technique for fabricating uniform and high-

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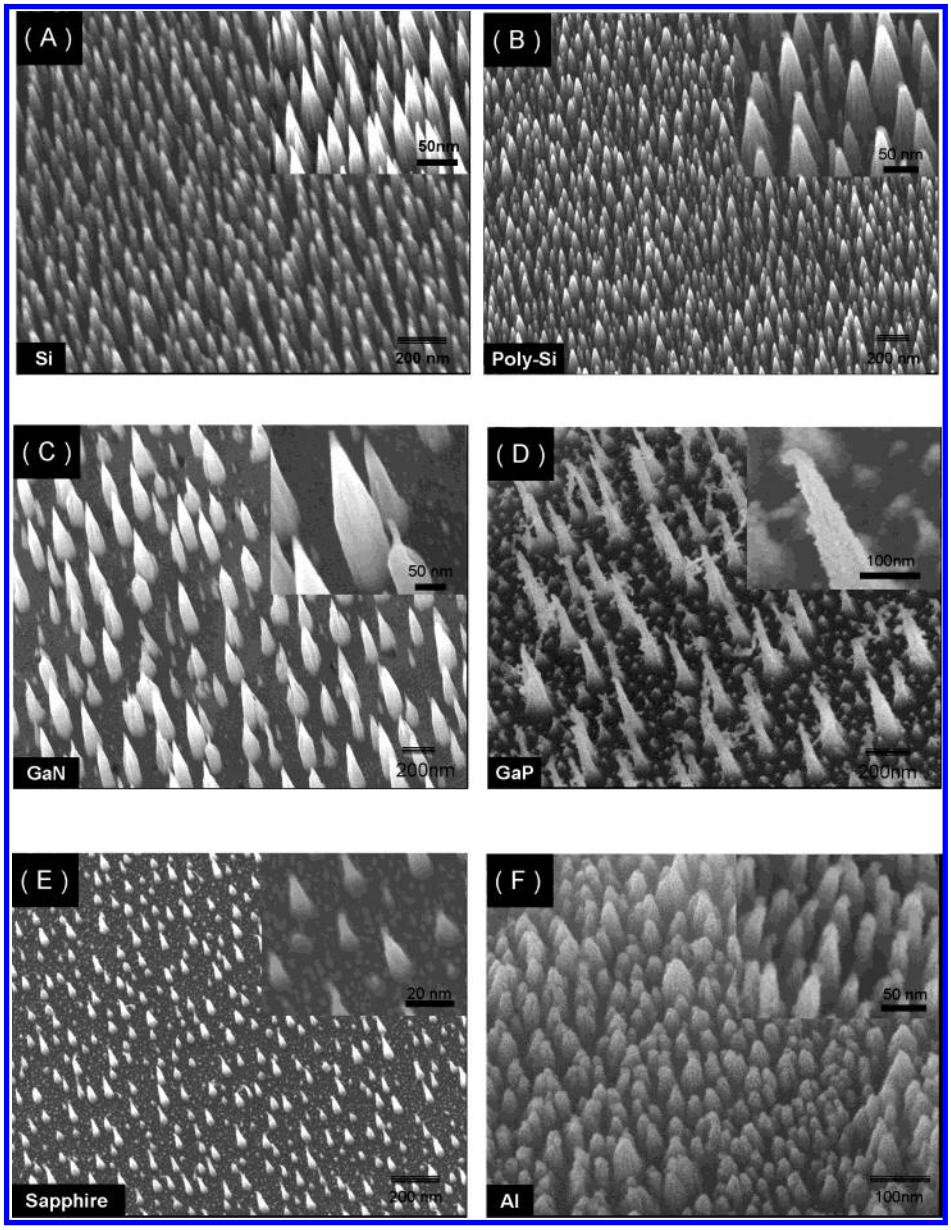

Figure 1. Tilted top-view HRSEM morphologies of the nanotip arrays fabricated by the self-masked process of various substrates: (A) single-crystal silicon (Si); (B) polycrystalline silicon (poly-Si); (C) epitaxial gallium nitride (GaN) film on sapphire; (D) single-crystal gallium phosphide (GaP); (E) sapphire; and (F) aluminum. The insets show their corresponding magnified images.

density nanotip arrays over a large area in a cost-effective manner, using a Seki high-density electron cyclotron resonance (ECR) plasma reactor. The pre-cleaning of the substrate by hydrogen (H_2) plasma, followed by simultaneous process of self-masking and reactive etching of the unmasked area for nanotip formation, was done in the reaction chamber in one step and without interrupting the vacuum. Reactive gases comprising of argon (Ar), H_2, methane (CH_4), and silane (SiH_4) (10%, diluted in helium) with typical flow rates of 3, 8, 2, and 0.2 sccm, respectively, were activated by a microwave power of typically 1200 W at a chamber pressure of 5.8 mTorr, during the nanotip fabrication process. Nanotip arrays were etched out from a variety of substrates maintained at a temperature between 100 °C to 250 °C, as measured by a two-color optical pyrometer.

Figure 1 shows the tilted top-view high-resolution scanning electron microscope (HRSEM) images of nanotip arrays formed by the SMDE technique on various substrates, e.g., single-crystal silicon (Si), polycrystalline silicon (poly-Si), gallium nitride (GaN), gallium phosphide (GaP), sapphire, and aluminum (Al). Nanotips were found to be well aligned and uniformly distributed over the entire surface with a high density for all the samples. In case of single crystalline 6 in. Si wafers, Si nanotip density as high as $1.5 \times 10^{11}/cm^2$ was obtained with a high aspect ratio of ~50. Similar geometric features of the nanotips as observed on all substrates with different crystal orientation, as demonstrated in Figure 1, suggest no orientation dependence of the etching process involved and recognizes a general applicability of the SMDE process in the field of nanotip fabrication, apart from its simplicity and compact process steps.

Further structural investigation was carried out by using high-resolution transmission electron microscope (HRTEM). Typical HRTEM images of the nanotips of crystalline silicon

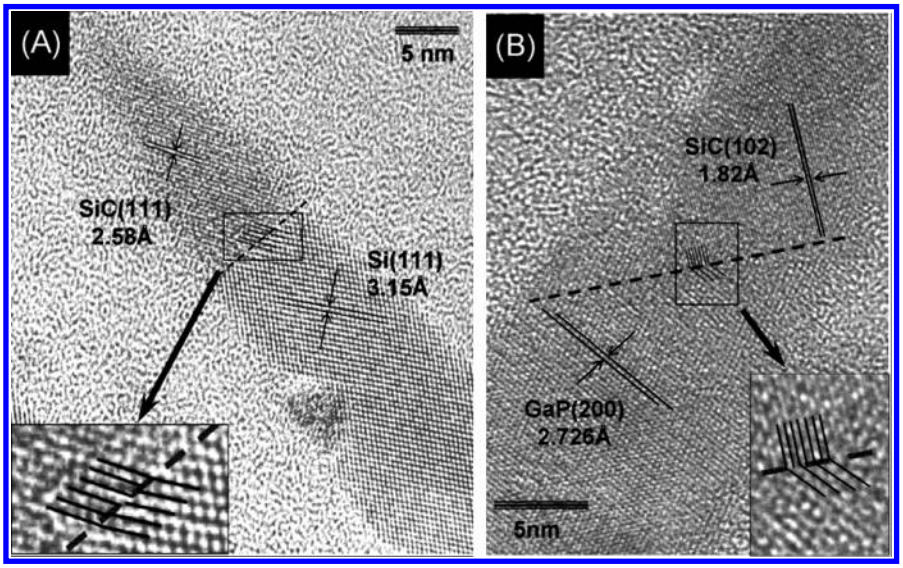

Figure 2. (A) HRTEM image of the Si nanotip revealing a SiC cap formed on top of the tip. Inset shows the magnified HRTEM image of the interface between Si and SiC cap on which the lattice mismatch of Si/SiC = 4:5 can be observed. (B) HRTEM image of the GaP nanotip with SiC cap also formed on the tip. Inset shows the magnified HRTEM image of the interface between GaP and SiC cap on which the lattice mismatch of GaP/SiC = 1:2 can be observed.

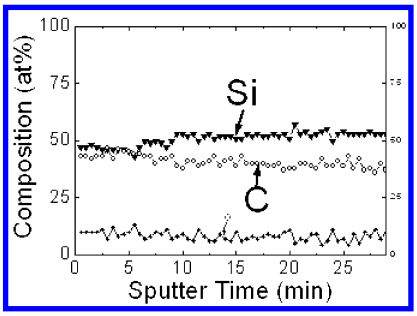

Figure 3. High-resolution Auger depth profile at the top of the nanotip showing the composition of the cap to be Si/C = 1:1.

and GaP are shown in Figure 2A and Figure 2B, respectively. In both cases, ~1 nm apex radius of the tip was obtained, which can be compared favorably to the finest tip reported so far. More interestingly, a cap has been identified at the top of the tip with lattice spacing different from that of the body of the tip. Figure 2A shows the Si nanotip substrate with a lattice spacing of 3.15 Å and the cap with a lattice spacing of 2.58 Å, which is close (2.38% deviation) to the literature data of 2.51 Å for (111) *d* spacing of 3C−SiC.[28] HRTEM study of the GaP nanotips sample revealed a similar cap structure. As shown in Figure 2B, the cubic GaP structure exhibits a (200) lattice spacing of 2.726 Å at the bottom of the tip, whereas the cap exhibits a lattice spacing of 1.82 Å, which is close to (0.55% deviation) the literature data of 1.83 Å for (102) *d* spacing of 2H−SiC.[29]

To confirm this, a high resolution Auger depth profile was performed on the cap and a Si/C = 1:1 stoichiometry was identified from the composition data presented in Figure 3. Accordingly, the formation of a SiC cap, acting as the nanomask, is believed to be instrumental in the fabrication of the nanotip arrays not only for Si but also for non-Si substrates. The dashed lines in the inset of Figure 2A and 2B indicate the interface between SiC cap and etched substrates. It appears that the SiC caps were formed on Si and GaP substrates in a "heteroepitaxial" manner. A lattice matching relationship of 4:5 with a 5° angle for Si and SiC (or 1:2 with 41° angle for GaP and SiC) was observed.

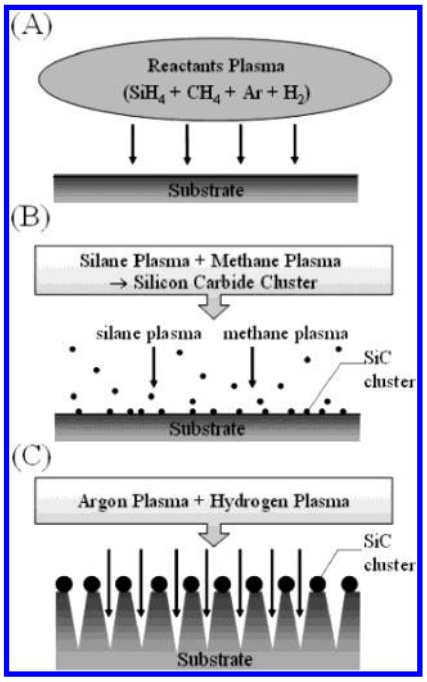

Figure 4. Schematic diagram for the nanotip formation: (A) the reactive gases are composed of silane, methane, argon, and hydrogen; (B) the SiC nanosized clusters are formed from the reaction of SiH_4 and CH_4 plasma and uniformly distributed on the substrate surface; and (C) the unmasked region is etched by Ar and H_2 plasma, whereas the region masked by SiC caps protects the substrate from etching, and hence creates the conical tips.

Figure 4 illustrates the schematic description of the nanotip formation. The gas-mixture consisting of SiH_4, CH_4, Ar, and H_2 present in the ECR plasma is supposed to react and play two different roles: formation of SiC nanomasks and etching of the substrate to develop nanotips (Figure 4A). It is believed

that in the ECR plasma, SiC nanosized clusters are formed from the reaction of SiH_4 and CH_4 plasma[30] and uniformly distribute themselves over the substrate surface (Figure 4B). Meanwhile, Ar and H_2 plasma are responsible for the physical etching and chemical etching, respectively, of the substrates. The SiC nanoclusters deposited on the substrate then act as nanomasks against etching, because of their higher hardness and chemical inertness. Under the protection of a high density of SiC caps, formation of high density and high aspect ratio nanotip arrays can be realized (Figure 4C).

This one-step approach, promoting the occurrence of SiC ("bottom up") and dry etching of substrates ("top down"), enables the fabrication of various nanotips without choosing a specific substrate or pretreating with a specific heterogeneous etching resistant as used in conventional methods. Studies that use masks developed by pretreating the substrates have no control on the size of the masks grown. In comparison, the SMDE process possesses a control on the size and density of the SiC clusters simply via the process parameters of the high-density plasma environment, such as process temperature, gas pressure, and composition, which translates into crucial control of the tip morphologies and densities. For example, the high-temperature environment favors the formation of SiC masks at such high densities so as to cover the entire substrate surface inhibiting the nanotip formation. Such detailed dependence of morphology on experimental conditions will be discussed in a separate paper.

The mechanism underlying the self-assembly of nanomasks is unclear, however, symmetry and lattice mismatch between the substrate and the mask material are likely to play a role.[31] After the simultaneous formation of SiC nanoclusters and etch-active reagents in the plasma, self-organization of nanomasks appears to be a concerted process involving both the substrate and the mask; their lattice mismatch of different dimensions may lead to the differences in the geometrical features of nanotips, including their surface density, while preparing nanotips using different substrates.

We would like to pay special emphasis to the applicability of the SMDE technique to a series of materials. The slight difference in morphology of post-etching structures on different materials is in fact a drawback for all etching processes. In SMDE technique, we have a combination of physical and chemical dry etching process. The resultant shape would be affected by the inherent difference in physical hardness and chemical reactivity of the substrate with the plasma. Consequently, we successfully combined photolithography with SMDE technique to form silicon nitride patterned arrays of nanotips as shown in Figure 5, which demonstrated the potential of the SMDE technique in device applications.

Quantum confinement effects in Si as well as compound semiconductors arising from reduction in dimensions have been widely investigated.[32−35] The study of the optoelectronic properties of these nanotips relative to their bulk counterparts is ongoing and will be reported in a separate paper. The field emission property of such sharp nanotip arrays in a simple diode structure reveals an ultralow turn-on field (defined as the field at which an emission current density of 10 μA/cm^2 is obtained) of 0.35 V/μm.[36] Further studies on gate-controlled field emission devices such as that shown in Figure 5 is underway. Meanwhile, we have applied our nanotips as a template for metallic nanoparticulate growth for surface-enhanced Raman scattering (SERS) study, and an enhancement factor as high as 10^6-10^8 for Rhodamine 6G was observed.[37]

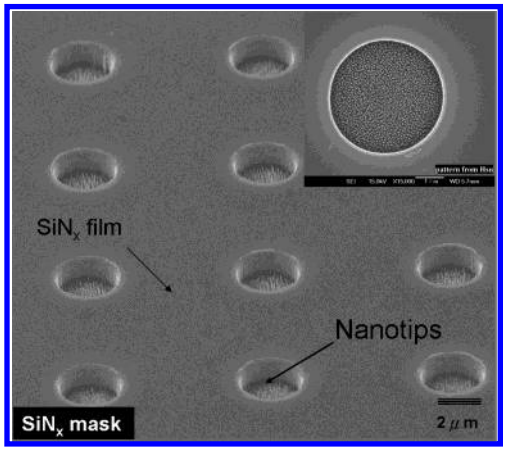

Figure 5. Patterned arrays of naotips generated by photolithography process using silicon nitride as the etching resistant.

In conclusion, the fabrication of uniform nanotips on various substrates over large area at low temperatures has been demonstrated by this in-situ SMDE technique. The advantages of this technique lie in the relative process simplicity, general applicability in a number of semiconductors and metals, and compatibility with well-established semiconductor processes.

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