A Dual-Gate-Controlled Single-Electron Transistor Using Self-Aligned Polysilicon Sidewall Spacer Gates on Silicon-on-Insulator Nanowire

Shu-Fen Hu, Yung-Chun Wu, Chin-Lung Sung, Chun-Yen Chang, *Member, IEEE*, and Tiao-Yuan Huang, *Fellow, IEEE*

***Abstract*—A dual-gate-controlled single-electron transistor was fabricated by using self-aligned polysilicon sidewall spacer gates on a silicon-on-insulator nanowire. The quantum dot formed by the electric field effect of the dual-gate structure was miniaturized to smaller than the state-of-the-art feature size, through a combination of electron beam lithography, oxidation, and polysilicon sidewall spacer gate formation processes. The device shows typical MOSFET *I-V* characteristics at room temperature. However, the Coulomb gap and Coulomb oscillations are clearly observed at 4 K.**

***Index Terms*—Nanotechnology, quantum dots (QD), quantum wires, silicon-on–insulator (SOI) technology.**

I. Introduction

SILICON single-electron devices are one of the potential key elements in achieving extremely low-power consumption and high-density integration for future large-scale integrated circuits (LSIs). Most silicon-based single-electron transistors (SETs) employ a naturally grown, lithographically defined single quantum dot (QD) with nanosize as the transport bridge between the source and the drain. These conventional single-QD-based SETs, however, depict poor stability in the Coulomb blockade effect due to the inevitable quantum-mechanical cotunneling process. Recently, various single-electron transistors based on silicon-on-insulator (SOI) substrate have been demonstrated. Coulomb blockade oscillation is attributed to the formation of randomly distributed Coulomb islands separated by tunnel barriers formed by the SOI substrate [1]–[12]. Matsuoka *et al.* [13] have observed the Coulomb blockade at lower temperature (100 mK) by six-QD-coupling in a Si metal-oxide-semiconductor (MOS) field-effect-transistor (FET) structure with dual gate. Park *et al.* [14] have also reported a dual-gate-controlled SET based on SOI structure that exhibited Coulomb blockade phenomena by three-QD-coupling. Such multi-QD-based SETs are conducive to more stable single-electron circuits because coupled dots are defined by independently controllable gates, which are designed to separately control the tunneling potential barriers to compensate for variations due to size fluctuation in QDs [13], [14]. Kim *et al.* [15], [16] reported an electrically induced quantum dot SET in SOI nanowire that showed Coulomb oscillation and movement of the oscillation peak in two independently controllable tunnel junctions. However, the scaling of their device, even though not limited by lithography, is limited by the controllability of chemical vapor deposition (CVD) and reactive ion etching (RIE) processes [15], [16]. Here we present our experimental work using electron-beam (e-beam) direct writing combined with oxidation to achieve thin and narrow wires on SIMOX wafers. Specifically, a dual-gate-controlled SET was successfully fabricated by self-aligned polysilicon sidewall spacer depletion gates on the SOI nanowire. The Coulomb island is determined by the thickness as well as the width of the nanowire, and its length is defined by the separation between two polysilicon sidewall spacer gates, which are formed by electron beam lithography combined with the sidewall spacer processes. The Coulomb oscillations and Coulomb staircase phenomenon by multidot coupling at low temperature are successfully demonstrated.

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S.-F. Hu and C.-L. Sung are with the National Nano Device Laboratories, Hsinchu 300, Taiwan, R.O.C. (e-mail: sfhu@ndl.gov.tw).

Y.-C. Wu is with the National Nano Device Laboratories, Hsinchu 300, Taiwan, R.O.C., and is also with the Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

C.-Y. Chang and T.-Y. Huang are with the Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

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II. Experimental

The SET in this study was fabricated using SIMOX wafers fabricated on $\langle 100 \rangle$ p-type Si substrates, with a thin 60-nm silicon layer on top of a 400-nm buried SiO_2. After depositing a 10-nm capping oxide, the top silicon layer was doped by phosphorous ion implantation at a dose of 2×10^{14} ions/cm^2 and with an energy of 40 kV. The doping results in a significant drop in the silicon sheet resistance to around $965 \sim 1118\ \Omega/\square$. Afterwards, the silicon device layer was thinned down by a sacrificial oxidation with subsequent oxide strip. E-beam direct writing, by a Leica Weprint 200 system with NEB22A e-beam resist, was then employed to define 80-nm-wide narrow lines. After pattern transfer, the 80-nm-wide silicon wires were further thinned and narrowed, and a 20-nm gate oxide was subsequently grown at 925 °C for 43 min in oxygen which served to further reduce the silicon wires' dimension. A TEOS SiO_2 layer was then deposited, patterned using e-beam lithography, and RIE etched to form TEOS narrow bar perpendicular to the nano silicon wire. To further reduce the TEOS width from 80 to 40 nm, wafers were dipped in 5% diluted HF solution for 30 s. Next, a 10-nm-thick oxide was thermally grown in dry O_2 at 800 °C for damage curing, which also formed a good quality

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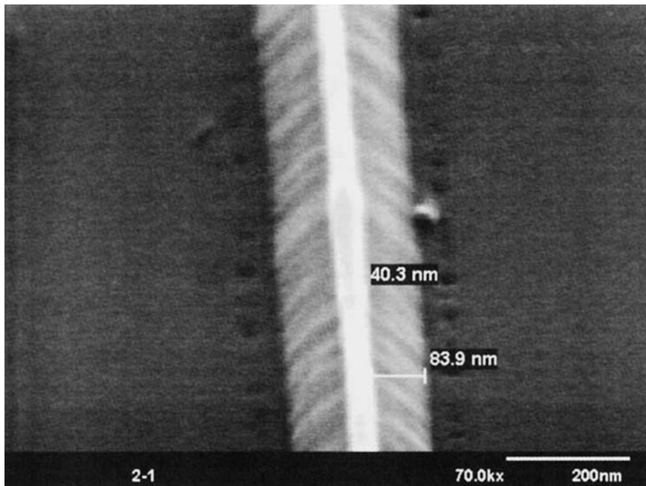

Fig. 1. Scanning electron microscopy (SEM) picture of the self-aligned polysilicon sidewall spacers abutting the narrow TEOS bar.

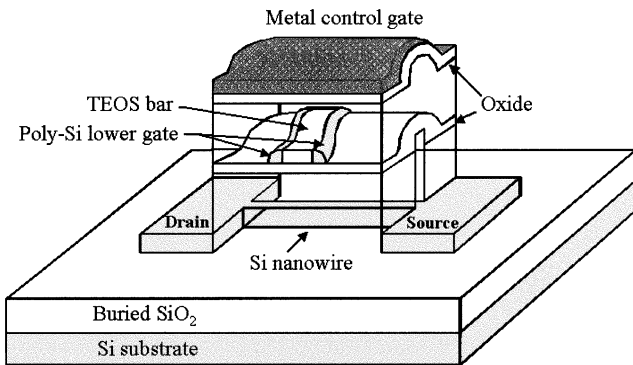

Fig. 2. Schematic diagram of the self-aligned dual-gate-controlled SET structure.

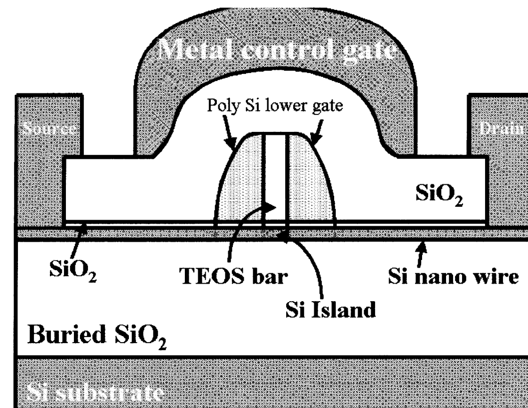

Fig. 3. Cross-sectional drawing of the self-aligned dual-gate-controlled SET.

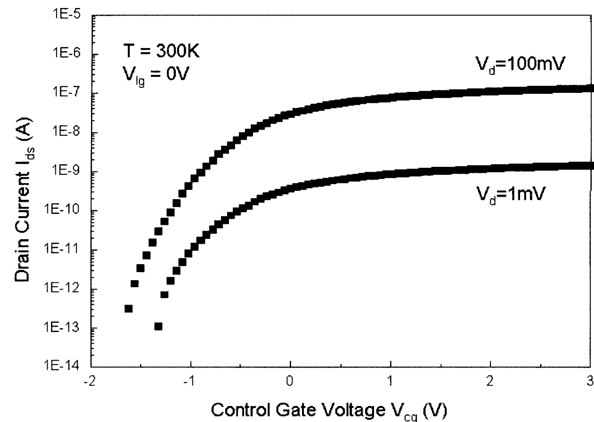

Fig. 4. Drain current versus control gate voltage measured at $\mathrm{T} = 300\ \mathrm{K}$. The source–drain biases are 1 and 100 mV.

gate oxide on the exposed nano silicon wire. The thickness of the final SOI layer is around 3 nm [7]. Afterwards, an *in-situ* n^{+}-doped 150-nm-thick polysilicon layer was deposited using LPCVD. This was followed by an RIE etching of the n^{+} poly-Si layer in Cl_2 reactive ion plasma to form self-aligned sidewall polysilicon spacers abutting the TEOS narrow bar, as shown in Fig. 1. After depositing another 110-nm-thick TEOS oxide layer and contact patterning, aluminum metal film was deposited and patterned to form the metal control gate on top of the active device area, and also to provide electrical contacts to the device. Fig. 2 shows a schematic of the fabricated dual-gate-controlled SET. The corresponding cross sectional view is shown in Fig. 3, indicating biasing electrodes and major geometric parameters. It should be noted that the two polysilicon sidewall spacers, when properly biased negatively, serve as the lower gates to induce two depletion regions in the nano silicon wire beneath the thin 10-nm gate oxide. As a result, single QD of SET operation is formed in the active channel of the nano silicon wire by negatively biasing the lower gates. The top metal control gate, positioned over the top of the two lower spacer gates, was designed to control the tunneling potential barriers to compensate for variations due to size fluctuation in QD. The thickness of the control gate oxide is 110 nm, while the thickness of the gate oxide underneath the polysilicon spacer gates is 10 nm. The width of the sidewall spacer gate is $\sim$84 nm, and the space between the two spacer gates, which is the width of the TEOS nano bar, is around 40 nm. Thus, Coulomb island with feature size smaller than that characteristic of the state-of-the-art e-beam lithography is achieved in our structure. The device characteristics were measured by an HP4156B parameter at 300 and 4.2 K in liquid helium cryogenic probing system.

III. Results and Discussion

Drain current versus control gate voltage V_{cg} measured at $\mathrm{T} = 300\ \mathrm{K}$ are shown in Fig. 4 for two drain-to-source biases of 1 and 100 mV. Typical MOSFET *I–V* characteristics were observed. The dependence of drain-to-source current on the lower gate (i.e., polysilicon spacer) voltage V_{lg} at 300 K, with the control-gate voltage as a parameter, is shown in Fig. 5. It can be seen that the drain current I_{d} decreases rapidly with decreasing V_{lg}. This feature is indicative of the formation of an electrostatic tunneling potential barrier below the polysilicon spacer gate, and the creation of nano-size quantum dots on the wire channel, thus cutting off the channel current. I_{d} is cut off at various cutoff voltages (V_{lg}) of 0.2 V, -1.3 V and -1.6 V for different control-gate voltages (V_{cg}) of -1 V, 1 V, and 3 V, respectively. The shift of the cutoff voltage to more negative value with increasing control-gate voltage implies that the cutoff is likely due to the

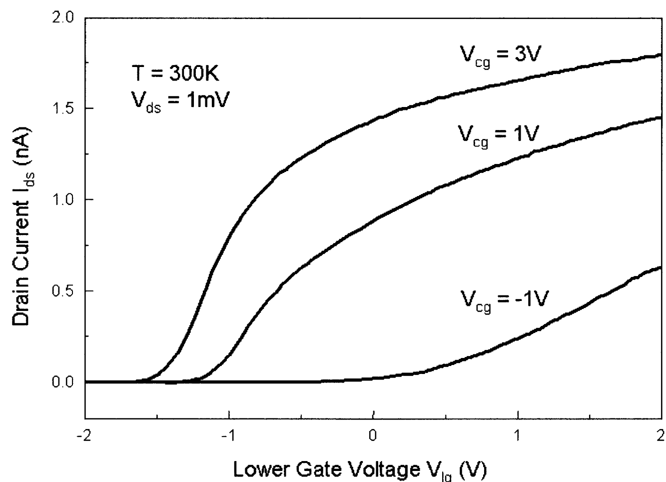

Fig. 5. Measured $I_d - V_{lg}$ characteristics at $V_{ds} = 1$ mV and $T = 300$ K with various control gate voltage of -0.1, 1, and 3 V.

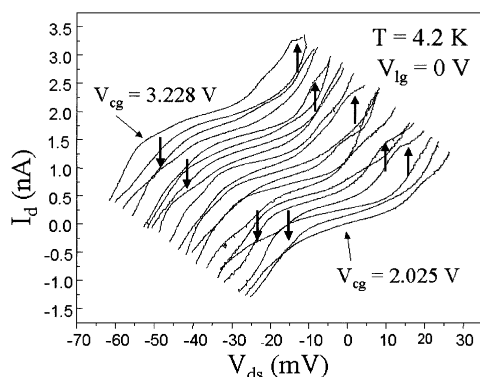

Fig. 6. Measurements of source–drain current at a low temperature $T = 4.2$ K. The control metal gate voltage varies from 2.025 V to 3.228 V in steps of 60 mV.

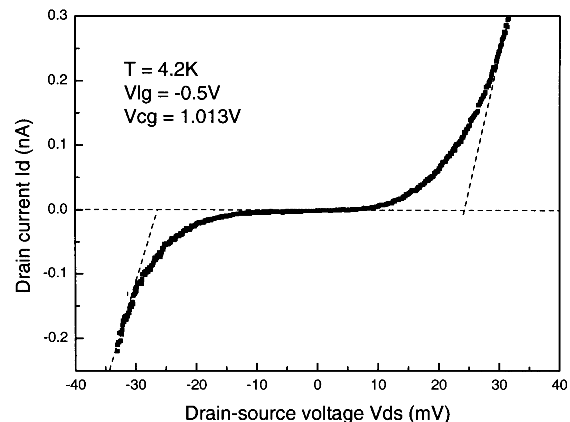

Fig. 7. Drain current voltage characteristics of the device with a fixed lower gate voltage $V_{lg} = -0.5\ V$ and control-gate voltage $V_{cg} = 2.341\ V$, measured at 4.2 K.

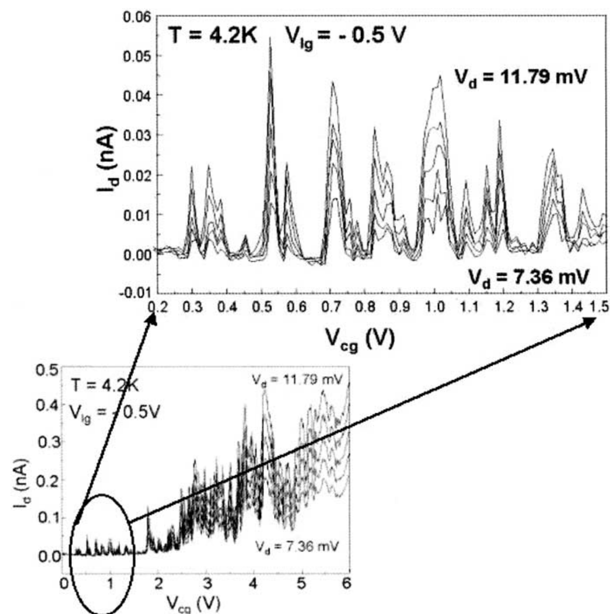

Fig. 8. Coulomb oscillations of the dual-capacitive coupled gate on the transport properties of nano tunneling channel at 4.2 K as a function of the top control gate voltage with resolved quantum levels for different V_d's. V_d varies from 7.36 mV (bottom) to 11.79 mV (top) in steps of 1.1 mV.

channel current decrease by the lower gate-induced electrostatic potential barriers, rather than some charged defect fluctuation, which is uncontrolled and possibly occurs at the Si-SiO_2 interface [17].

The drain-to-source current–voltage characteristics measured at a low temperature $T = 4.2$ K are plotted in Fig. 6 with the control-gate voltage from 2.025 to 3.228 V in steps of 60 mV. This is a clear indication of the Coulomb blockade effect. Moreover, some of the curves depict Coulomb staircase (as indicated by arrows in Fig. 6) at different applied voltages. The origin of the Coulomb blockade effects shown in Fig. 6 observed when only the upper control gate bias is applied may be due to the roughness of the SOI nano wire, or the impurities in distributed electron islands separated by tunneling barriers could be formed by dopant fluctuations within the nanostructure [18]. Furthermore, by applying negative voltage to the lower gates to induce depletion regions in the nano channel beneath the gate oxide, two electron-tunneling barriers are induced and a quantum dot is created between these two electrically induced barriers. In Fig. 7 we show the drain current–voltage characteristics of the device for a fixed lower gate voltage $V_{lg} = -0.5\ V$ and a controlled-gate voltage $V_{cg} = 2.341\ V$, measured at 4.2 K. The corresponding Coulomb gap is found to be 50 mV. Due to the limit of our measurement system, we can not support the data above 4.2 K.

The effects of the dual-capacitive coupled gate on the transport properties of the nano tunneling channel were also measured. In Fig. 8, $I_d - V_{cg}$ characteristics with respect to the control-gate are shown. The drain-to-source bias is varied between 7.36 to 11.79 mV in steps of 0.9 mV, while the lower gate voltage is fixed at -0.5 V. When the lower gate voltage is biased at around -0.5 V, which is negative enough to form two small energy barriers for the quantum dot in the source-to-drain tunneling channel. In Fig. 8, $I_d - V_{cg}$ characteristics show nonlinear $I_d - V_d$ ones even at the peak V_g. These results suggest that Coulomb diamond is not closed at peak position, which means that a multiple-island SET is formed [19], [20]. Electrons tunnel through the nano channel, and the quantized nature of the energy level inside the nano channel causes the observed

oscillation peaks. But it is thought that these barriers are formed mainly due to the lower gate-induced electrostatic potential. The complex periodic oscillation curve indicates the superposition of different modes. The current exhibits oscillations and the period $\Delta V_{\rm g}$ is around 50, 100, and 150 mV, respectively. If we assume the island has a spherical shape, the dot capacitance corresponds to the self-capacitance of a sphere with a diameter of 30 nm. This value is consistent with the device structure; in our device, the Coulomb island is determined by the thickness and width of the nanowire, the length is defined by the separation of the two spacer depletion gates which are formed by e-beam lithography combined with the spacer formation processes. The effective size of the Coulomb island should therefore be smaller than $40 \times 80 \times 60$ nm^3, due to further shrinkage by thermal oxidation process and the electrical field effect. Assuming a dominant charging dot, the control gate capacitance $(c_{\rm g} = e/\Delta V_{\rm g})$ is estimated to be $e/2\Delta V = 1.06 \sim 3.2$aF and the dot capacitance (C) is around 6.4 aF. From these measurements, we obtain typical energy scales of the charging energy (Ec) to be around 11.25 meV. However, the requirement for the charging energy is much larger than the thermal energy. According to the orthodox theory of single-electron tunneling, Coulomb oscillations and Coulomb blockade only matter, if the Coulomb energy is bigger than the thermal energy. Otherwise thermal fluctuations will disturb the motion of electrons and will wash out the quantization effects. The necessary condition is $Ec = e^2/2C > k_B\, T$, where k_B is Boltzmann's constant and T is the absolute temperature. This means that the capacitance C has to be smaller than 1.03 aF for charging effects to appear at room temperature. The patterned structure size can be estimated smaller than $20 \times 20 \times 30$ nm^3 for room temperature operation.

Park *et al.* [14] reported previously that they barely observed the Coulomb-blockade effect by enhancing the effect with increasing number of the coupled dots. In contrast, we have successfully demonstrated a SET with pronounced Coulomb-blockade effect by employing the dual-gate structure. This is probably due to the narrower width within and between the spacer depletion gates in our device, thus leading to two narrower barriers and the quantum dots, which are beneficial to the observation of the Coulomb-blockade effect.

IV. Conclusions

The electrically induced multiple quantum dots on a narrow silicon wire have been successfully demonstrated. The dual-gate-controlled device employs a narrow-channel (width <80 nm and thickness <60 nm) FET defined by e-beam lithography combined with self-aligned polysilicon sidewall spacers that serve as depletion gates. The *I–V* characteristics depict typical Coulomb gap characteristics of the single-electron charging effect. The Coulomb oscillations by single dot coupling were observed at low temperature. The effective size of the Coulomb island is consistent with the device structure of a sphere with a diameter of 30 nm by thermal oxidation process and the electric field effect. Further reduction of the quantum dot's size is promising with the proposed method that could lead to possible room temperature operation in the near future.

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Shu-Fen Hu was born in Tainan, Taiwan, R.O.C. She received the Bachelor degree in physics from Shoochow University, Taipei, Taiwan, in 1981, and the M.Phil. and Ph.D. degrees in physical chemistry from the University of Cambridge, Cambridge, U.K., in 1992 and 1995, respectively.

For eight years, she worked as a Process Engineer at semiconductor factories. From 1995 to 1997, she was with the National Tsing Hua University, Hsinchu, Taiwan, as a Postdoctorate. In 1997, she joined the National Nano Device Laboratories, Hsinchu, Taiwan, as an Associate Researcher. Her scientific research interests include nano structures and nanoelectronics. She is the author or coauthor of more than 30 publications in international journals.

Yung-Chun Wu received the B.S degree in physics from the National Central University, Taoyuan, Taiwan, R.O.C., and the M.S. degree, also in physics, from the National Taiwan University, Taipei, Taiwan, in 1996 and 1998, respectively. He is currently pursuing the Ph.D. degree at the National Chiao-Tung University, Hsinchu, Taiwan.

From 1998 to 2002, he was an Assistant Researcher at the National Nano Device Laboratory, Hsinchu, Taiwan, engaged in research on single-electron transistors and electron-beam lithography technology. His Ph.D. research includes fabrication, simulation, and characterization of submicron LTPS TFT and novel nano-scale devices.

Chin-Lung Sung received the B.S. degree in materials science from National Tsing-Hua University, Hsinchu, Taiwan, R.O.C., in 1982. He is currently pursuing the Master degree at the National Chiao-Tung University, Hsinchu.

After his military service, he became a Semiconductor Process Engineer working in semiconductor factories from 1984 to 1993. In 1993, he joined the National Nano Device Laboratories, Hsinchu, as a Senior Technical Research Staff Member. He is coauthor of more than 15 publications in international journals.

Chun-Yen Chang (M’88) was born in Feng-Shan, Taiwan, R.O.C. He received the B.S. degree in electrical engineering from National Cheng Kung University (NCKU), Taiwan, in 1960, the M.S. degree in tunneling in semiconductor-superconductor junctions and the Ph.D. degree in carrier transport across metal–semiconductor barrier, both from National Chiao-Tung University (NCTU) Hsinchu, Taiwan, in 1969.

In 1969, he became a Full Professor at NCKU. From 1977 to 1987, he established a strong electrical engineering and computer science program at NCKU where GaAs, Si, and poly-Si researches were established in Taiwan for the first time. Since 1987, he served consecutively as Dean of Research (1987–1990), Dean of Engineering (1990–1994), and Dean of Electrical Engineering and Computer Science (1994–1995) at NCKU. Simultaneously, he was serving as the Founding President of National Nano Device Laboratories (NDL), Hsinchu, from 1990 to 1997. From 1997 to 1998, he served as Director of the Microelectronics and Information System Research Center (MIRC), NCTU. In August 1998, he was appointed as the President of NCTU. As the National Chair Professor and President of NCTU, his vision is to lead the university for excellence in engineering, humanity, art, science, management and bio-technology.

Dr. Chang received the IEEE Third Millennium Medal in 2000. He is a Member of Academia Sinica and a Foreign Associate of the National Academy of Engineering.

Tiao-Yuan Huang (S’78–SM’87–F’95) was born in Kaohsiung, Taiwan, R.O.C., on May 5, 1949. He received the B.S.E.E. and M.S.E.E. degrees from National Cheng Kung University, Tainan, Taiwan, in 1971 and 1973, respectively, and the Ph.D. degree in electrical engineering from the University of New Mexico, Albuquerque, in 1981.

He served two years in the Taiwan Navy and was with the Chung Shan Institute of Science and Technology, Taoyuan, Taiwan, for another two years. He spent 14 years working in U.S. semiconductor industries, where he held various technical and managerial positions. In 1995, he returned to Taiwan to become a Chair Professor with the National Chiao Tung University, Hsinchu, and Deputy Director in charge of Research and Development of the National Nano Device Laboratories, Hsinchu, Taiwan, in 1995.

Dr. Huang is currently on the program committee of the International Conference on Solid-State Devices and Materials (SSDM). He served on the Technical Committee of the IEEE International Electron Devices Meeting (IEDM) in 1990 and 1991, respectively.