A 11-mW Quadrature Frequency Tripler with Fundamental Cancellation

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***Abstract*— A low-power quadrature frequency tripler is designed by using the sub-harmonic mixer configuration. The circuit is implemented in CMOS 0.180um technology. The frequency tripler consumes 11.5mW, while the output buffers consumes 43.1mW, all with supply voltage of 1.8V. The fundamental Harmonic Rejection Ratio (HRR_1) achieves more than 35dB, and the conversion gain achieves -4.2dB at output frequency of 4.5GHz. The entire chip area occupied 1.4x1.1 mm^2.**

***Index Terms*— frequency tripler, doubler, harmonic rejection ratio, sub-harmonic mixer.**

I. Introduction

Signal generation is critical in many wireless systems in order to provide an LO signal for frequency conversion. Frequency multiplication is popularly accepted to produce very high-frequency signals using low-frequency inputs. Typically the method relies on strong input signals that drive a device into the strongly nonlinear region to obtain the high-order frequency harmonics, of which the desired output signal is selected by filtering.

A frequency tripler utilizes the third-order nonlinearity. The device is biased to maximize the third-order harmonic output [1, 2]. The circuit usually results in large power consumption and low frequency conversion efficiency. Alternative approaches include the waveform shaping method [3], and the injection-locking method [4]. A frequency tripler using sub-harmonic mixers was proposed in [5]. It generates the third-order harmonic current efficiently. Similar approach is also found in [6].

In practice, frequency multiplication comes with harmonic spurs, undesired for LO applications. The fundamental spur is usually the largest spur. Those spurs might introduce undesired frequency conversion and degrade system performance. Most triplers therefore require filters to reduce the spurious noise level. An effective method is cancellation by active circuitry. With appropriate phase and magnitude tuning, the fundamental spur is greatly suppressed [6]. Nevertheless the entire circuit consumes large power as it requires several stages for signal processing.

In this work, a low-power cancellation circuitry is proposed and verified in a CMOS frequency tripler. This is an extension of the tripler circuit in [5] to carry out cancellation without filtering. The low power cancellation circuit generates the required signal in 180 degrees out of phase to the input fundamental, which is therefore cancelled at the output to obtain a high harmonic rejection ratio. The output loading effect due to the cancellation circuitry is minimal. Moderate conversion gain under low power consumption is obtained. The entire circuit features quadrature signals at the input and output, applicable to RF transceivers associated with quadrature modulation. This approach is verified by an S-band generator in 0.18um CMOS technology. It can be further extended to a higher frequency range.

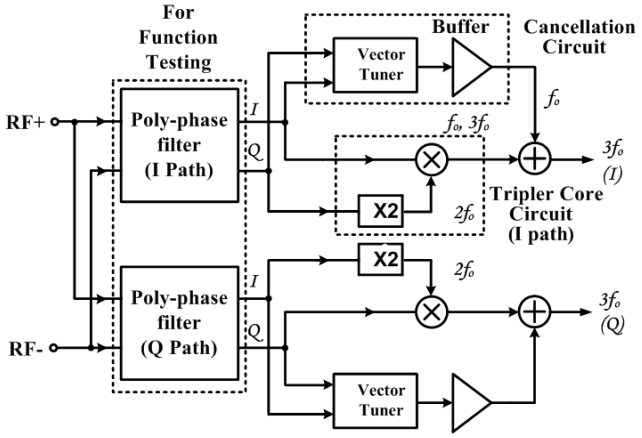

Fig. 1. The block diagram of the proposed frequency tripler with fundamental cancellation.

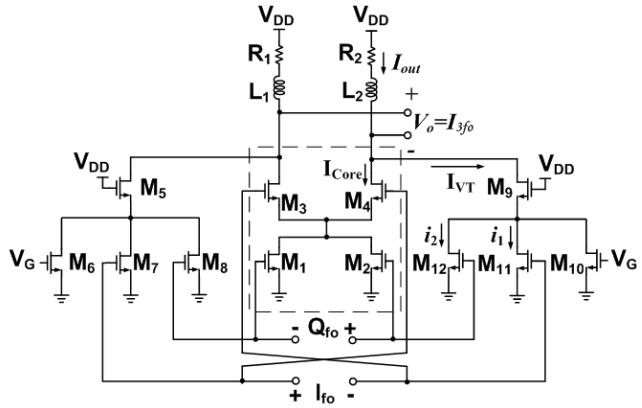

Fig. 2. The schematic of the tripler core with cancellation circuit (I Path).

II. CIRCUIT DESIGN

Fig.1 shows the block diagram of the proposed quadrature frequency tripler with fundamental cancellation. It consists of an I/Q-pair of triplers and cancellation circuits. The low-power tripler core circuit follows the single-balanced subharmonic mixer design in [5]. A transistor pair connected in parallel forms a frequency doubler. It takes the fundamental frequency at f_o to generate the second-order harmonic at $2f_o$, which is then mixed with the fundamental to produce the third-order harmonic output at $3f_o$. To maximize the conversion gain, quadrature input signals are required. By doing so, a pair of the core circuits completes a quadrature tripler. In the front of the circuit, two poly-phase filters of three stages are applied to generate the required quadrature input signals for measurement purpose.

It is assumed that all even-order spurs can be significantly suppressed in a double-balanced mixer design. The only notable one is the fundamental, which is therefore the design goal for the cancellation circuit to deal with in this work. Cancellation occurs by producing out-of-phase fundamental signals with respect to the tripler fundamental outputs. This approach works for a good portion of frequency bandwidth. Without loss of generality, the operation frequency is chosen in the range of few GHz frequencies to verify the low-power scheme.

A. Tripler Core Circuit

Circuit implementation is shown in the dashed box of Fig. 2. The tripler consists of transistors $M_{1\text{-}4}$ as a single-balanced subharmonic mixer. This current re-use topology is advantageous in low power consumption. The bottom transistor pair (M_1, M_2) forms a frequency doubler that generates the output current at $2f_o$, which in turn drives the source couple differential pair (M_3, M_4), which works as the switching stage of the mixer. This mixer produces outputs of the frequency f_o and $3f_o$ ($2f_o \pm f_o$). To maximize the output current at $3f_o$, each transistor is biased at the condition to achieve a high value of the first derivative of the transconductance (gm'). The efficiency of frequency conversion also relies on the phase relationship of the two input signals to the upper and lower differential pairs. It is found the phase difference needs to be ±90 degrees out of phase, or a quadrature pair.

The tripler output current, i_{core}, carries many undesired harmonics, expressed as

$$i_{Core} = \sum_n A_n \cos(n\omega t + \psi_n) \qquad (1)$$

where those terms of n=1 and n=2 correspond to the fundamental and the second-order harmonics respectively. Only the third-order harmonic of n=3 is the required output. Spurious noise can be characterized by the harmonic rejection ratio (*HRR*) defined as

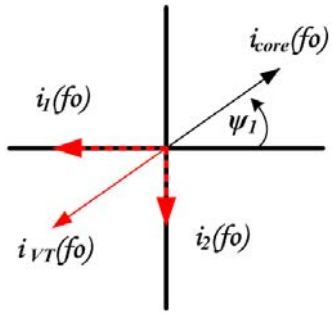

Fig. 3. The concept of the fundamental frequency cancellation.

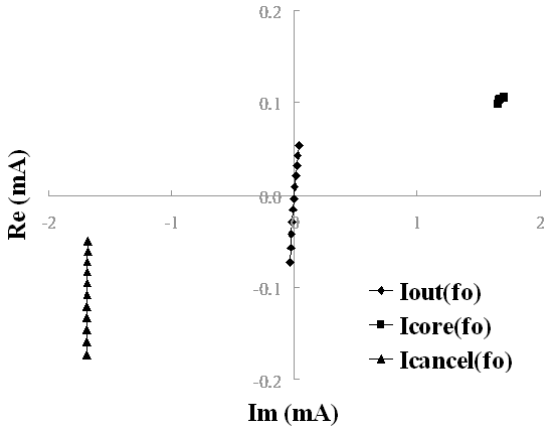

Fig. 4. Simulation result of the current at input frequency from 1GHz to 2GHz.

$$HRR_n = 20\log\left(\left|\frac{\text{3rd - order harmonic output}}{\text{n}^{\text{th}}\text{ - order harmonic output}}\right|\right). \qquad (2)$$

where n refers to the n-th order harmonic. A high *HRR* value is preferred. Traditionally, filters are used to eliminate undesired spurs to enhance circuit performance.

B. Fundamental Cancellation Circuit

As aforementioned, the fundamental cancellation circuit is introduced to suppress the spur at the fundamental frequency to obtain a high HRR_1 value. As shown in Fig. 2, the cancellation circuit is implemented in the differential form. It consists of a unit current gain buffer (M_5 and M_9) and a vector tuner ($M_{7,\ 8}$ and $M_{11,\ 12}$). Transistors (M_6 and M_{10}) work as current sources to provide appropriate biasing current to the gain buffer. The gain buffer isolates the tripler and vector tuner to reduce the loading effect on the tripler core due to the parasitic capacitance from the vector tuners.

The fundamental component of i_{core} is due to the direct feed-through of the input signal at the gate port of M_4. The cancellation circuit generates cancellation current I_{vt}

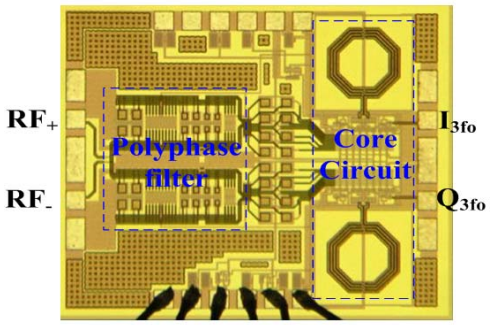

Fig. 5. Microphotograph of the entire quadrature tripler.

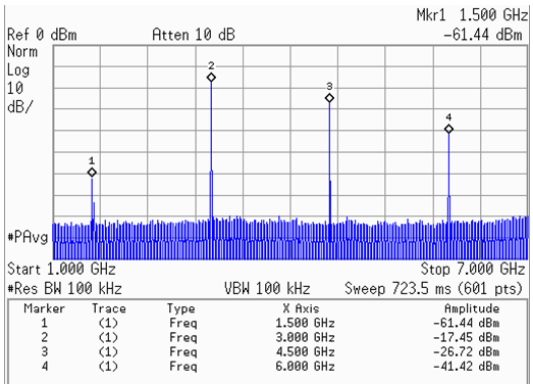

Fig. 6. Output spectra with 19 dBm input signal at1.5GHz.

of 180-degree out of phase to null out that component. I_{vt} comes from the vector combination of the input I and Q signals, which magnitudes are adjusted by M_{11} and M_{12}, respectively, to produce the required phase and magnitude. Fig. 3 demonstrates the concept of the fundamental frequency cancellation. The current i_1 and i_2 are associated with the drain current of transistor M_{11} and M_{12}, respectively. Since direct feedthrough gives transfer gain less than one, transistors M_{11} and M_{12} do not need to provide large gain. As such, both transistors could biased at the low-power subthreshold condition.

Ideal fundamental cancellation occurs only at single frequency point. For bandwidth concern, the bias condition is somewhat adjusted to extend the operation bandwidth. Fig. 4 shows the simulation results of fundamental cancellation over the input frequency from 1 GHz to 2 GHz. It appears i_{core} is quite frequency-independent, but I_{vt} moves along with the input frequency. Nevertheless, the cancellation circuit greatly reduces the fundamental to be no more than 5%.

III. Measurement Results

The tripler circuit with fundamental frequency cancellation is fabricated in 0.18 um CMOS technology.

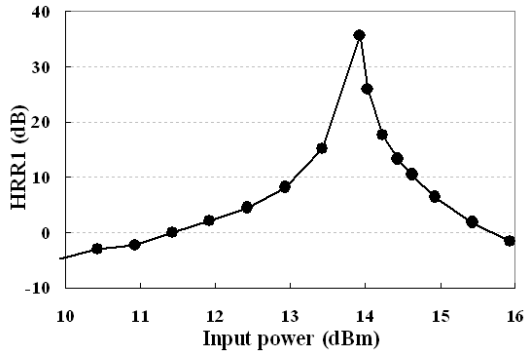

Fig. 7. Harmonic rejection of the fundamental at 1.5 GHz.

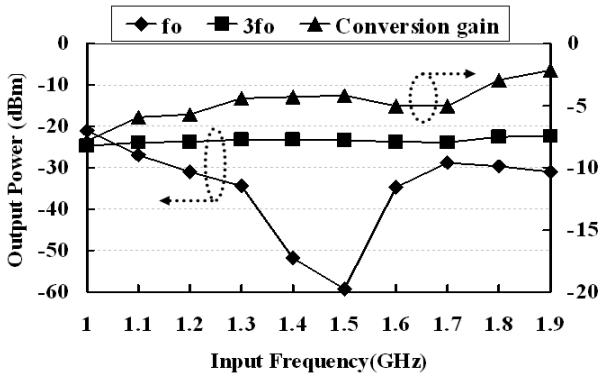

Fig. 8. The output power and conversion gain.

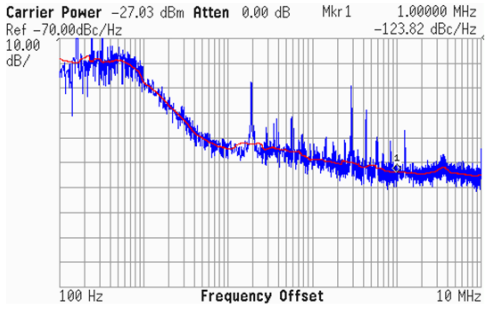

Fig.9.The phase noise of the output at *3fo* (*fo* =1,5GHz).

The microphotograph is shown in Fig. 5. The entire die area is 1.4×1.1 mm^2 including pads, but the circuit only occupies 0.35×1.1 mm^2 without the poly-phase filters. An off-chip 180^o hybrid coupler provides a differential signal to the pair of three-stage poly-phase filters, which produces quadrature I/Q signals to drive the core circuit. The cascaded three stages result in very large signal loss but wide bandwidth. There is no need of the quadrature phase generator in integrated environment. Open-drain buffers are used at the output for measurement purpose.

The output signal is probed at one side of the differential output with the other side terminated. Fig. 6 shows an output spectrum snapshot with the input signal

(P_{in}) of 19dBm at 1.5GHz. In this single-balanced implementation the second-order harmonic appears to be very large, but it is not concerned in double-balanced circuit applications. Transistor bias is directly controlled by the gate voltage in this simple test circuit. It is sensitive to process variation regarding to the fundamental cancellation. During measurements, the gate voltages are re-adjusted for the optimal performance. This can be improved with better biasing circuitry. After calibration of cable loss, the output fundamental level of f_o is -59.3 dBm. The conversion voltage gain is -4.2 dB, excluding the loss due to the poly-phase filters and output buffers using simulated values.

Fig. 7 demonstrates the HRR_1 versus P_{in} with the input frequency at 1.5 GHz. The optimal P_{in} is 14 dBm, yielding to an HRR_1 more than 35 dB. Fig. 8 shows the power levels of the f_o and $3f_o$ outputs and the conversion voltage gain. The conversion gain is about -5 dB over the frequency range of interest. Measured at the input frequency of 1.5 GHz, the output phase noise at $3f_o$ is -123.8 dBc/Hz at 1MHz offset as shown in Fig. 9. The phase noise of the input signal is -142.3 dBc/Hz, yielding to discrepancy of 8.9dB relative to the ideal multiplication.

The total power consumption in operation is 11.5mW (Pin=14dBm), while the output buffer consumes 43.1 mW, all with V_{DD} supply voltage of 1.8 V. The circuit performance is summarized in Table I. Table II gives comparison with other work. This design gives very low power consumption, while HRR_1 achieves a great level.

TABLE I.
Measured tripler performance summary.

Technology	CMOS 0.18um
Supply Voltage	1.8 V
DC Power (With Buffer)	11.5 mW (43.1mW)
Fundamental Rejection Ratio	35 dB
Conversion Gain	-4.2dB
Chip Area (Core circuit)	1400x1100 um^2 (350x1100 um^2)

IV. Conclusion

A novel technology of tripler with fundamental frequency cancellation circuit is realized using TSMC 0.18 um CMOS technology. The fundamental frequency is one of the most significant in multiplier circuit design. In this circuit, the harmonic rejection ratio HRR_1 achieves more than 35dB and provides conversion gain of -4.2 dB. The proposed tripler produces output signals in quadrature phases. It can be applied to signal generation in the millimeter-wave applications.

Acknowledgment

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TABLE II.
Performance comparison with other works.

	[2]	[5]	[6]	This work
Technology	SiGe HBT	CMOS 180 nm	CMOS 180 nm	CMOS 180 nm
Frequency (GHz)	8	7	1	1.5
HRR1 (dBc)	7	22.4	30	35
Conversion Gain (dB)	-8	-5.6	3	-4.2
DC Power (mW)	92.4	7.5	68	11.5 w/o buffer

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