

# Al<sub>2</sub>O<sub>3</sub>-Ge-On-Insulator n- and p-MOSFETs With Fully NiSi and NiGe Dual Gates

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**Abstract**—High- $\kappa$  Al<sub>2</sub>O<sub>3</sub>/Ge-on-insulator (GOI) n- and p-MOSFETs with fully silicided NiSi and germanided NiGe dual gates were fabricated. At 1.7-nm equivalent-oxide-thickness (EOT), the Al<sub>2</sub>O<sub>3</sub>-GOI with metal-like NiSi and NiGe gates has comparable gate leakage current with Al<sub>2</sub>O<sub>3</sub>-Si MOSFETs. Additionally, Al<sub>2</sub>O<sub>3</sub>-GOI C-MOSFETs with fully NiSi and NiGe gates show 1.94 and 1.98 times higher electron and hole mobility, respectively, than Al<sub>2</sub>O<sub>3</sub>-Si devices, because the electron and hole effective masses of Ge are lower than those of Si. The process with maximum 500 °C rapid thermal annealing (RTA) is ideal for integrating metallic gates with high- $\kappa$  to minimize interfacial reactions and crystallization of the high- $\kappa$  material, and oxygen penetration in high- $\kappa$  MOSFETs.

**Index Terms**—Ge, Ge-on-insulator (GOI), MOSFET, NiGe, NiSi.

## I. INTRODUCTION

**M**ETAL GATES on high- $\kappa$  gate-dielectrics [1]–[4] and on strained-Si [5] or on Ge-on-insulator (GOI) [6] are required to optimize the performance of transistors in advanced C-MOSFETs. The high- $\kappa$  gate-dielectric is required to reduce the gate leakage current at a small equivalent-oxide-thickness (EOT); the metal gate electrode [5], [7]–[12] can eliminate the gate depletion effect and increase the transistor drive current; strained-Si or GOI can improve carrier mobility and thus increase the drive current. In this letter, high- $\kappa$  Al<sub>2</sub>O<sub>3</sub> gate dielectrics on GOI C-MOSFETs [6] were integrated with metal-like fully silicided NiSi [5], [10]–[12] and germanided NiGe dual gates. The advantages of GOI are that Ge has both a lower hole and electron effective mass than Si, and GOI is free of defects [6], meeting the very large scale integration (VLSI) manufacturing requirement ( $< 1 \text{ cm}^{-2}$ ) with much lower value than the  $\sim 10^4 - 10^6 \text{ cm}^{-2}$  density in globally strained-Si on SiGe. Fully NiSi and NiGe gates are formed at the same low temperature of 400°C by RTA, which is required to reduce the diffusion of metal into the gate dielectric [12], [13]. Besides, the fully NiSi and NiGe gates have the advantages of being

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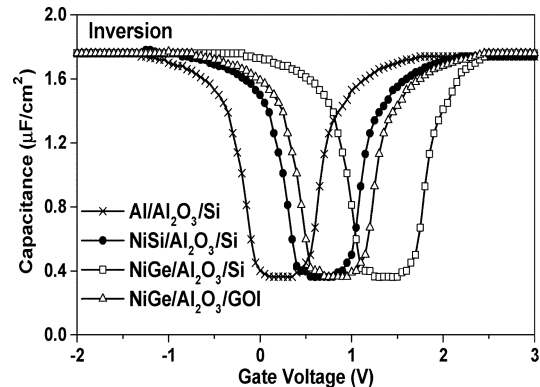


Fig. 1.  $C$ - $V$  characteristics of Al<sub>2</sub>O<sub>3</sub>-Si and Al<sub>2</sub>O<sub>3</sub>-GOI p-MOSFETs with fully silicided NiSi, fully germanided NiGe, and control Al gates. The same value of accumulation and inversion capacitance is due to the metal-like fully NiSi or NiGe gate electrode.

compatible with current VLSI processes, while providing a large work function difference [14]. At 1.7 nm EOT, the Al<sub>2</sub>O<sub>3</sub>-GOI C-MOSFETs with fully NiSi and NiGe gates have comparable gate leakage currents but 1.94 and 1.98 times higher electron and hole mobilities, respectively, than those of Al<sub>2</sub>O<sub>3</sub>-Si control devices.

## II. EXPERIMENTAL

GOI wafers were formed by depositing 75 nm SiO<sub>2</sub> on both Ge and Si wafers, followed by bonding SiO<sub>2</sub>-Ge and SiO<sub>2</sub>-Si at 500 °C for 10 h. An O<sub>2</sub> plasma was used to activate the SiO<sub>2</sub> surface before bonding and a constant pressure was applied during bonding. After the GOI wafers were thinned down, a 400 nm isolating layer of SiO<sub>2</sub> was deposited on the GOI. The source and drain regions were implanted with 35-keV phosphorus or 25 keV boron to form n- and p-MOSFETs, respectively. The RTA activation was performed at 500 °C or 950 °C for GOI or Si, respectively. Then, the Al<sub>2</sub>O<sub>3</sub> gate dielectric was grown on the GOI [6]. The dual fully silicided NiSi and germanided NiGe were formed on both the Al<sub>2</sub>O<sub>3</sub> gate dielectric and opened contact regions of the source-drain. The NiSi or NiGe is formed by depositing 15-nm amorphous Si or Ge on Al<sub>2</sub>O<sub>3</sub>-GOI; depositing 15-nm Ni on the SiAl<sub>2</sub>O<sub>3</sub>-GOI or Ge-Al<sub>2</sub>O<sub>3</sub>-GOI, and then annealing at 400 °C for 30 s for silicidation [12] or germanidation, respectively. For comparison, control Al<sub>2</sub>O<sub>3</sub>-Si MOSFETs with Al metal gates were fabricated.

## III. RESULTS AND DISCUSSION

Fig. 1 plots the capacitance-voltage ( $C$ - $V$ ) characteristics of Al<sub>2</sub>O<sub>3</sub>-Si and Al<sub>2</sub>O<sub>3</sub>-GOI p-MOSFETs with fully silicided

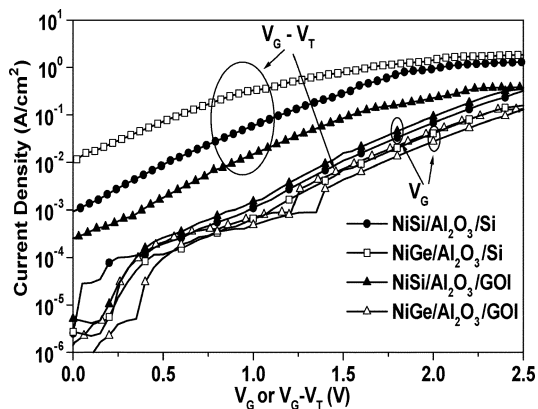


Fig. 2.  $J_G-V_G$  and  $J_G-(V_G-V_T)$  characteristics of Al<sub>2</sub>O<sub>3</sub>-Si and Al<sub>2</sub>O<sub>3</sub>-GOI capacitors with fully silicided NiSi and fully germanided NiGe gates.

NiSi, fully germanided NiGe, and control Al gates. That the capacitances measured under inversion and accumulation are the same suggests that the NiSi and NiGe gates are fully silicided or germanided, free from poly gate depletion. A  $\kappa$  value of 9 and an EOT of 1.7 nm are obtained from the  $C-V$  characteristics, and the large shifts in the  $C-V$  curves are due to the different flat band voltages ( $V_{fb}$ ).

Fig. 2 shows the gate dielectric leakage currents of Al<sub>2</sub>O<sub>3</sub>-Si and Al<sub>2</sub>O<sub>3</sub>-GOI nMOS capacitors with fully NiSi and NiGe gates. The higher leakage current than expected from the  $J_G$  versus  $V_G-V_T$  plot may be related to slight Ni diffusion [13], [15] into the 1.7-nm EOT Al<sub>2</sub>O<sub>3</sub> gate oxide. Similar findings are also observed for fully NiSi and NiGe gates on 1.9-nm-SiO<sub>2</sub>-Si MOSFETs, although these leakage currents are lower than those of the Al control devices obtained from the  $J_G$  versus  $V_G$  plot [15]. Further improvement may be obtained by adding N into the gate dielectric to form an oxynitride. For the same EOT of 1.7 nm, the leakage current at  $V_G = 1$  V is three to four orders of magnitude lower than that of SiO<sub>2</sub>, because of the thicker high- $\kappa$  material. A high-quality Al<sub>2</sub>O<sub>3</sub> gate dielectric can also be formed on GOI at 1.7 nm EOT, based on the measured comparable leakage current. Additionally, GOI is ideal for high- $\kappa$  MOSFETs since the highest thermal budget for device fabrication is only 500 °C RTA for implant annealing. At such a low temperature, the problems of interface reaction, high- $\kappa$  crystallization, and penetration of oxygen, often found in high- $\kappa$ /Si MOSFETs, are all suppressed.

Fig. 3 compares the  $I_D-V_D$  characteristics for Al<sub>2</sub>O<sub>3</sub>-Si and Al<sub>2</sub>O<sub>3</sub>-GOI C-MOSFETs with fully NiSi, NiGe and control Al gates. GOI has significantly higher  $I_D$  than Si devices, because Ge has smaller electron and hole effective masses than Si. The  $I_D-V_D$  curves of Al<sub>2</sub>O<sub>3</sub>-Si MOSFETs are almost the same as those of the control Al gate, implying that the device performance is negligibly degraded when using fully NiSi and NiGe gates. This is because the low silicide/germanide formation temperature, 400 °C, prevents the diffusion of excess Ni into Al<sub>2</sub>O<sub>3</sub>-Si and Al<sub>2</sub>O<sub>3</sub>-GOI [12], [13]; such excess Ni must be used to ensure the complete reaction of Si or Ge on the gate dielectric to avoid gate depletion.

Fig. 4(a) and 4(b) presents the electron and hole mobilities obtained from the measured  $I_D-V_G$  curves of n- and p-MOS-

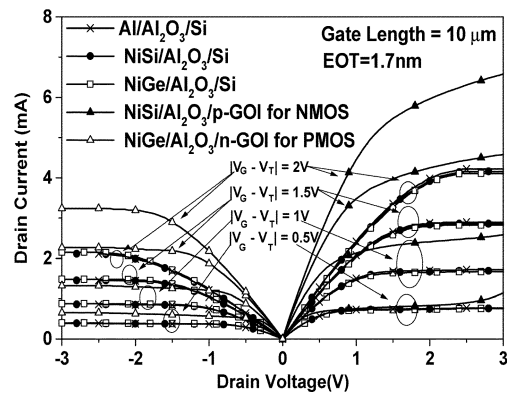


Fig. 3.  $I_D-V_D$  characteristics of Al<sub>2</sub>O<sub>3</sub>-Si and Al<sub>2</sub>O<sub>3</sub>-GOI n- and p-MOSFETs with fully silicided NiSi, fully germanided NiGe, and control Al gates. The fully NiSi is used for nMOSFET due to the lower workfunction and NiGe is used for p-MOSFETs due to higher workfunction. The gate length is 10  $\mu$ m and width is 100  $\mu$ m.

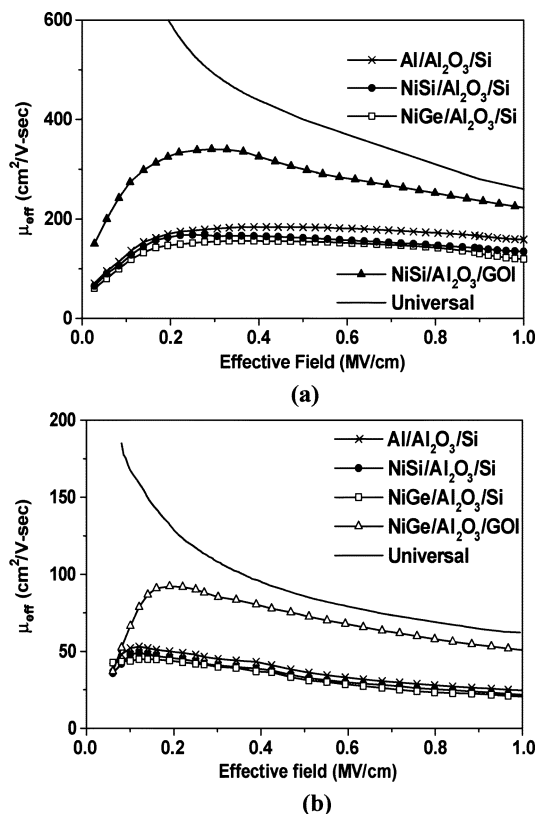


Fig. 4. (a) Electron and (b) hole mobilities from  $I_D-V_G$  characteristics of Al<sub>2</sub>O<sub>3</sub>-Si and Al<sub>2</sub>O<sub>3</sub>-GOI n- and p-MOSFETs with fully silicided NiSi, fully germanided NiGe, and control Al gates.

FETs, respectively. A mobility lower than the universal mobility is typical for high- $\kappa$  Al<sub>2</sub>O<sub>3</sub>-Si MOSFETs. Further improvement, using novel high- $\kappa$  with lower interface and bulk dielectric charges, is currently under development. The peak electron and hole mobilities for Al<sub>2</sub>O<sub>3</sub>-GOI with fully NiSi and NiGe gates are increased by factors of 1.94 and 1.98 to 350 and 100 cm<sup>2</sup>-V-s, respectively. The slightly lower hole mobility than obtained in our previously developed Al/Al<sub>2</sub>O<sub>3</sub>-GOI MOSFET [6] may be associated with the nonoptimized source-drain NiSi or NiGe contact formed at the same time as the gate.

#### IV. CONCLUSION

High- $k$   $\text{Al}_2\text{O}_3$ -GOI C-MOSFETs were integrated with fully silicided NiSi and germanided NiGe dual gates. The capacitances and leakage currents obtained using fully NiSi and NiGe gates were similar to those obtained using Al metal gates on 1.7-nm EOT  $\text{Al}_2\text{O}_3$  gate dielectric. These devices have approximately twice the electron and hole mobilities as  $\text{Al}_2\text{O}_3$ -Si devices, and a process which can be compatible with current VLSI technologies.

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