Positive Oxide Charge-Enhanced Read Disturb in a Localized Trapping Storage Flash Memory Cell

Wen-Jer Tsai, Chih-Chieh Yeh, Nian-Kai Zous, Chen-Chin Liu, Shih-Keng Cho, Tahui Wang, *Senior Member, IEEE*, Samuel C. Pan, *Member, IEEE*, and Chih-Yuan Lu, *Fellow, IEEE*

***Abstract*—Read disturb-induced erase-state threshold voltage instability in a localized trapping storage Flash memory cell with a poly-silicon–oxide–nitride–oxide–silicon (SONOS) structure is investigated and reported. Our results show that positive trapped charge in bottom oxide generated during program/erase (P/E) cycles play a major role. Both gate voltage and drain voltage will accelerate the threshold voltage (V_t) drift. Hot-carrier caused disturb effect is more severe in a shorter gate length device at low temperature. A model of positive charge-assisted electron tunneling into a trapping nitride is proposed. Influence of channel doping on the V_t drift is studied. As the cell is in an "unbiased" storage mode, tunnel detrapping of positive oxide charges is responsible for the threshold voltage shift, which is insensitive to temperature.**

***Index Terms*—Cycling-induced oxide charges, Flash EEPROM, hot-carrier effect, MXVAND, NROM, PHINES, positive charge-assisted electron tunneling, read disturb, poly-silicon–oxide–nitride–oxide–silicon (SONOS), tunnel detrapping, threshold voltage (V_t) instability.**

I. Introduction

RECENTLY, localized charge-trapping storage, two-bits-per-cell Flash memory technology with a poly-silicon–oxide–nitride–oxide–silicon (SONOS) structure has attracted much attention [1]–[6]. In addition to its simpler fabrication process, the smaller cell size and higher packing density, the absence of drain turn-on and overerase are considered to be the advantages over current floating-gate Flash memory technologies [7]. Fig. 1 shows a typical SONOS memory cell, which is an nMOSFET with an oxide–nitride–oxide (ONO) stack as the gate dielectric. Based on this device structure, various methods of operation have been proposed. For example, NROM [2], multiplex virtual-grained AND (MXVAND) [3] (hot-electron programming and hot-hole erasing) and programming by hot hole injection nitride electron storage (PHINES) [5] [hot-hole programming and Fowler–Nordheim (FN) tunnel erasing] have been demonstrated to be promising candidates for Flash EEPROM technology. Charge loss characteristics of these cells have been discussed, and corresponding models have been proposed [3], [8]–[11]. Various ONO processing technologies [12] and alternative trapping layer materials [13] have been investigated to further improve their charge retention.

Manuscript received June 26, 2003; revised September 25, 2000. The review of this paper was arranged by Editor S. Kimura.

W.-J. Tsai, C.-C. Yeh, and T. Wang and are with the Macronix International Company, Ltd., Hsinchu, Taiwan, R.O.C., and also with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C. (e-mail: vincenttsai@mxic.com.tw).

N.-K. Zous, C.-C. Liu, S.-K. Cho, S. C. Pan, and C.-Y. Lu are with the Macronix International Company, Ltd., Hsinchu, Taiwan, R.O.C.

Digital Object Identifier 10.1109/TED.2003.822869

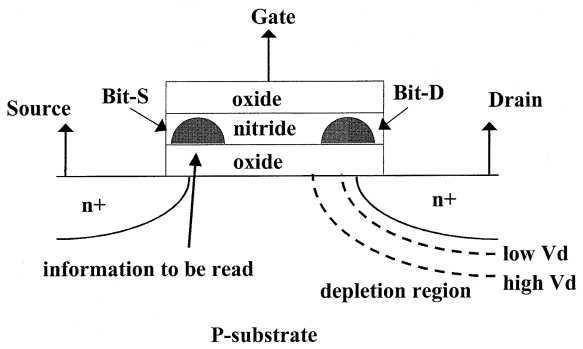


Fig. 1. Schematic representation of the cell structure and localized charge storage. Concept of reverse read is depicted by the depletion region in which the effect of injected charges is screened out.

The unique feature of two-bits-per-cell storage is due to the localized charge injection, nonconducting property of charge storage material, and a reverse read scheme [2]. As depicted in Fig. 1, a drain bias (V_d) is necessary to read out the information stored in bit-S. The appliedV_d must be large enough to "screen" out the injected charges at the drain bit (*Bit-D*). The read current (or threshold voltage) is then controlled by the charge state near the source (*Bit-S*), almost regardless of the charges at Bit-D. Typically, the applied bit-line voltage at read is around 1.6 V, which is higher than the read voltage in a floating-gate Flash memory cell (typically around 1 V). Fig. 2 shows the threshold voltage (V_t) shift of a 10-K program/erase (P/E) cycled cell during read operation, whereas the V_t drift is not observed in a noncycled cell. In the figure, the applied gate bias (V_g) is 2.5 V, and the drain bias is 1.6 V. This V_t shift, which will degrade the memory window and result in failure of cell operation, however, is rarely explored [14]. The purpose of this work is to find the dominant mechanisms that cause such erase-state V_t instability.

II. Experimental

The samples used in this paper are made of an nMOSFET-like device, with an ONO gate dielectric structure, in a virtual ground array. The source and drain are formed by buried-diffusion bit-lines [2]. The thickness of each ONO layer is 9 (top oxide), 6, and 7 nm. Devices with gate length from 0.5– 0.3μm and initial threshold voltage ($V_{\rm ti}$) from 1.2–3 V are characterized. The gate width is around 0.35 μm. Temperature effect from -20 °C to 85 °C is studied. Channel hot-electron injection and band-to-band tunneling-induced hot-hole injection are utilized for programming and erasing, respectively. Read operation is

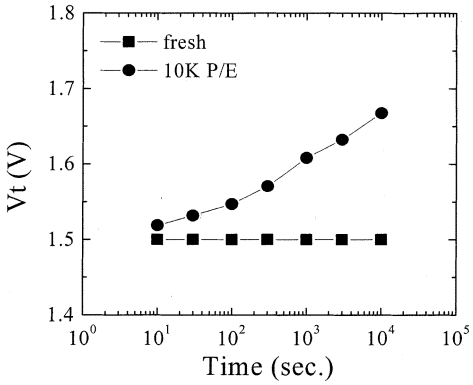


Fig. 2. Read-disturb characteristics of a fresh cell and a 10-K P/E cycled cell. $L_g = 0.5$ μm and $V_g/V_d/V_s = 2.5$V, /1.6V, /0 V.

TABLE I
OPERATION PRINCIPLES AND BIAS CONDITIONS UTILIZED DURING CELL OPERATIONS

	Bit-D			Bit-S		
	Vg	Vd	Vs	Vg	Vd	Vs
Program (CHE)	11V	5V	0V	11V	0V	5V
Erase (BTBT HH)	-3V	8V	0V	-3V	0V	8V
Read (Reverse)	2.5V	0V	1.5V	2.5V	1.5V	0V

achieved with a reverse read scheme. The bias conditions are summarized in Table I. Program time is around 5 μs, and erase time is about 5 ms. With such conditions, 2-V difference between program-state and erase-state V_t can be obtained. Three disturb modes are investigated for P/E cycled cells in erase state. In the first one, gate and drain biases are applied and the source is grounded. It is the conventional read disturb (RD) mode. The second one has an applied gate bias, and the source and drain are grounded. It is referred to as gate disturb (GD) mode, which is to emulate the gate bias effect on cells sharing the same word-line with the cell to be read. Finally, the room temperature drift (RT) mode, in which the V_t drift is insensitive to temperature [10], is the special case in which the cell is in "unbiased" storage (without any applied bias).

III. MODELING OF POSITIVE OXIDE CHARGE EFFECT ON READ DISTURB

Fig. 3 shows the V_t shift of a 10-K P/E cycled cell in a two-phase measurement, e.g., RT and RD are measured in sequence or vice versa. It is found that after RT (or RD), the following RD (or RT) is reduced. This gives us a hint that RT and RD may have the same cause, since they influence each other. It also means that V_t shift due to RD is dependent on the sampled time. Since positive oxide charge detrapping (with the coexistence of residual negative charges in nitride) has been clarified to be the major cause of RT [3], [10], these positive oxide charges created during P/E cycling are considered to affect RD also. It also explains the cycling effect on the observed erased-state V_t instability [3]. Table II shows the V_t drift models at various bias conditions and the corresponding time evolutions. In each case, the cycling-induced positive oxide charge plays a major role.

As the cell is stored without applied andV_d (RT mode), tunnel detrapping of the cycling-generated positive oxide charges (J_h in Table II) is the dominant mechanism. According to the tunnel front model [15], this detrapping current follows a t^{-1} time dependence. Its V_t evolution would have a logarithmic time dependence ($\Delta V_t \propto \log(t)$) accordingly.

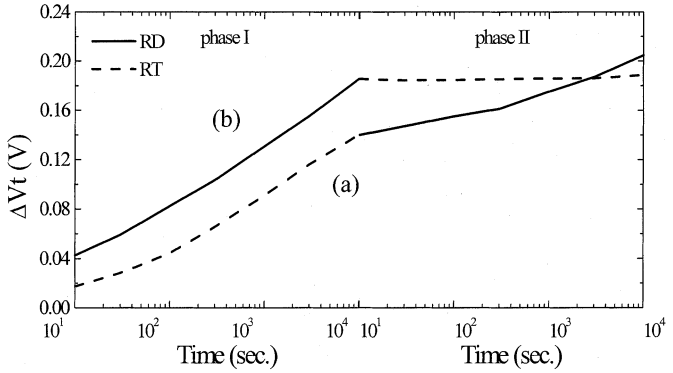


Fig. 3. Two-phase measurement of the temporal evolution V_t shift of a 10-K P/E cycled cell. In curve (a), the cell is at RT in the first 10^4 s and is at RD in the following 10^4 s. The sequence is reversed in curve (b). Bias condition of RT and RD are $V_g/V_d/V_s = 0$V, 0V, 0 V and $V_g/V_d/V_s = 3$V, 1.6V, 0 V, respectively. $L_g = 0.5$ μm.

If a sufficiently highV_g is applied (e.g., for cells belonging to the same word-line of a selected-reading cell, GD mode), an inversion layer is induced beneath the gate. The positive oxide charges will cause the inversion electrons to tunnel into the trapping nitride at such high vertical field. According to the positive charge-assisted tunneling (PCAT) model [16], this injection current ($J_{\rm cat}$ in Table II) will follow the t^{-p} law where t is the elapsed time, and p is around 0.7. The V_t shift, thus, has a power-law time dependence t^n with $n = 1 - p \approx 0.3$.

As for the read cell, in which the readV_g and V_d are applied (RD mode), channel electrons will be accelerated by the lateral field near the drain region. Both the high drain field and the positive oxide charges will enhance electron injection into nitride. This positive oxide charge-enhanced hot-electron injection will cause a positive V_t drift with the same time dependence as GD, i.e., $\Delta V_t \propto t^n$.

IV. RESULTS AND DISCUSSIONS

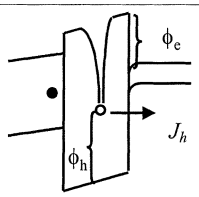
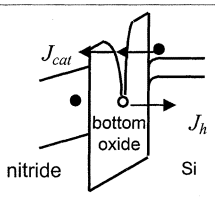
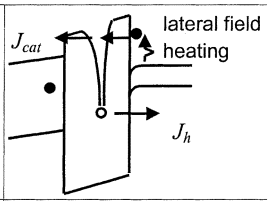
A. Bias Dependence of Read Disturb

Fig. 4 shows the GD characteristics of a 10-K P/E cycled cell. The applied gate bias is from $V_g = 0$ V (RT mode) to $V_g = 4$ V. It is found that V_t shift shows linear dependence on log(t) at $V_g = 0$ V. This has been well modeled by hole tunnel detrapping [15]. However, accelerated V_t drift, which exhibits a power-law time dependence t^n, is observed at $V_g = 4$ V. It would be clear if we show the ΔV_t versus disturb time on a log-log plot, as indicated by the open square and the right-axis in Fig. 4. Since the time evolution of V_t drift would show a power-law time dependence t^n if PCAT dominates, the accelerated V_t drift with its unique time dependence confirms that positive charge-assisted electron tunneling into the trapping nitride takes place at high vertical field, in addition to hole tunnel detrapping. The V_g dependence of ΔV_t is shown in Fig. 5.

Fig. 6 shows the RD characteristics of a 10-K P/E cycled cell with $L_g = 0.5$ μm. The drain bias is from 1.7–2.3 V, and the gate bias is 3 V. V_t shift versus drain bias is shown in Fig. 7. Since the

TABLE II

SCHEMATICS OF BAND DIAGRAMS AND CARRIER TRANSPORT MECHANISMS AT VARIOUS BIAS CONDITIONS. SOLID CIRCLES REPRESENT THE RESIDUAL ELECTRONS IN TRAPPING NITRIDE AND CHANNEL ELECTRONS IN SILICON, AND OPEN CIRCLES REPRESENT THE POSITIVE TRAPPED CHARGES IN BOTTOM OXIDE. ϕ_h AND ϕ_e REPRESENT THE HOLE AND ELECTRON TUNNELING BARRIER HEIGHTS, RESPECTIVELY. m_h AND m_e REPRESENT THE HOLE AND ELECTRON TUNNELING EFFECTIVE MASSES, RESPECTIVELY. N_h IS THE EFFECTIVE POSITIVE OXIDE CHARGE VOLUME DENSITY. THREE CARRIER TRANSPORT PATHS ARE ILLUSTRATED. (a) POSITIVE OXIDE CHARGE-TUNNEL DETRAPPING AT LOW OXIDE FIELD (J_h). (b) POSITIVE OXIDE CHARGE-ASSISTED ELECTRON INJECTION INTO NITRIDE ($J_{\rm cat}$), IN ADDITION TO J_h, AT HIGH OXIDE FIELD. (c) POSITIVE OXIDE CHARGE-ASSISTED ELECTRON INJECTION INTO NITRIDE ($J_{\rm cat}$), IN ADDITION TO J_h, AT HIGH LATERAL FIELD. HOT CARRIERS ARE GENERATED VIA LATERAL FIELD HEATING. TIME EVOLUTIONS OF THEIR INJECTION CURRENTS AND V_t SHIFTS ARE ALSO FORMULATED

Hole tunnel detrapping	Positive charge-assisted electron tunneling (PCAT)	
		
Low vertical field Low lateral field	**High vertical field Low lateral field**	**High vertical field High lateral field**
Room temp. drift Vg/Vd=0V/0V	**Gate disturb Vg/Vd=3V/0V**	**Read disturb Vg/Vd=3V/2V**
$J_h \propto \frac{N_h}{\sqrt{m_h \phi_h}} t^{-1}$ [15]	$J_{cat} \propto N_h t^{-p}$	$p = \sqrt{\frac{m_e \phi_e}{m_h \phi_h}} \sim 0.7$ [16]
$\Delta V_t^{\,h}(t) \propto \frac{N_h}{\sqrt{m_h \phi_h}} \log(t)$	$\Delta V_t^{\,cat}(t) \propto N_h t^n$	$n = 1\text{-}p \sim 0.3$

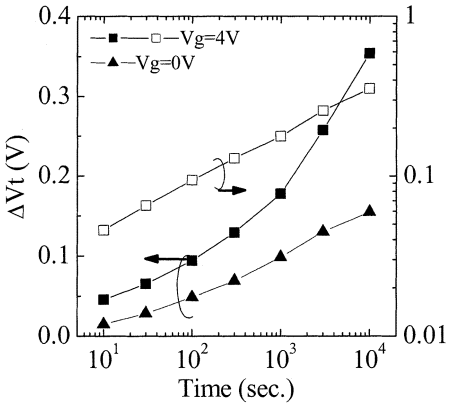


Fig. 4. V_t shift versus disturb time of a 10-K P/E cycled cell at various gate biases. The drain and source are grounded and $L_g = 0.5$ μm.

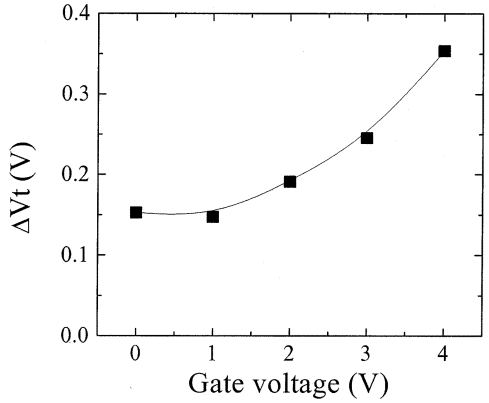


Fig. 5. V_t shift versus applied gate bias of a 10-K P/E cycled cell. The drain and source are grounded, and the disturb time is 10^4 s $L_g = 0.5$ μm.

nitride conduction band edge is 2.1 eV above the silicon conduction band edge, sufficient lateral-field heating is necessary to make the channel electrons inject into the trapping nitride, if the vertical field is low. The drastically enhanced RD found at high drain bias ($V_d = 2.3$ V) can be explained by the channel hot-electron injection into the trapping nitride. In addition, the t^n time dependence of V_t drift also indicates that PCAT process is involved. As V_d decreases, the hot-carrier effect is too weak to make the electrons inject into the trapping nitride. The V_t shift is then dominated by hole tunnel detrapping, which is the same as RT (Fig. 4, $V_g \approx 0$ V). It is shown that for $V_d < 2$ V, the V_t shift due to read disturb is almost the same (Fig. 7), and ΔV_t is proportional to $\log(t)$ (Fig. 6). Furthermore, a smaller V_t shift at $V_g/V_d = 3$ V/1.7 V than at 3 V/0 V can be explained by reduced vertical field in the former case [17].

V_d acceleration is widely used for hot-carrier lifetime projection. As shown in Fig. 8, V_d acceleration effect is observed at high V_d. However, gate-enhanced read disturb, instead, dominates at low drain bias where the hot-carrier effect is insignificant. The V_t shift is almost independent of V_d in this regime (e.g., $V_d < 2$ V with $L_g = 0.5$ μm). The extrapolated lifetime based on the results at high V_d regime will be overestimated if we use a low drain voltage during read operation, where the hot-carrier effect is very weak.

B. Channel Length Scaling Effect

It is known that the hot-carrier effect will become more serious in a short-channel device. Fig. 9 shows the RD results of three cells with gate length (L_g) of 0.5, 0.4, and 0.3 μm, respectively. Increased RD is observed in a shorter gate length cell. In addition, the temporal evolution of the V_t shift follows a $\log(t)$ time

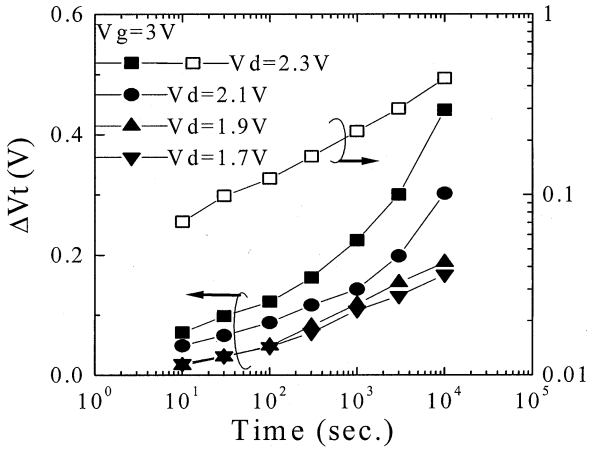


Fig. 6. V_t shift versus disturb time of a 10-K P/E cycled cell at various drain biases. $V_g/V_s = 3$ V/0 V and $L_g = 0.5$ μm.

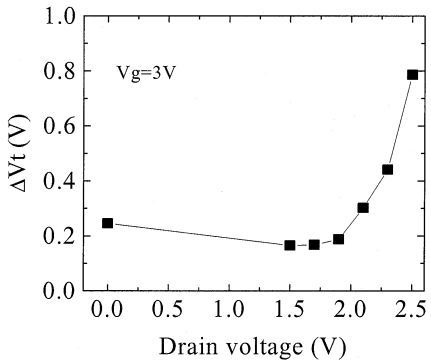


Fig. 7. Read disturb-induced V_t shift versus applied drain bias of a 10-K P/E cycled cell. The disturb time is 10^4 s $V_g/V_s = 3$ V/0 V and $L_g = 0.5$ μm.

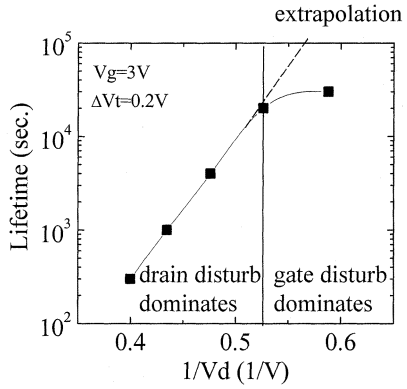


Fig. 8. Lifetime projection by V_d-acceleration approach. Lifetime is defined as the disturb time resulting in a V_t shift of 0.2 V. $V_g/V_s = 3$ V/0 V and $L_g = 0.5$ μm. As shown in the figure, lifetime is overestimated in the low-V_d regime where gate-enhanced disturb dominates.

dependence for $L_g = 0.5\,\mu$m, and exhibits a t^n time dependence for $L_g = 0.3\,\mu$m. It implies that strong hot-carrier enhanced RD dominates the V_t shift as the channel length is scaled down.

C. Temperature Effect

We also investigate the temperature effect on RD. It is reported that hot-carrier-induced gate current injection increases with decreasing temperature, even with a low drain bias (e.g., $V_d < 2$ V) [18]. Fig. 10 shows that RD is almost independent of temperature in a long-channel device ($L_g = 0.5$ μm), in which

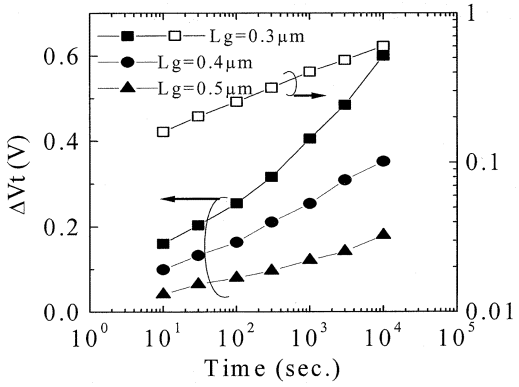


Fig. 9. V_t shift versus disturb time of 1-K P/E cycled cells with different channel lengths. $V_g/V_d/V_s = 3$ V/1.6 V/0 V.

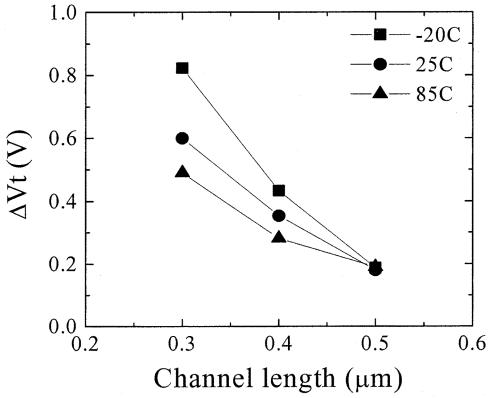


Fig. 10. Temperature effect on read disturb of 1-K P/E cycled cells. Devices with gate lengths of 0.5 μm, 0.4 μm, and 0.3 μm are characterized. The applied gate and drain biases are 3 and 1.6 V, respectively, and the disturb time is 10^4 s.

hole tunnel detrapping dominates [so it is termed as room-temperature drift (RT)]. On the other hand, enhanced RD is observed at low temperature in a shorter device ($L_g = 0.3$ μm), where hot-carrier-enhanced degradation dominates.

D. Channel Doping Effect

Channel doping is usually used to control short-channel effect and to improve hot-electron injection efficiency. It is reported that GD is worse in a high-$V_{\rm ti}$ cell [19]. RT, GD, and RD are characterized for cells with initial threshold voltages of 1.2, 2, and 3 V, respectively, in our study. During GD and RD measurements, we use $(V_g - V_{\rm ti}) = 1.5$ V, which is the same gate overdrive that conducts the same read current for each cell. The read drain bias is 1.6 V. The results are plotted in Fig. 11.

As shown in Fig. 11, two major features are observed. First, RT is almost the same for these three cells, while GD and RD increase with increased $V_{\rm ti}$ (channel doping). Second, V_t shift is strongly enhanced by V_gV_d in high-$V_{\rm ti}$ cells; however, it is less affected byV_gV_d in a low-$V_{\rm ti}$ cell. More severe RD in a high-$V_{\rm ti}$ cell is due to a stronger hot-carrier effect, since the channel doping concentration is higher. As tunneling detrapping of positive oxide charges is responsible for the V_t drift in low vertical/lateral field, RT is expected to be almost the same in these three cells (solid squares in Fig. 11). Since the same gate overdrive implies the same inversion charge density in these cells, we need to find out the cause that results in the enhanced GD in a high-$V_{\rm ti}$ cell.

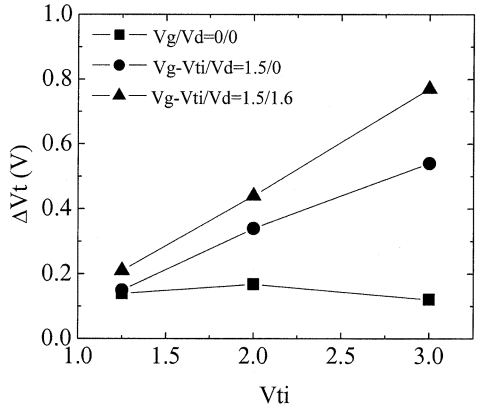


Fig. 11. Initial threshold voltage versus room-temperature drift, gate disturb, and read disturb. The cells undergo 10-K P/E cycles. The bias conditions for GD and RD are $V_g - V_{\rm ti}/V_d/V_s = 1.5$ V/0 V/0 V and 1.5 V/1.6 V/0 V, respectively, and $V_g = V_d = V_s = 0$ V for RT. The disturb time is 10^4 s and $L_g = 0.5\ \mu$m.

The oxide (vertical) field can be formulated as (without trapped charges)

$$E_{\rm ox} = \frac{V_g - V_{ti}}{T_{\rm ox}} + \frac{\sqrt{2\varepsilon_{si}(2\phi_f)qN_A}}{\varepsilon_{\rm ox}}$$

in strong inversion, where $E_{\rm ox}$ is the oxide field, $T_{\rm ox}$ is the equivalent oxide thickness of the ONO stack, N_A is the effective channel doping concentration, and ϕ_f is the potential difference between the Fermi level (with acceptor concentration of N_A) and the intrinsic Fermi level. $\varepsilon_{\rm ox}$ and ε_{Si} are the dielectric constants of oxide and silicon, respectively. Obviously, even with the same gate overdrive (V_g–$V_{\rm ti}$), the vertical field is stronger in a cell with higher channel doping N_A. The higher vertical field will enhance the charge tunneling rate [17]. This explains the larger V_t shift in a high-$V_{\rm ti}$ cell.

V. Conclusion

RD-induced V_t instability is investigated in this work. It is found that at low vertical/lateral field, tunneling detrapping of cycling-induced positive oxide charges dominates the V_t shift, which is insensitive to temperature. A hot-carrier effect (drain field heating) dominates the V_t shift in a short-channel device, especially at low temperature. Gate voltage-enhanced V_t drift occurs even in a long-channel device, and it is much worse in a high-$V_{\rm ti}$ cell. All of the results are attributed to positive oxide charges, which are created during P/E stress, that enhance electron injection into the trapping nitride. Process improvements and operational optimizations have been shown effective in suppressing these disturbs [20], [21].

References

[1] T. K. Chan, K. K. Young, and C. Hu, "A true single-transistor oxide-nitride-oxide EEPROM device," *IEEE Electron Device Lett.*, vol. EDL-8, pp. 93–95, 1987.

[2] B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, "NROM: a novel localized trapping, 2-bit nonvolatile memory cell," *IEEE Electron Device Lett.*, vol. 21, pp. 543–545, Nov. 2000.

[3] W. J. Tsai, N. K. Zous, C. J. Liu, C. C. Liu, C. H. Chen, T. Wang, S. Pan, and C.-Y. Lu, "Data retention behavior of a SONOS type two-bit storage Flash memory cell," in *IEDM Tech. Digest*, 2001, pp. 719–722.

[4] H. Tomiye, T. Terano, K. Nomoto, and T. Kobayashi, "A novel 2-bit/cell MONOS memory device with a wrapped-control-gate structure that applied source-side hot-electron injection," in *Symp. VLSI Tech. Dig.*, 2002, pp. 206–207.

[5] C. C. Yeh, W. J. Tsai, M. I. Liu, T. C. Lu, S. K. Cho, C. J. Lin, T. Wang, S. Pan, and C.-Y. Lu, "PHINES: a novel low power program/erase, small pitch, 2-bit per cell Flash memory," in *IEDM Tech. Dig.*, 2002, pp. 931–934.

[6] M. H. White, D. Adams, and J. Bu, "On the go with SONOS," *IEEE Circuits Devices Mag.*, vol. 16, pp. 22–31, 2000.

[7] M. K. Cho and D. M. Kim, "High performance SONOS memory cells free of drain turn-on and over-erase: Compatibility issue with current Flash technology," *IEEE Electron Device Lett.*, vol. 21, pp. 399–401, Oct. 2000.

[8] Y. Roizin, M. Cutman, E. Aloni, V. Kairys, and P. Zisman, "Retention characteristics of microFlash memory (activation energy of traps in the ONO stack)," in *Proc. Non-Volatile Semiconductor Memory Workshop*, 2001, pp. 128–129.

[9] E. Lusky, Y. Shacham-Diamand, I. Bloom, and B. Eitan, "Electron discharge model of locally-trapped charge in oxide-nitride-oxide (ONO) gate for NROMTM nonvolatile semiconductor memory device," in *Proc. Solid State Devices Materials Conf.*, 2001, pp. 534–535.

[10] W. J. Tsai, S. H. Gu, N. K. Zous, C. C. Yeh, C. C. Liu, C. H. Chen, T. Wang, S. Pan, and C.-Y. Lu, "Cause of data retention loss in a nitride-based localized trapping storage Flash memory cell," in *Proc. Int. Reliabil. Phys. Symp.*, 2002, pp. 34–38.

[11] M. Jannai, "Data retention, endurance and acceleration factors of NROM devices," in *Proc. Int. Reliabil. Phys. Symp.*, 2003, pp. 502–505.

[12] M. Tanaka, S. Saida, Y. Mitani, I. Mizushima, and Y. Tsunashima, "Highly reliable MONOS devices with optimized silicon nitride film having deuterium terminated charge traps," in *IEDM Tech. Digest*, 2002, pp. 237–240.

[13] T. Sugizaki, M. Kobayashi, H. Minakata, M. Yamaguchi, and Y. Tamura, "New 2-bit/Tr MONOS type Flash memory using Al_2O_3 as charge trapping layer," in *Proc. Non-Volatile Semiconductor Memory Workshop*, 2003, pp. 60–61.

[14] W. J. Tsai, C. C. Yeh, N. K. Zou, C. C. Liu, S. K. Cho, C. H. Chen, T. Wang, S. Pan, and C.-Y. Lu, "Hot carrier enhanced read disturb and scaling effects in a localized trapping storage SONOS type Flash memory cell," in *Proc. Solid State Devices and Materials Conf.*, 2002, pp. 164–165.

[15] S. Manzini and A. Modelli, "Tunneling discharge of trapped holes in silicon dioxide," in *Insulating Films on Semiconductors*. Amsterdam, The Netherlands: Elsevier, 1983, pp. 112–115.

[16] T. Wang, N. K. Zous, J. L. Lai, and C. Huang, "Hot hole Stress Induced Leakage Current (SILC) transient in tunnel oxides," *IEEE Electron Device Lett.*, vol. 19, pp. 411–413, Nov. 1998.

[17] T. Wang, N. K. Zous, and C. C. Yeh, "Role of positive trapped charge in stress-induced leakage curret for Flash EEPROM devices," *IEEE Trans. Electron Devices*, vol. 49, pp. 1016–1910, Nov. 2002.

[18] D. Esseni, L. Selmi, E. Sagiorgi, R. Bez, and B. Ricco, "Temperature dependence of gate and substrate currents in the CHE crossover regime," *IEEE Electron Device Lett.*, vol. 16, pp. 506–508, Dec. 1995.

[19] C. T. Swift, G. L. Chindalore, K. Harber, T. S. Harp, A. Holfer, C. M. Hong, P. A. Ingersoll, C. B. Li, E. J. Prinz, and J. A. Yater, "An embedded 90 nm SONOS nonvalatile memory utilizing hot electron programming and uniform tunnel erase," in *IEDM Tech. Dig.*, pp. 927–930.

[20] C. C. Yeh, W. J. Tsai, T. C. Lu, S. K. Cho, T. Wang, S. Pan, and C. Y. Lu, "A modified read scheme to improve read disturb and second bit effect in a scaled MXVAND Flash memory cell," in *Proc. Non-Volatile Semiconductor Memory Workshop*, 2003, pp. 44–45.

[21] T. Wang *et al.*, "Reliability models of data retention and read-disturb in 2–bit nitride storage Flash memory cells," in *IEDM Tech. Dig.*, 2003, pp. 169–192.

Wen-Jer Tsai was born in Hualien, Taiwan, R.O.C., on April 23, 1969. He received the B.S. and M.S. degrees in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1991, and 1993, respectively, where he is currently pursuing the Ph.D degree.

He joined Macronix International Company, Ltd., Hsinchu, in 1995 as a Device Engineer. From 1995 to 2000, he worked on simulation, modeling, and design of nonvolatile memory devices. Since 2000, he has been engaged in the development of device and reliability physics of nitride storage Flash memory technology. His research interests include device characterization and reliability physics of nonvolatile memory devices.

Chih-Chieh Yeh received the B.S. and M.S. degrees in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1997 and 1999, respectively.

In 2001, he joined Macronix International Company Ltd., Hsinchu, where he has been working on the device characterization of Flash memories.

Nian-Kai Zous received the Ph.D. degree in electronics engineering from National Chiao-Tung University (NCTU), Hsinchu, Taiwan, R.O.C., in 2002.

He joined the Macronix International Company, Ltd., Hsinchu, in 2003, working in the Advanced Device Group of the Device Technology Division. His current research activities include the study of reliability issues in nitride storage devices.

Chen Chin Liu was born in Taiwan, R.O.C., in 1968. He received the B.S. and M.S. degrees in electronic engineering from National Cheng-Kung University (NCKU), Tainan, Taiwan.

In 1996, he joined the Nonvolatile Memory Technology Department of Macronix International Company, Ltd., Hsinchu, Taiwan. Until 1999, he was engaged in development of 0.25-μm nitride storage Flash memory technology served for 128-Mb Flash memory product.

Shih-Keng Cho received the M.S. degree in electronics engineering from National Cheng-Kung University (NCKU), Tainan, Taiwan, R.O.C., in 1997.

He joined the Macronix International Company, Ltd., Hsinchu, Taiwan, in 1997, working in the Flash Technology Department. He is currently engaged in the development of 0.25-μm nitride storage Flash memory technology served for Flash memory product.

Tahui Wang (M'86–SM'94) was born in Taoyuan, Taiwan, R.O.C., on May 3, 1958. He received the B.S.E.E. degree from National Taiwan University, Taipei, Taiwan, in 1980 and the Ph.D. degree in electrical engineering from the University of Illinois, Urbana-Champaign, in 1985.

From 1985 to 1987, he was with Hewlett-Packard Laboratories, Palo Alto, CA, where he was engaged in the development of GaAs HEMT devices and circuits. Since 1987, he has been with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, where he is currently a Professor. His research interests include hot-carrier phenomena characterization and reliability physics in VLSI devices, RF CMOS devices and nonvolatile semiconductor devices.

Dr. Wang was given the Best Teacher Award by Taiwan's Ministry of Education. He has served as technical committee member of many international conferences, among them IEDM, IRPS, and VLSI-TSA.

Samuel C. Pan (S'83–M'87) received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, R.O.C., in 1980, and the M.S. and Ph.D. degrees in electrical engineering from the University of Illinois, Urbana-Champaign, in 1984 and 1986, respectively.

From 1983 to 1986, he was a Research Assistant in the Solid State Electronics Laboratory, University of Illinois. In 1987, he joined Intel Corporation, Santa Clara, CA, as a Senior Device Physicist, working on 0.8-μm Flash EPROM development and 0.6-μm CMOS process development. In 1995, he became Staff Circuit Designer and worked on 0.25-μm Pentium/Pro microprocessors with the focus on cache memory and PLA design. At the end of 1996, he moved back to Taiwan, and joined Macronix International Company, Ltd., Hsinchu, Taiwan, as QR Deputy Director. In 1999, he was named TD Director to lead process development for 0.18–0.15-μm Flash and mask ROM memory technologies. In June 2003, he joined Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC), Hsinchu, as the Director of Advanced Product Engineering. His current interests include device physics, device/Flash cell reliability, and methodologies for technology development and yield enhancement.

Dr. Pan is a member of Phi Kappa Phi and Eta Kappa Nu.

Chih-Yuan Lu (M'77–SM'84–F'94) received the B.S. degree from National Taiwan University, Taipei, Taiwan, R.O.C., in 1972, and the M.A., M.Ph., and Ph.D. degrees from Columbia University, New York, NY, in 1974, 1975, and 1977, respectively, all in physics.

From 1978 to 1983, he was an Associate Professor and was promoted to Full Professor in National Chiao-Tung University, Hsinchu, Taiwan. In 1983, he was with North Carolina State University, Raleigh, as a Visiting Associate Professor and Adjunct Research Staff Member of the Microelectronic Center of North Carolina (MCNC), Research Triangle Park. In 1984, he joined AT&T Bell Laboratories, where he was engaged in very high voltage bipolar-CMOS-DMOS (BCDMOS) IC technology for telecommunication applications, CMOS DRAM technology, laser programmable redundancy, and submicron CMOS ULSI technology. He joined the Electronics Research and Service Organization, Industrial Technology Research Institute, Hsinchu, (ERSO/ITRI) in late 1989 as a Deputy General Director responsible for semiconductor and integrated circuit operation, especially the Grand Submicron Project. This project later successfully developed Taiwan's first 8-in CMOS submicron manufacturing technology with high-density DRAM/SRAM as technology vehicles. In late 1994, he was the cofounder of Vanguard International Semiconductor Corporation, Hsinchu, which is a spinoff memory IC Company from ITRI's Submicron Project. He was the Vice President of Operations, Vice President of Research and Development, and later President from 1994 to 1999. He brought Vanguard from a research and development laboratory to a U.S. $400 million sales company and went IPO in 1998. He is currently Chairman and CEO of Ardentec Corporation, Hsinchu, a VLSI testing service company, and also serves Macronix International Company (MXIC), Ltd., Hsinchu, as a Senior Vice President/CTO. He led MXIC's technology development team to successfully achieve the state-of-the-art nonvolatile memory technology and embedded SoC technology, now, MXIC is the top nonvolatile semiconductor company in Taiwan. He has published more than 100 technical papers and has been granted 123 international patents. He also authored more than 30 articles in science education and R&D policy in magazines and newspapers. He served as the President of *Science Monthly* from 1978 to 1983.

Dr. Lu was the Executive Secretary and Managing Director of the Board and Board Director since 1998 for the Physical Society of R.O.C. from 1981 to 1984. He has been Vice-Chairman and then Chairman of IEEE Electron Devices Society, Taipei Chapter, from 1991 to 1996, and Board Director and Supervisor of IEEE Section since 1996. He is a member of many honor societies, including Sigma Pi Sigma, Phi Tau Phi, and Phi Lambda. He is a life member of the American Physical Society, the Physical Society of ROC, the Chinese Institute of Engineers, and CIE-USA. He received the National Science and Technology Achievement Award from the Prime Minister of Taiwan, R.O.C., in 1994. In 1995, he was awarded the National Invention Award, and in 2002, he was awarded the most prestigious semiconductor award in Taiwan—the Pan Wen Yuan Award.