Abnormal ESD Failure Mechanism in High-Pin-Count BGA Packaged ICs Due to Stressing Nonconnected Balls

Wen-Yu Lo and Ming-Dou Ker, *Senior Member, IEEE*

***Abstract*—An abnormal failure mechanism due to ESD pulse applied on the nonconnected (NC) solder balls of a high-pin-count (683 balls) BGA packaged chipset IC is presented. The ESD test results of the IC product were found below human-body-model (HBM) 2 kV when stressing all balls or only stressing NC balls, but above HBM 3 kV when stressing all balls excluding NC balls. Failure analyses, including scanning electron microscopy (SEM) photographs and the measurement of current waveforms during ESD discharging event, have been performed. With a new proposed equivalent model, a clear explanation on this unusual phenomenon is found to have a high correlation to the small capacitor method (SCM). Several solutions to overcome this failure mechanism are also discussed.**

***Index Terms*—Ball grid array (BGA), charged-device model (CDM), electrostatic discharge (ESD), scanning electron microscopy (SEM), small capacitor method (SCM).**

I. Introduction

THE trend of IC technology is toward smaller device dimension and higher integrated density. The ability of more function blocks integrated into a single chip, which includes a large amount of input/output signals, makes rapid progress of IC packages to have high pin counts. Many types of IC packages have been developed for this trend, such as the quad flat package (QFP), the pin grid array package (PGA), and the ball grid array package (BGA). With the increase of IC pin counts, IC products suffer higher failure possibility to electrostatic discharge (ESD) hazards during assembling, handling, and testing. In order to improve the ESD immunity of IC products, much attention has been paid to the design and failure analyses of the on-chip ESD protection circuits. But the relation between ESD damages and the IC packages has seldom been discussed. A few reports have shown the package-related ESD issues caused by ESD pulses applied on the nonconnected (NC) pins [1], [2]. However, there are still neither clear analyses nor good understanding of this kind of failure mechanism.

In this paper, the ESD-damaged event on the neighboring signal balls when the human-body-model (HBM) ESD pulses applied on NC balls of a 683-pin wired-bond BGA packaged IC is presented. These ESD-protected signal balls in the neighborhood of the NC balls can sustain higher than 3-kV HBM ESD level when the ESD pulses are directly applied on them. But some of them will fail below 2-kV HBM ESD stress when the ESD pulses are applied on the NC balls with respect to VSS or VDD grounded. The failure mechanism of this event is quite different from the traditional HBM ESD damage. With a new proposed equivalent model, the measurement of current waveforms under ESD pulse condition, and the failure points found by scanning electronic microscopy (SEM), a high correlation between this failure mechanism and the small capacitance method (SCM) [3] has been found. This high correlation gives a clear explanation of this unusual event. Therefore, the ESD protection solutions to overcome such abnormal failure mechanism can be developed to successfully prevent such damages in the high-pin-count BGA ICs.

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II. ESD Damages Induced by NC Balls

A. NC Balls in BGA Packaged ICs

The 683-pin wired-bond BGA packaged chipset IC was fabricated with 0.18-μm logic CMOS technology. The cross-sectional view and the top and bottom photographs of the 683-pin BGA packaged IC are shown in Fig. 1(a) and (b), respectively. The signal or power/ground pads on silicon dies are connected to the solder balls on the package surface through the Au wires and the traces in the package substrate. NC balls are reserved in the BGA package for further function extension of the next-generation products. These NC balls exist with only solder balls on the package and short traces in the package substrate, without bond wires connecting to the dies.

B. ESD Tests With NC Balls

According to the HBM [4] and machine-model (MM) [5] ESD test standards, these NC balls are currently not necessary to be stressed. But, in real-world conditions, the NC balls can be possibly touched by ESD hazards. Thus, these NC balls are treated as signal balls in our ESD qualification procedures. The ESD test results of the BGA packaged IC were found below HBM 2 kV, but above MM 300 V. The failure criteria on these IC products are judged by the auto test equipment (ATE) with the electrical and function specifications. Leakage or short-circuit failures were found in some signal balls of a high-speed data bus. To clarify that these ESD failures of signal balls were indeed induced by the NC balls, several sets of ESD test experiments were performed, as the following: 1) when only the NC

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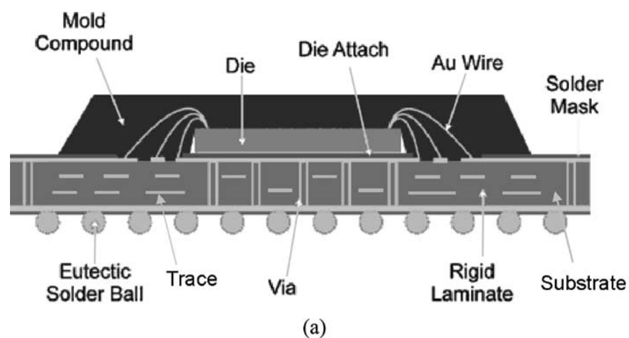
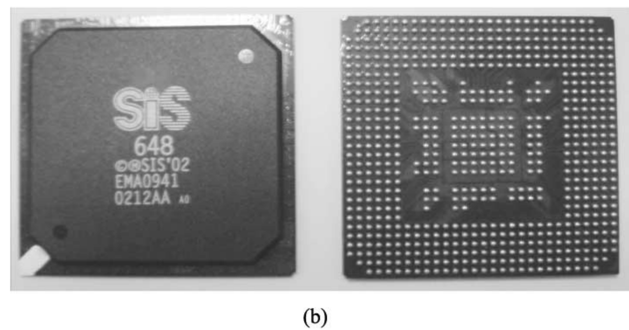


(a)



(b)

Fig. 1. (a) The cross-sectional view and (b) the top and bottom photographs of the 683-pin BGA packaged chipset IC.

TABLE I
ESD TEST RESULTS OF THE CHIPSET IC WITH DIFFERENT ESD STRESS COMBINATIONS ON THE SIGNAL OR NC BALLS

Stress Method	HBM	MM
Stress on all balls	< 2kV	> 300V
Stress only on NC balls	< 2kV	
Stress excluding NC balls	> 3kV	> 300V

balls were stressed under the ESD test, the leakage or short-circuit failures would be found in some of these signal balls that located in the neighbor of the NC balls with HBM level less than 2 kV; 2) when ESD pulses were applied on all the balls of the ICs excluding these NC balls, the HBM ESD level of the whole chip could pass 3 kV. The results of the MM ESD tests seem not to be influenced by the NC balls. The ESD test results among these ESD test experiments are summarized in Table I. Both positive and negative polarities of ESD pulses applied on NC or signal balls with respect to VSS or VDD balls grounded are all considered in these experiments. The ESD result of each test experiment shown in Table I is the worst case absolute value among the various test results of all stress combinations with positive and negative ESD pulses. From these results, it has been confirmed that the NC balls do indeed induce ESD failures on the signal balls during the HBM ESD test.

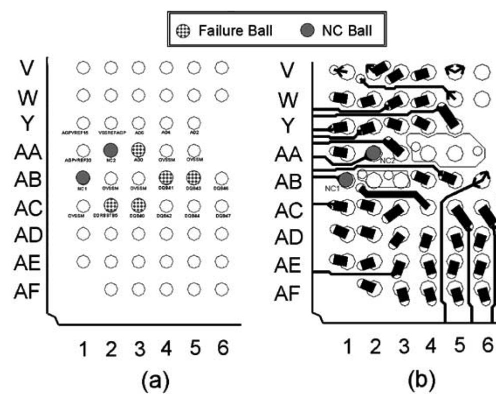


Fig. 2. (a) The ball assignment and (b) the trace layout of the NC and failure signal balls in the BGA packaged IC.

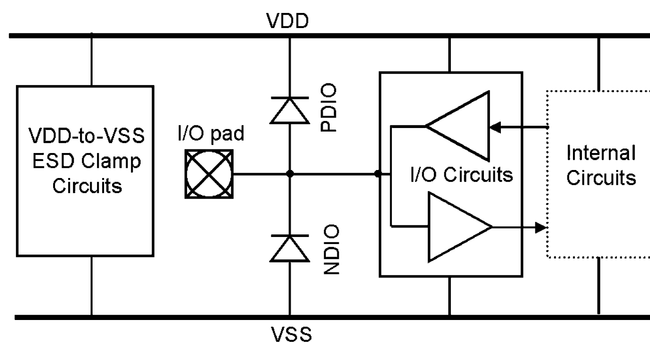
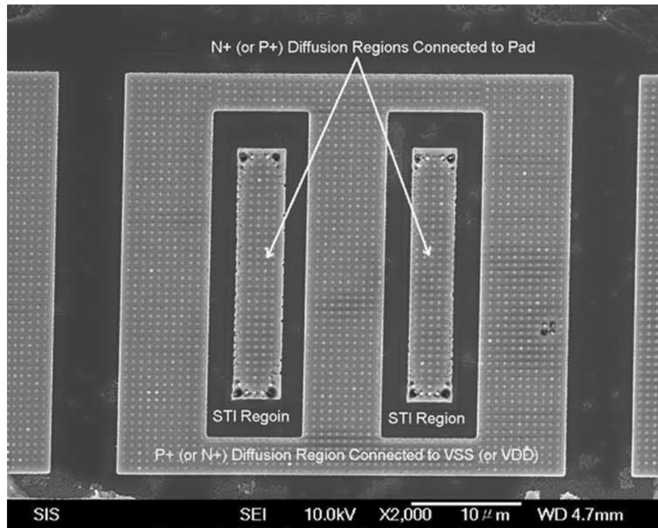


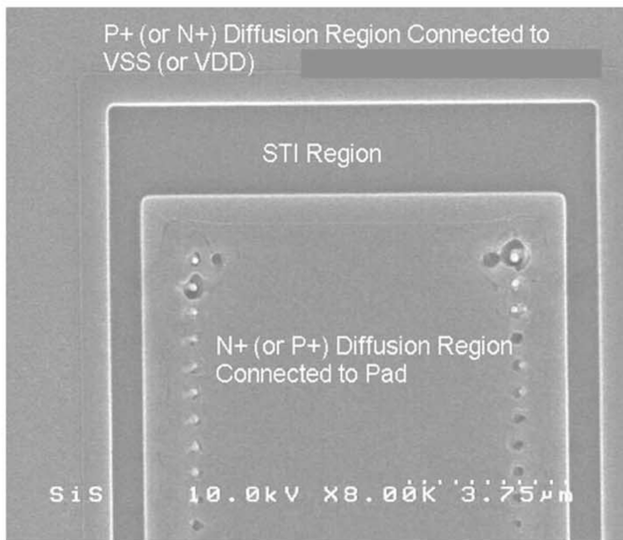
Fig. 3. Schematic view of on-chip ESD protection and I/O circuits of the signal balls.

C. ESD Failures Induced by the NC Balls

The drawing of the ball assignment/location and the trace layout related to the NC and failure signal balls are shown in Fig. 2(a) and (b), respectively. As shown in Fig. 2, the failure balls are located around the neighbor of the NC balls or with their traces close to NC balls, and the minimum space between two adjacent traces is only 50 μm. The schematic view of the ESD protection circuits for these signal balls is shown in Fig. 3. The I/O ESD protection scheme of these signal balls is formed by the low-capacitance diodes in conjunction with the VDD-to-VSS ESD clamp circuits [6], [7]. The diodes are p+ diffusion in n-well (PDIO) and n+ diffusion in p-well (NDIO) shallow trench isolation (STI) bounded diodes. Fig. 4(a) and (b) shows the SEM pictures of failure points on these diodes. Contact destructions on the diodes are found around the boundaries between the diffusion and the STI regions, especially around the corners of the diffusion regions that connected to the signal pad. ESD failures at the corners of the STI bounded diodes caused by HBM ESD pulses have also been reported in earlier literature [8]–[10] due to the results of high current density and thermal heating. This kind of damage induced by HBM ESD pulses applied on NC balls would be the same cause of high current density and thermal heating, however, the HBM ESD immunity of this unusual event with NC balls (below 2 kV) and the normal ESD test without NC balls (above 3 kV) is quite different. Thus, the failure mechanism in this event should be different from that in the normal ESD test condition. Gate ruptures also have been found



(a)



(b)

Fig. 4. (a) The SEM picture and (b) the zoomed-in picture of the contact destructions of input ESD diodes induced by ESD pulse applied on the NC balls.

on the output driving MOS devices, as that shown in Fig. 5. The damage points in Fig. 5 are quite different from the traditional HBM ESD damages on the output driving MOS devices, which are usually the destruction of drain diffusions or breakdown between drain and source diffusions as those shown in [10].

III. Failure Analyses and Protection Solutions

A. Simplified Model and Verification

A simplified model to explain the relationship between the NC balls and the failure signal balls under the HBM ESD test is proposed and shown in Fig. 6. The C_M represents the lumped parasitic capacitor between the trace of the NC ball and the trace of the signal ball. The $C_{\rm NC}(C_S)$ is the lumped parasitic capacitor between the trace of the VSS ball and the trace of the NC ball (signal ball). For convenience of analysis, lumped equivalent circuits of these parasitic capacitors were considered in

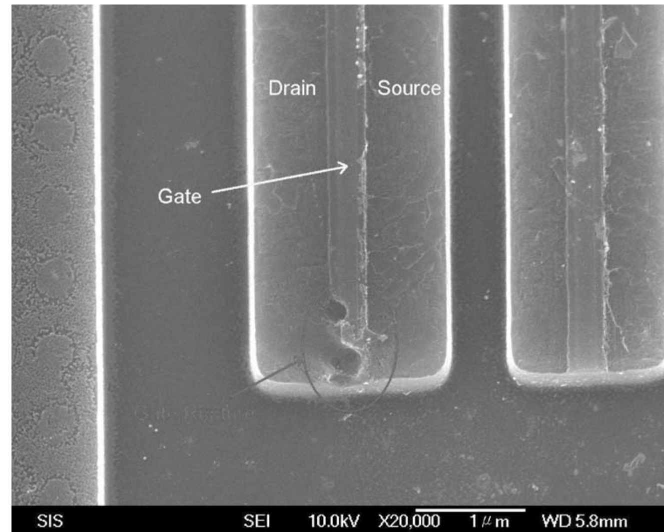


Fig. 5. SEM picture showing the gate of the output driving MOS rupturing due to HBM ESD pulse applied on the NC balls.

this model instead of distributed ones. Thus, the capacitances of these lumped equivalent capacitors were decided by the location of balls and the distance between traces. The equivalent circuit of ESD protection and I/O circuits of the signal ball under the ESD pulse condition was simplified as a variable resistor R_{SB}, because the ESD clamp device into its snapback or breakdown region has a low impedance path to discharge the ESD current. The capacitor $C_{\rm ESD}$, resistor $R_{\rm ESD}$, two-port switch, and the high-voltage pulse generator form the equivalent circuit of the HBM or MM ESD tester. The capacitance of $C_{\rm ESD}$ is 100 pF for HBM and 200 pF for MM. The resistance of $R_{\rm ESD}$ for HBM and MM is 1500 and 0 Ω, respectively. For simplicity, only the case of ESD pulse applied on the NC ball with respect to the grounded VSS ball is considered in this model. The case of ESD pulse applied on the NC ball with respect to grounded VDD ball can be analyzed in a similar way by replacing the VSS ball in Fig. 6 with VDD ball. The considered signal ball in this model is floating because the ESD pulse is applied to the NC ball. During the ESD test, the capacitor $C_{\rm ESD}$ will be charged to an initial voltage (at $t = 0$), $V_{\rm ESD}(0)$, by the high voltage pulse generator first. Then, the charged capacitor $C_{\rm ESD}$ will be discharged to the NC ball by the control of the two-port switch.

In order to get a clearer insight of the failure mechanism, the expressions of the voltage $V_{\rm NC}(t)$ on the NC ball and the current $i_{\rm ESD}(t)$ through the discharging loop during the discharging period are derived. Fig. 7(a) shows the equivalent circuit of the simplified model. For convenience of the derivations and analyses, two assumptions have been made. The first assumption is that the variable resistor R_{SB} is large enough to take as open circuit, as shown in Fig. 7(b), before the ESD overstress reaches to this ESD clamp device. The second assumption is that the variable resistor R_{SB} is small enough to be taken as short circuit, as shown in Fig. 7(c), after the ESD overstress reaches to the ESD clamp device of the signal ball. The capacitor C_X is used to stand for the total capacitance between the NC and VSS balls. The capacitance of C_X should be much smaller than that

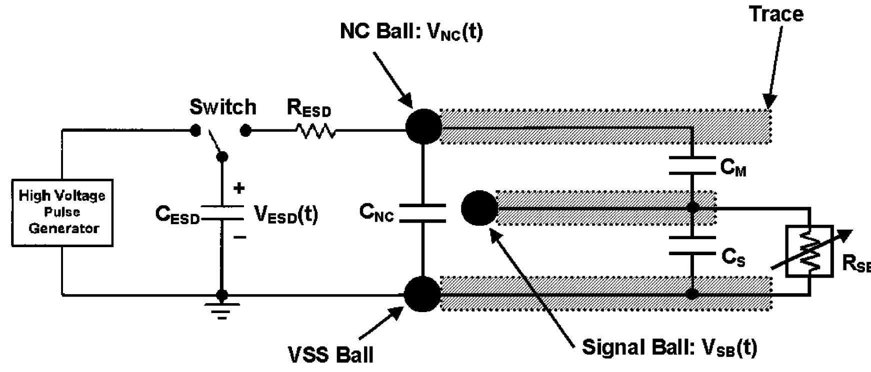


Fig. 6. Simplified model proposed to explain the relationship between the NC ball and the signal ball under HBM or MM ESD pulses applied on the NC ball. The variable resistor R_{SB} is used to stand for the ESD protection and I/O circuits of the signal ball under this condition.

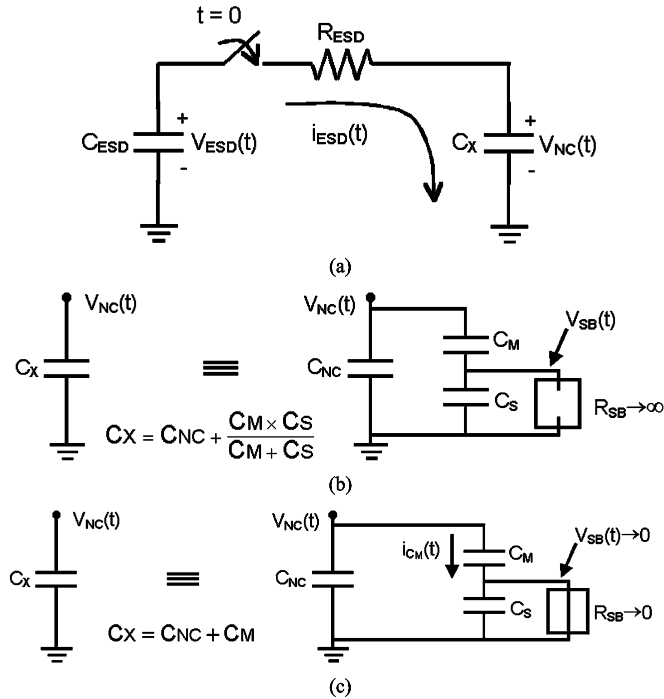


Fig. 7. (a) The equivalent circuit of the proposed simplified model. The capacitor C_X is used to stand for the equivalent capacitor between the NC and VSS balls. (b) The relationship between the equivalent capacitor C_X and the simplified model under the assumption $R_{SB} \rightarrow \infty$. (c) The relationship between the equivalent capacitor and the simplified model under the assumption $R_{SB} \rightarrow \infty$.

of $C_{\rm ESD}$ ($C_{\rm ESD} = 100$ pF for HBM). The expressions of the capacitance of C_X in these two cases are shown in (1) and (2):

$$C_X = C_{\rm NC} + \frac{C_M \times C_S}{C_M + C_S} \quad \text{as } R_{SB} \rightarrow \infty \tag{1}$$

$$C_X = C_{\rm NC} + C_M \quad \text{as } R_{SB} \rightarrow 0. \tag{2}$$

The expressions of the voltage on the NC ball, $V_{\rm NC}(t)$, and the current through the discharging loop, $i_{\rm ESD}(t)$, during the discharging period can be found in (3) and (4), where the time constant τ is expressed in (5).

$$V_{\rm NC}(t) = \left(\frac{C_{\rm ESD} \times V_{\rm ESD}(0)}{C_{\rm ESD} + C_X}\right)\left(1 - \exp^{-t/\tau}\right), \quad t \geq 0 \tag{3}$$

$$i_{\rm ESD}(t) = \left(\frac{C_{\rm ESD} \times V_{\rm ESD}(0)}{C_{\rm ESD} + C_X}\right)\left(\frac{1}{R_{\rm ESD}}\right) \times \exp^{-t/\tau}, \quad t \geq 0 \tag{4}$$

$$\tau = R_{\rm ESD} \times C_X. \tag{5}$$

In the case of $R_{SB} \rightarrow \infty$, the voltage on the signal ball during the ESD pulse applied to the NC ball would be

$$V_{SB}(t) = \left(\frac{C_M}{C_M + C_S}\right)\left(\frac{C_{\rm ESD} \times V_{\rm ESD}(0)}{C_{\rm ESD} + C_X}\right)\left(1 - \exp^{-t/\tau}\right), \quad t \geq 0. \tag{6}$$

The energy stored in the capacitor C_S during the discharging process would be

$$E_{CS} = \frac{1}{2} C_S {V_{SB}}^2. \tag{7}$$

From (6), the smaller C_S and the larger C_M will cause the higher voltage V_{SB} on C_S. From (6) and (7), the dominant factors affect the energy stored on C_S would be V_{SB}, which is strongly dependent on the C_M and $V_{\rm ESD}(0)$. The time constant τ affects the period of time for $V_{SB}(t)$ to reach its steady state. The energy stored on C_S would be finally dissipated by the ESD protection devices or I/O circuits, when some of the devices were broken down or turned on to make the variable resistor R_{SB} decreasing. Thus, the energy stored in C_S (when the ESD pulse is applied on the NC ball) can be taken as an index of the quantity of energy that is applied to the signal ball in this process. The higher energy stored in C_S will cause higher risk to damage the signal ball.

In another case of $R_{SB} \rightarrow 0$, most of the transient current $i_{CM}(t)$ during the ESD pulse applied on the NC ball will flow through the small resistor R_{SB}. The expression of the transient current $i_{CM}(t)$ is derived in (8).

$$i_{CM}(t) = \left(\frac{C_M}{C_{\rm NC} + C_M}\right) \times \left(\frac{C_{\rm ESD} \times V_{\rm ESD}(0)}{C_{\rm ESD} + C_X}\right) \times \left(\frac{1}{R_{\rm ESD}}\right) \times \exp^{-t/\tau}. \tag{8}$$

The power dissipated on the resistor R_{SB} (when the transient current $i_{CM}(t)$ flowing through R_{SB}) can be expressed as

$$P_{R_{SB}} = i_{CM^2} \times R_{SB}. \tag{9}$$

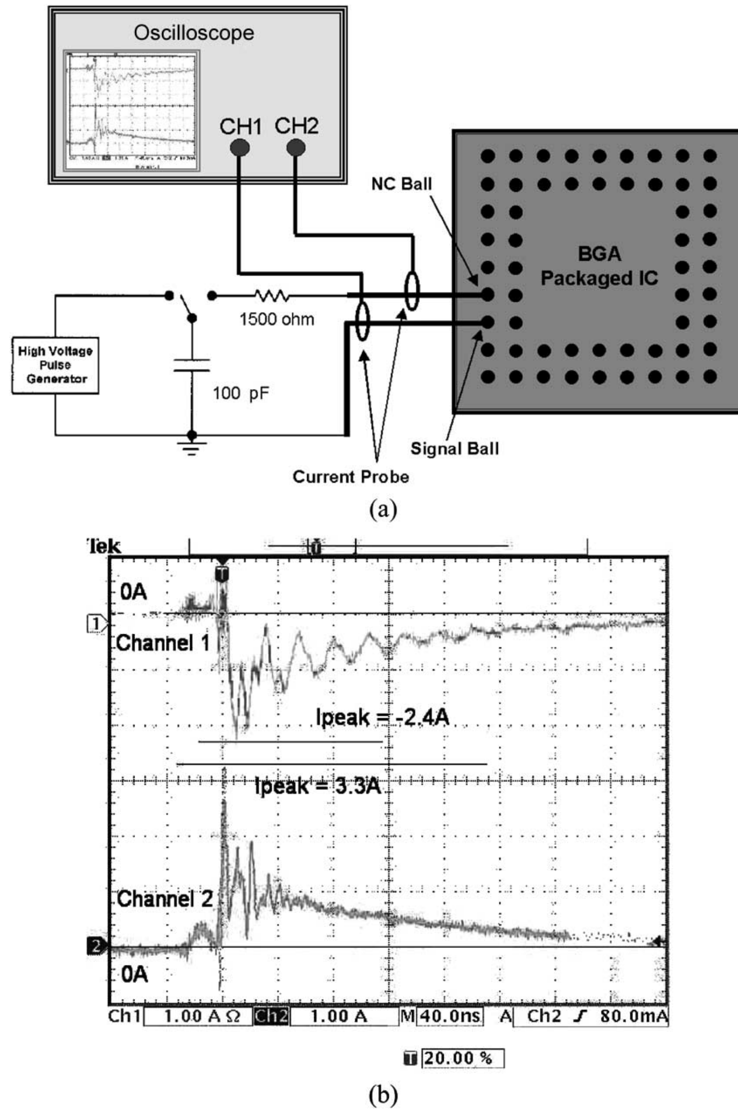


Fig. 8. (a) The experimental setup used to measure the current waveforms between NC and signal balls under HBM ESD pulse applied on the NC ball with signal ball grounded. (b) The measured current waveforms under HBM 2-kV ESD stress. Channel 1 is the current waveform flowing out from the signal ball, and channel 2 is the current waveform flowing in the NC ball.

From (8), the peak value of the transient current $i_{CM}(t)$ is dominated by the voltage $V_{\rm ESD}(0)$, the resistance of $R_{\rm ESD}$, and the capacitance of C_M. The time constant τ affects the time period of $i_{CM}(t)$ decayed from its peak value to zero. From (5), the time constant τ is inversely proportional to $R_{\rm ESD}$. Thus, a small value of $R_{\rm ESD}$ will lead to a high peak value of transient current, but the current pulse will disappear very soon, which is similar to the CDM ESD current waveform of high current peak within a very short discharging period. If the dissipated power in (9) is integrated with respect to time, it can be found that the main factors affecting the energy dissipated on the resistor R_{SB} when ESD pulse is applied on the NC ball are C_M and $V_{\rm ESD}(0)$.

In real conditions, the equivalent resistance of R_{SB} of the signal ball when ESD pulse is applied on the NC ball would be variable and between these two extreme cases. However, from the above two extreme cases of assumptions, the main factors that affect the energy dissipated on the signal ball when ESD pulse is applied on the NC ball are all C_M and $V_{\rm ESD}(0)$. In fact, the results of the above derivations can explain why signal balls usually fail with their locations or their traces close to the NC balls/traces in the HBM ESD test only. Because of the lower $V_{\rm ESD}(0)$ of the MM ESD test, the NC ball induced damage is not found in the MM ESD testing.

In order to investigate the possible ESD currents between the NC and signal balls under HBM ESD pulses applied on the NC ball, the experimental setup shown in Fig. 8(a) is performed. To monitor the current waveform of the signal ball, this signal ball is terminated to ground. The ESD pulse voltage applied to the NC ball is $+2$ kV. A significant current was observed flowing out the grounded signal ball, as shown in Fig. 8(b). The peak currents measured at the NC ball's input (CH2) and the signal ball's output (CH1) are $+3.3$ A and -2.4 A, respectively. The negative sign of the current stands for the direction of current flowing out from the signal ball.

Another experimental setup, provided in Fig. 9(a), is used for comparison with that in Fig. 8(a). $+2$-kV HBM ESD pulse was directly applied on the signal balls with the VSS ball grounded. The NC ball was connected to ground for monitoring the cur-

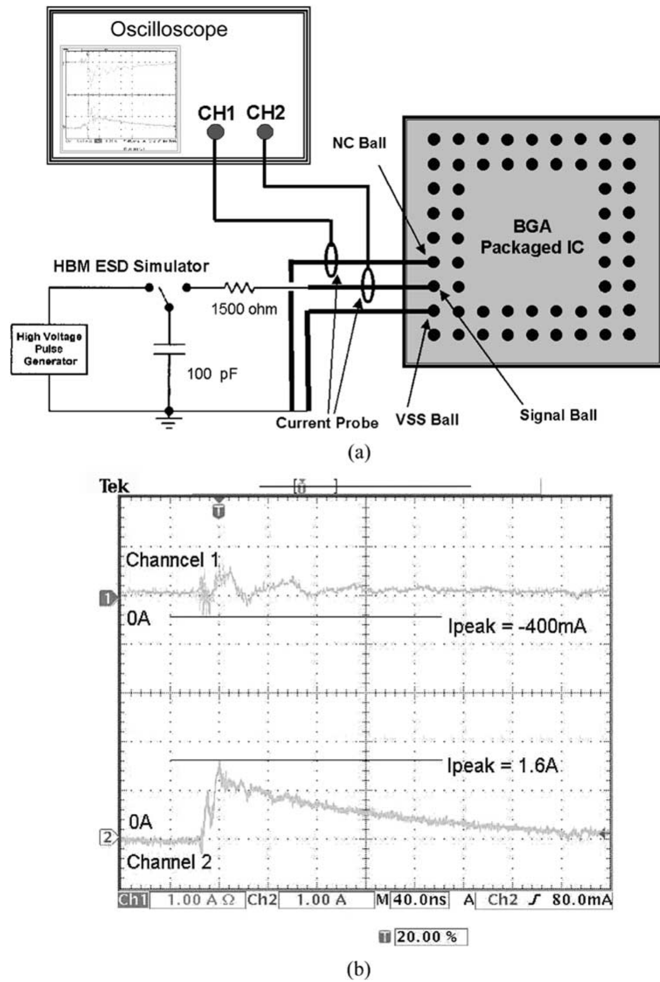


Fig. 9. (a) The experimental setup used to measure the current waveforms between NC and signal balls under HBM ESD pulse applied on the signal ball with VSS and NC balls grounded. (b) The measured current waveforms under HBM 2-kV ESD stress. Channel 1 is the current waveform flowing out from the NC ball, and channel 2 is the current waveform flowing in the signal ball.

rent waveform. No significant current was observed flowing out from the NC ball, as shown in Fig. 9(b). The peak currents measured at the signal ball's input (CH2) and the NC ball's output (CH1) are $+1.6$ A and -400 mA, respectively.

From the results of the above two experiments, it can be proved that a current path exists between the NC and signal balls due to the voltage transient occurring across the parasitic capacitor C_M. In the case of ESD pulse applied on the NC ball, due to no direct device to clamp the ESD transient voltage on the NC ball, the current flowing out from the signal ball has a significant high peak current (-2.4 A) and a short duration (<40 ns) of the high current range. On the contrary, the small current (-400 mA) flowing out the NC ball is observed in Fig. 9 during the ESD pulse applied on the signal ball, where the ESD transient voltage can be clamped by the I/O ESD protection devices.

B. Correlation With Small Capacitance Method (SCM)

The ESD results of the signal balls can pass the HBM ESD stress of 3 kV when the ESD pulses are directly applied on them, but fail at the 2-kV HBM ESD stress when the ESD pulses are applied on the NC ball. From (6) and (7), the energy dissipated

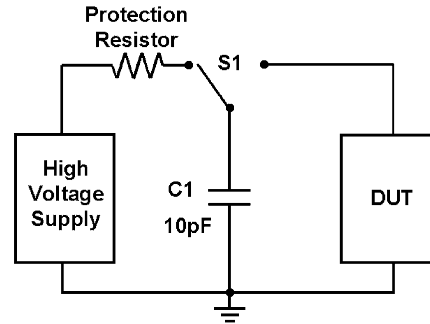


Fig. 10. Equivalent circuit of the SCM proposed in [3], which is used as an evaluation method for the charged-device model (CDM) ESD event.

in the resistor R_{SB} due to ESD pulse applied on the NC ball would be smaller than the energy dissipated in the ESD devices or I/O circuits of the signal ball when the signal ball is directly stressed by ESD pulses. The damage points of the failure signal balls shown in Fig. 4 and Fig. 5 are different from the traditional ESD damages directly induced by HBM test. Thus, the failure mechanism of this event would be different from the HBM and MM ESD failures.

From the equivalent circuit of the proposed model in Fig. 7, the transient ESD current $i_{\mathrm{ESD}}(t)$ when ESD pulse is applied on NC ball charges C_S through C_M to a voltage level. The energy stored on C_S has been expressed in (7). The electrostatic charges stored on C_S (gained from ESD pulse applied on NC ball) is discharging along the trace and bond wire to the on-chip ESD protection devices or I/O circuits of the signal ball. This transient process to make ESD destruction on the signal ball is found to be similar to that of the SCM [3]. The SCM is an ESD evaluation method for the charged device model (CDM) ESD event. The equivalent circuit of the SCM method is shown in Fig. 10. A 10-pF capacitor is charged by a high-voltage supply to such as 1000 V, and then discharged to the device under test (DUT) through a very low-impedance path. The current waveform, voltage to fail, and the failure modes of DUT due to the SCM are found to be similar to that of CDM testers [3]. Both the current waveforms of SCM and CDM have high peak current, fast rise time, and short discharging duration. The failure modes induced by SCM reported in [3] are mainly junction destructions (energy destruction) around the contacts, or the ruptures of the gate oxide (electric-field destruction), due to localized heat dissipation or high transient voltage. The parasitic capacitor C_S during ESD pulse applied on the NC balls has the equivalent function to the 10-pF capacitor in the SCM method. Although the parasitic capacitor C_S may not be 10 pF as that in the SCM method, the SEM pictures of failure points induced by SCM or ESD on the NC ball are compared in Fig. 11(a) and (b), where a high similarity is found. The failure pictures of CDM-induced ESD damages on gate oxide in [11] and [12] are very similar to that shown in Fig. 11(b), which are induced by HBM ESD pulse applied on the NC ball. This high correlation between ESD damages induced by NC ball and those induced by the SCM method (to simulate CDM ESD event) can be used to explain why the signal balls can withstand the 3-kV HBM ESD stress on themselves, but fail when 2-kV HBM ESD pulses are applied on the NC balls. The failure mechanism induced by HBM ESD pulse

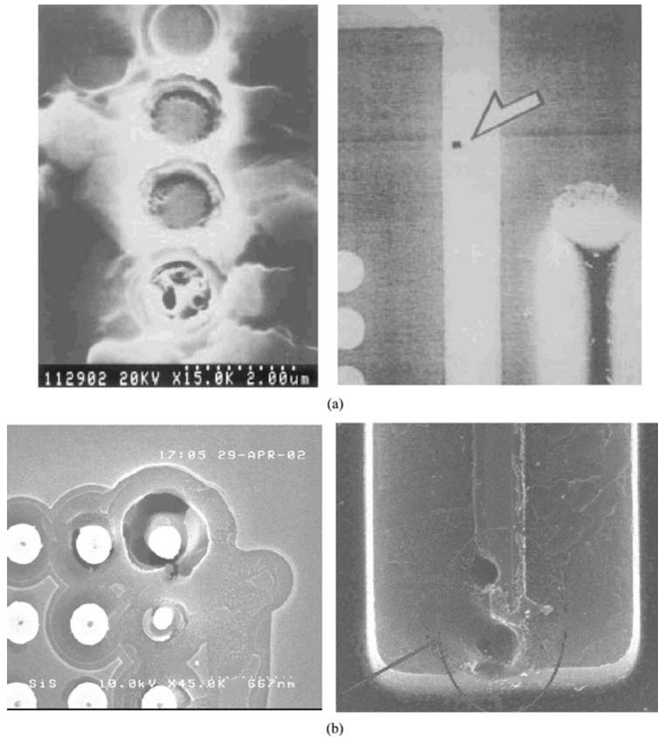


Fig. 11. (a) The SEM pictures of the junction destruction induced by SCM and gate-oxide rupture induced by CDM [3]. (b) The SEM pictures of the junction destruction and gate-oxide rupture induced by HBM ESD pulse applied on the NC ball.

applied on the NC ball is very similar to SCM or CDM ESD induced damages, which are caused by high peak and short duration of ESD current pulse.

C. Protection Solutions

From many ESD test results and failure analyses, two directions to prevent ESD damages induced by NC ball are listed below. According to these two directions, several methods are proposed to solve this NC ball induced problem.

1) Reducing the Voltage or Charges Coupled to C_s Under ESD Pulse Condition: Reducing the voltage or charge coupled to C_S means to reduce the energy stored in C_S that may cause damage to the signal balls. From the simplified equivalent circuit shown in Fig. 6, increasing the capacitance of $C_{\rm NC}$ or decreasing the capacitance of C_M can reducing the voltage or charge coupled to C_S under the ESD stress conditions. Inserting the VDD or VSS guard traces around the NC ball and its trace is an efficient way to prevent ESD damages induced by the NC ball. Separating the NC ball and its trace far away from other signal balls is also a way to increase the failure threshold of the NC ball induced ESD damages. The most efficient way for reducing the voltage or charges coupled on C_S is to directly connect the NC ball to VDD or VSS in the package through traces or bond wires, but it is not an NC ball anymore. In fact, by using the VDD or VSS guard traces, the ESD immunity of the high-pin-count BGA packaged IC has been improved to above HBM 3 kV. The ESD immunity of MM ($>$300 V) is not affected by the NC balls, because the pulse voltage of MM ESD stress is not as high as that (2000 V) of HBM ESD stress to couple enough electrostatic charges on C_S to destroy the signal ball.

2) Improving the Current Conduction Efficiency of ESD Devices Under High Peak and Fast Transient Condition : Due to the high peak current and fast transient of the current waveform induced by the ESD pulse applied on NC ball, most energy will be dissipated in a short duration of time. Such ESD current will be crowded in some limited areas of the ESD diodes which have the minimum resistance. As shown in Fig. 4, contact destructions on the ESD diodes are located on the boundaries between the diffusion and STI regions, especially around the corners. These ESD diodes can sustain above 3-kV HBM and above 300-V MM direct ESD pulses, but fails by the NC ball induced event during 2-kV HBM ESD stress. Because the discharge durations of HBM and MM ESD events are much longer than that of such NC ball induced event, the ESD diodes in conjunction with the VDD-to-VSS ESD clamp circuit can conduct the ESD current efficiently. However, when the ESD pulse is applied on the NC ball, the ESD current discharging through the ESD diodes of signal ball has a CDM-like short period. The VDD-to-VSS ESD clamp circuit cannot be turned on in time to share the ESD current away from the diodes. Therefore, the ESD pulse applied on the NC ball causes CDM-like failures on the ESD diodes or the output driving MOS of the neighboring signal ball.

To make the ESD diodes more efficient to discharge the high-peak and fast-transient current pulse, the layouts of ESD diodes are suggested in the finger style to obtain a larger perimeter with a lower turn-on resistance.

IV. Conclusion

According to the ESD test standards, the NC balls are not necessarily stressed, but we still treat these NC balls as signal balls under ESD tests for more strict reliability assurance. An abnormal ESD failure mechanism due to HBM ESD pulse applied on the NC balls of a high-pin-count BGA packaged IC has been presented. The failure modes of this mechanism are junction destructions and gate-oxide ruptures on the ESD diodes or output driving MOS of the signal balls around the neighbor of the NC balls. With the new proposed model, from the measurements of ESD current waveforms and the failure points found by SEM, a high correlation has been found between the NC ball induced ESD damages and the SCM method. This gives a reasonable interpretation for this abnormal failure mechanism. According to the failure analyses, two solutions have been provided to prevent such abnormal failures. One of the solutions has been practically used in the BGA packaged IC product to successfully improve the ESD immunity above 3-kV HBM and 300-V MM.

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