

Design, Optimization, and Performance Analysis of New Photodiode Structures for CMOS Active-Pixel-Sensor (APS) Imager Applications

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Abstract—The dark current in the active-pixel-sensor (APS) cell of a CMOS imager is known to be mainly generated in the regions of bird's beak after the local oxidation of silicon process as well as the surface damage caused by the implantation of high doping concentration. Furthermore, shallow and deep pn-junctions can improve the photo-sensitivity for light of short and long wavelengths, respectively. In this paper, two new photodiode structures using p-substrate and lightly-doped sensor implant SN- as pn-junction photodiode with the regions of bird's beak embraced by SN- and p-field implants, respectively, are proposed and analyzed to reduce dark current and enhance the overall spectral response. $5\ \mu\text{m} \times 5\ \mu\text{m}$ APS cells fabricated in a $0.35\text{-}\mu\text{m}$ single-poly-triple-metal (1P3M) 3.3-V CMOS process are designed by using the proposed photodiode structures. As shown from the experimental results, the two proposed photodiode structures of $5\ \mu\text{m} \times 5\ \mu\text{m}$ APS cells have lower dark currents of 30.6 mV/s and 35.2 mV/s at the reverse-biased voltage of 2 V and higher spectral response, as compared to the conventional structure and other photodiode structures. Thus, the two proposed new photodiode structures can be applied to CMOS imager systems with small pixel size, high resolution, and high quality.

Index Terms—Active-pixel-sensor (APS), CMOS imager, dark current, pn-junction photodiode, spectral response.

I. INTRODUCTION

NOWADAYS, CMOS imagers which integrate photo-sensors, optics, analog readout circuits [1]–[3], and intelligent signal processing circuits [4], [5] on a single chip are widely used in many applications. Furthermore, CMOS imagers have been extensively used in portable products due to its low voltage [6], [7], low power consumptions [8], and low cost [1], as compared with the CCD technology. With the rapid scaling down of CMOS technology, the design of multi-million-pixel high-resolution CMOS imagers [9], [10] has become more and more challenging. Generally, small pixel size, low dark current, high fill factor, and high spectral response are required in the high-resolution CMOS imagers.

To achieve these performance requirements, one of the key elements is the photodiode array in which the photodiodes should be designed and optimized carefully. The two critical parameters in the design of photodiodes for imager applications are the dark

current and the spectral response. Large dark current in the photodiode array of CMOS imagers can lead to nonuniformity, low scalability, and reduced dynamic range. The first source of dark current depends on doping concentrations, bandgap, and temperature of the reverse-biased photodiode [11]. The second source is the defect-generated dark current determined by the shape of photodiode layout, the cross-sectional structure of the photodiode, and the fill factor [11]. The shape of photodiode layout can be designed to reduce the dark current [11]. Generally, the second source of dark current is mainly generated from the pn-junction depletion region under bird's beak in local oxidation of silicon (LOCOS) process [12] or in the interface isolation of shallow trench isolation (STI), as well as the surface damage caused by the implantation of high doping concentration.

Some process modifications in CMOS technology are required [13] to reduce the dark current of the photodiode while maintaining other performance of parameters unchanged. Recently, several new photodiode structures have been proposed to reduce the dark current, such as the pinned photodiode [14], the nonsilicide source/drain pixel [15], and the hole-accumulated diode structure [16]. The pinned photodiodes have small dark current, but the complex process may reduce yield and increase cost. The nonsilicide source/drain pixel can reduce the dark current under the penalty of speed reduction due to the large source/drain resistance. Due to the same principle of the pinned photodiode and the distance of the sensor junction from the isolation region (LOCOS or STI region), the hole-accumulated diode structure has low dark current. However, it requires the same complex process as the pinned photodiode.

The spectral response is another important parameter considered in the design of photodiodes. The high spectral response of photodiodes can be generated by using shallow and deep depth of the pn-junctions to absorb photons for light of short and long wavelengths, respectively. Among the proposed photodiode structures [14], [17], [18] for CMOS imager applications, the mixed P/N+ and P/N-well junctions [17] can absorb photons for light of short and long wavelengths by using P/N+ and P/N-well junctions, respectively. However, the structure is not scalable due to the large N-well width and space. The pinned photodiode [14] includes two junctions optimized independently of CMOS devices to improve the spectral response. However, the complex process steps remain disadvantageous. The spectral response and quantum efficiency of the hollow photodiode [18] are improved because of its extended depletion region. Controlling the uniformity of the hollow photodiode array is difficult due to the hollow shape of the photodiode.

Manuscript received November 1, 2002; revised July 2, 2003. This work was supported in part by PixelArt Imaging, Inc., and in part by UMC, Ltd. The associate editor coordinating the review of this paper and approving it for publication was Dr. Ralph Etienne-Cummings.

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Digital Object Identifier 10.1109/JSEN.2003.820361

TABLE I
ALL LAYERS AND THEIR FUNCTIONS IN THE DESIGN OF CMOS APS IMAGER

Layer	Function
SN+	Sensor implant with high doping density
SN-	Sensor implant with low doping density
N+	Definition of N+ source/drain implantation
NB	Regions of N+ is defined outside the mask of NB
P+	Definition of P+ source/drain implantation
p-field	Regions of p-field implant
pfb	Regions of p-field is defined outside the mask of pfb
thin oxide	Definition of thin oxide for devices
FOX	Regions of field oxide
p-substrate	Regions of p-substrate
SAB	Definition of salicide protection
metall(2)(3)	Definition of metall(2)(3) for interconnections
via1	Definition of via1 hole between metal1 and metal2
via2	Definition of via2 hole between metal2 and metal3
contact	Definition of contact window for metal1 to thin oxide and to poly
N-well	Definition of N-well
poly	Definition of poly-silicon

It is the aim of this paper to propose two new photodiode structures with low dark current and high spectral response. The pn-junction of p-substrate and the lightly-doped sensor implant SN- is used as a photodiode in both structures. The regions of bird's beak in the two proposed structures are completely embraced by the SN- implant and the p-field implant, thus, not located in the pn-junction depletion region. Both pn-junction depletion located under the bird's beak and surface damage due to high doping concentration can be avoided and the generation of dark current can be suppressed. Furthermore, the use of shallow and deep pn-junctions can increase the photo-sensitivity for light of short and long wavelengths, respectively. Thus, the spectral response can be improved. Systematic comparisons on measurement results of dark currents and spectral responses among the proposed photodiode structures and other structures in CMOS technology with reasonable process modifications are presented. From the experimental results, it has been verified that the two proposed structures in the $5\ \mu\text{m} \times 5\ \mu\text{m}$ APS cell of the CMOS imager have low dark currents of 30.6 mV/s and 35.2 mV/s at the reverse-biased voltage of 2 V, as well as good spectral response.

The rest of this paper is organized as follows. In Section II, two new CMOS photodiode structures in 0.35- μm 1P3M 3.3-V CMOS technology with salicide process are described. Principles of reducing the dark current and improving the spectral response are also presented. Other photodiode structures for comparison purpose are also described. In Section III, the layout consideration and optimization for the proposed photodiode structures and

other structures for comparisons are described. In Section IV, experimental results of dark current and spectral responses of the fabricated photodiodes are presented, analyzed, and compared to verify the advantageous performance of the proposed new photodiode structures. Conclusions and areas for future researches are finally made in Section V.

II. ANALYSIS OF NEW CMOS PHOTODIODE STRUCTURES

Generally, it is difficult to accurately characterize and predict both dark current and spectral response of a pn-junction photodiode by using model equations. In this work, based on the analysis on the mechanisms for dark currents and spectral responses as well as the understanding of process technology, we proposed and designed two photodiode structures for low dark current and/or high spectral response. Several other structures were also designed. Through extensive experimental measurements on dark currents and spectral responses of all fabricated photodiode structure, the mechanism can be verified and the optimal structure can be confirmed.

The cross-sectional views of the two proposed photodiode structures called Type P1 and Type P2 with the explanations of all dimension notations are shown in Fig. 1(a) and (b), respectively. The modified 0.35- μm single-poly-triple-metal (1P3M) CMOS process with a lightly-doped p-substrate and LOCOS structure is adopted to realize the two new structures. All the layers and their functions in the design of CMOS imager are summarized in Table I. The p-well is defined by a mask that

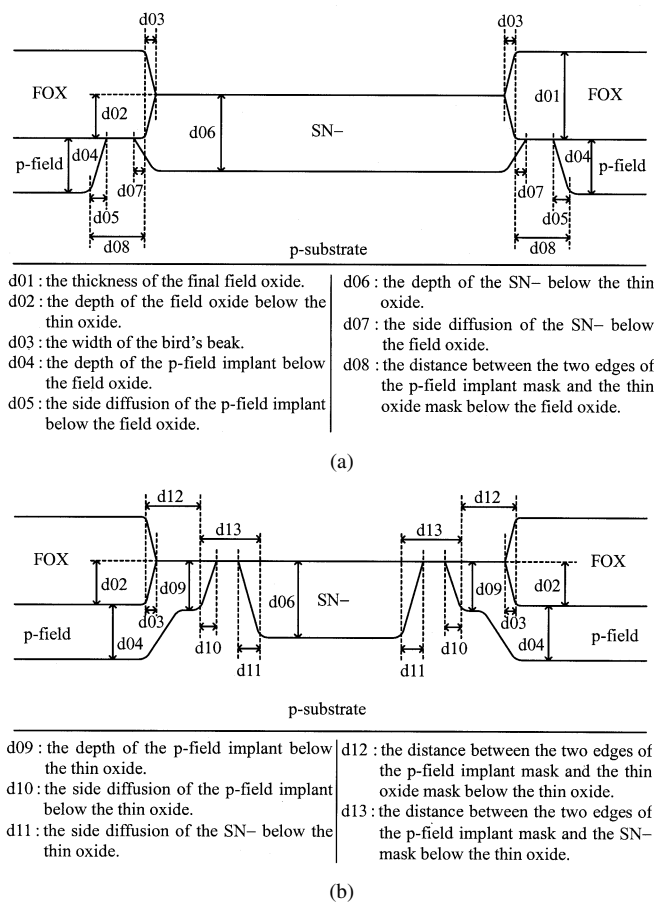


Fig. 1. Two proposed new photodiode structures. (a) Type P1: photodiode is composed of p-substrate and SN- with its bird's beak embraced by SN-. (b) Type P2: photodiode is composed of p-substrate and SN- with its bird's beak embraced by p-field.

differs from the complement of the n-well mask in this modified CMOS process. The p-field implant is defined by another mask and is completed before the use of the mask defined by the thin oxide. Following the growth of SiO₂ and SiN on the region defined by the thin oxide, the thick field oxide (FOX) is grown in areas where SiN is absent. Field oxide is grown in both vertical and lateral directions. The growth in the lateral direction results in the bird's beak. This technique of field oxide growth is so called LOCOS (local oxidation of silicon). The planarization technique used to etch the field oxide to its final thickness is then completed. The regions of the p-field implant below the field oxide are pushed downward during the growth of the field oxide. The cross-sectional views of the bird's beak, FOX, and the p-field implant are shown in Fig. 1(a) and (b).

In the photodiode structures, all significant dimensions are mentioned in notations. These dimensions depend on different CMOS fabrication technologies, fabrication equipments, and different fabs. The real values for these dimensions should be carefully optimized for a certain technology or fabrication fab.

In the structure of the Type P1 photodiode, all regions of the thin oxide are implanted by the lightly-doped sensor implant SN-, as shown in Fig. 1(a). Thus, the pn-junction of p-substrate and SN- is used as the photodiode. The length of d06 is longer than that of d02, so regions of the bird's beak are completely embraced by SN-.

Since the bird's-beak region has a high density of defects due to the high silicon/SiO₂ stress, the dark current will be increased significantly if the depletion region of the pn-junction photodiode is located in the bird's-beak region. In the Type P1 structure, the regions of bird's beak are not located in the depletion region of the pn-junction photodiode formed by the p-field implant and SN- if the following equation is adopted:

$$d08 > d05 + d07 + \Delta d05 + \Delta d07 \quad (1)$$

where $\Delta d05$ and $\Delta d07$ represent the mask misalignments of the p-field implant and SN-, respectively. Thus, the dark current that results from the bird's beak can be completely avoided in the Type P1 structure. Under these conditions, the depletion region of a photodiode is not located in the bird's-beak region. Too large d08 will decrease the fill factor. If d08 is equal to or smaller than the sum of d05 and d07, then the depletion region of the p-field/SN- junction will be in the bird's-beak region to increase the dark current.

The dark current of the photodiode is also increased due to the surface damage generated by the sensor implant. The higher doping concentration of the sensor implant will result in greater surface damage causing larger dark current. The surface damage in the Type P1 structure is low due to the low doping concentration of SN-. This further decreases the dark current in P1.

In the Type P1 structure, p-well is replaced by p-substrate in the formation of the pn-junction. Thus, the depletion region of the photodiode becomes wider to absorb more photons due to the lower doping concentration of p-substrate than that of p-well. In the Type P1 structure, the depletion region of the p-substrate/SN- junction photodiode at the bottom plate is deep enough to absorb long wavelength photons. Thus, the photosensitivity for the light of long wavelength can be improved. The depletion region of p-substrate and the side diffusion of SN- below FOX is effective in the absorption of short wavelength photons because this part of pn-junction is shallow enough to absorb photons for the light of short wavelength. Absorption of photons is not affected by FOX because FOX is transparent.

In the Type P2 structure, the pn-junction of p-substrate and SN- is used as a photodiode where SN- has the same doping concentration as in the Type P1 structure. In the Type P2, only the central part of thin-oxide region is implanted by SN- as shown in Fig. 1(b). The mask of SN- is defined inside the regions of thin oxide. The length of d09 is slightly larger than that of d04 because the regions of p-field implant below the thin oxide are not pushed out by the field oxide during its growth. The length of d09 is larger than that of d02. In the Type P2, the regions of bird's beak are completely embraced by the p-field implant.

The regions of bird's beak in the Type P2 structure are not located in the depletion region of pn-junction photodiode formed by the p-field implant and SN- if the following two equations are adopted:

$$d03 < d10 + d12 + \Delta d10 \quad (2)$$

$$d13 > d10 + d11 + \Delta d10 + \Delta d11 \quad (3)$$

where $\Delta d10$ and $\Delta d11$ represent the mask misalignments of the p-field implant and SN-, respectively. If the sum of d10 and d12 is designed to be much larger than the length of d03, then

the length of d_{13} can be designed to be shorter than the sum of d_{10} and d_{11} . In this case, the p-field implant and SN- will be in contact together but the regions of bird's beak will not be located in the depletion region of p-field/SN- junction because the doping concentration of p-field implant is higher than that of SN-. However, the fill factor is small in this case. If the sum of d_{10} and d_{12} is designed to be shorter than the length of d_{03} , then the length of d_{13} must be designed to be much longer than the sum of d_{10} and d_{11} to prevent the regions of bird's beak from being located in the depletion region of p-substrate/SN- junction. The fill factor is also small in this case.

The sum of d_{10} and d_{12} is designed to be slightly longer than the length of d_{03} and the length of d_{13} is designed to be slightly longer than the sum of d_{10} and d_{11} to protect the regions of bird's beak from being located in the depletion region of pn-junction and keep the fill factor as large as possible. The regions of bird's beak in this optimal design are completely embraced by the p-field implant and are not located in the depletion region of p-substrate/SN- junction. Thus, dark current from the bird's beak can be completely avoided in P2. The surface damage is also kept low in P2 due to the low doping concentration of both p-field implant and SN-.

In the performance of photo-sensitivity, the depletion region of the p-substrate/SN- junction at the bottom plate is deep enough and is, therefore, used to absorb photons for the light of long wavelength. Moreover, the depletion region of the pn-junction formed by the p-substrate and the side diffusion of SN- is used to absorb photons for the light of short wavelength.

Four structures, C1, C2, C3, and C4, with the explanations of all dimension notations shown in Fig. 2(a), (b), (c), and (d), respectively, are analyzed to compare their performance with that of the two proposed new photodiode structures. In Fig. 2(a), the p-substrate and N+ implant are used as the pn-junction photodiode. This structure is the same as Type P1 except that SN- is replaced by N+. Type C1 is the conventional photodiode structure used in the standard CMOS process. However, the bird's beak cannot be embraced completely by N+ because the length of d_{14} is shorter than that of d_{02} . Thus, some bird's-beak regions are located in the depletion region of the p-substrate/N+ junction. In the performance of photo-sensitivity, the shallow p-substrate/N+ junction at the bottom plate can be used to absorb photons for light of short wavelength.

In Fig. 2(b), the p-substrate and the SN+ implant are used as the pn-junction photodiode. SN+ is an extra sensor implant used in the modified CMOS process. The photodiode structure of Type C2 is the same as that of Type P1 except SN- is replaced by SN+. The length of d_{16} is shorter than that of d_{02} , so SN+ still cannot be used to embrace completely the regions of bird's beak. Thus, some bird's-beak regions are located in the depletion region of the p-substrate/SN+ junction. In the performance of photo-sensitivity, the shallow p-substrate/SN+ junction at the bottom plate can be used to absorb photons for light of short wavelength.

In Fig. 2(c), the p-substrate and SN+ are used as the pn-junction photodiode. The photodiode structure of Type C3 is the same as that of Type P2 except that SN- is replaced by SN+. The bird's beak will be located in the depletion region of the p-field/SN+ junction if the length of d_{19} is equal to that of

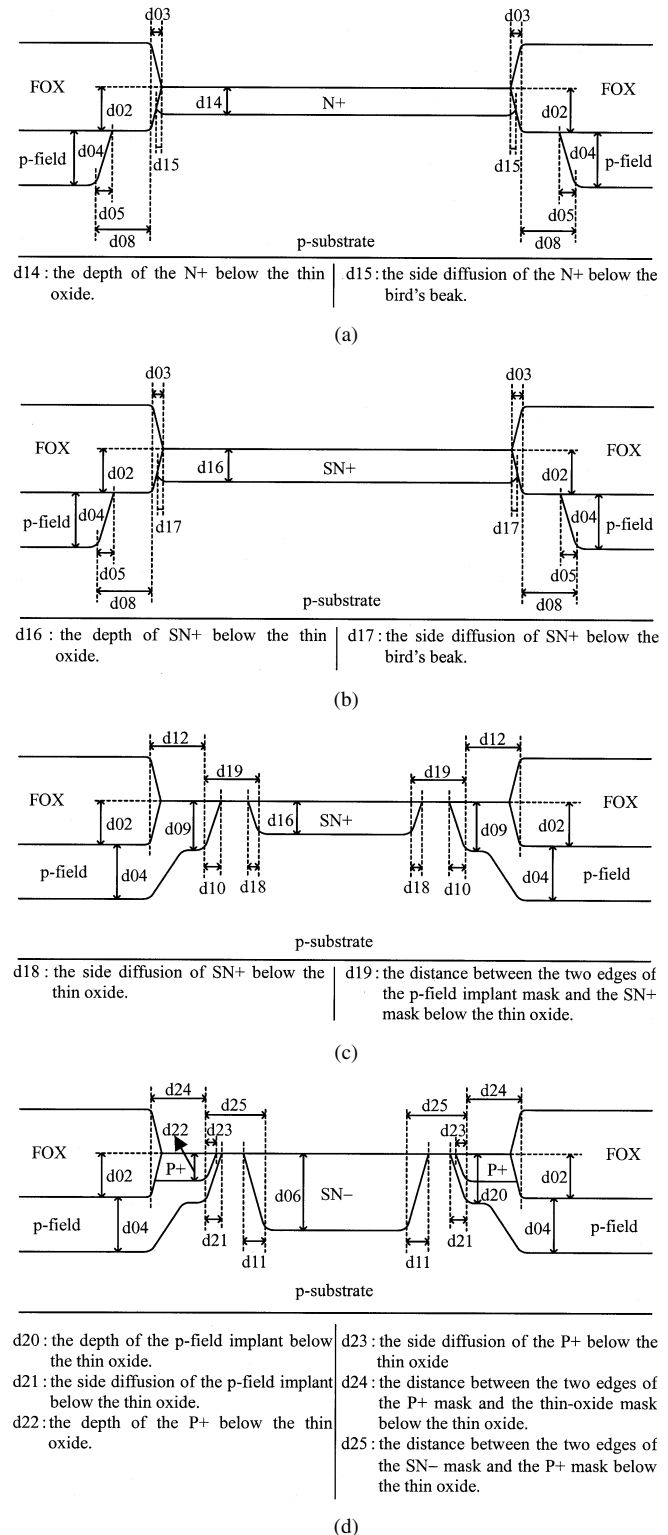


Fig. 2. Four photodiode structures for comparisons. (a) Type C1: SN- is replaced by N+ in the structure of P1 (conventional structure in CMOS imager). (b) Type C2: SN- is replaced by SN+ in the structure of P1. (c) Type C3: SN- is replaced by SN+ in the structure of P2. (d) Type C4: P+ is added to embrace the bird's beak in the structure of P2.

d_{13} in Fig. 1(b) because the doping concentration of SN+ is larger than that of the p-field implant. The depletion region of the pn-junction photodiode formed by the p-substrate and the side diffusion of SN+ can be used to absorb photons for light of

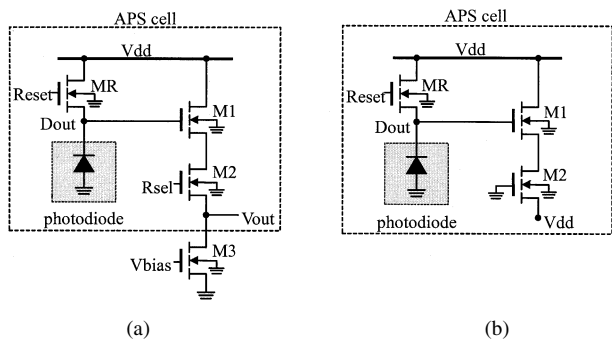


Fig. 3. (a) Circuit diagram of APS cell. (b) Circuit diagram of APS cell with its R_{set} and V_{out} connected to gnd and V_{dd} , respectively.

short wavelength. Moreover, the shallow p-substrate/SN+ junction at the bottom plate can also be used to absorb photons for light of short wavelength.

In Fig. 2(d), the p-substrate and SN- are used as the pn-junction photodiode. The photodiode structure of Type C4 is the same as that of Type P2 except that both P+ and p-field implant are used to embrace the bird's beak. The distance between the two edges of the P+ mask and the p-field mask is equal to zero. The regions of bird's beak are completely embraced by both of P+ and p-field implant if the lengths of d_{24} and d_{25} are equal to that of d_{12} and d_{13} , respectively. The photo-sensitivity of Type C4 is the same as that of Type P2.

III. LAYOUT OPTIMIZATION OF NEW PHOTODIODE STRUCTURES IN APS CELLS

The circuit diagram of APS cell is shown in Fig. 3(a), where the NMOSFET of MR is used to reset the voltage of the photodiode. The two NMOSFET's of M1 and M2 are used as source follower and row selector, respectively. The layouts of the two proposed new photodiode structures applied to the $5 \mu m \times 5 \mu m$ active-pixel-sensor (APS) cell are shown in Fig. 4(a) and (b), respectively. To show the layout of APS cell clearly, only masks of the thin oxide, poly, metal1, p-field block (pfb), N+ block (NB), SN-, P+, and contact are drawn in Fig. 4(a) and (b). Routing and interconnections of the APS cell are not shown in the layout diagrams. The placement of the three NMOSFETs is also shown in Fig. 4(a) and (b). The region of the p-field implant is defined outside the mask of pfb. The region of N+ is defined outside the mask of NB.

Even a single contact will drastically decrease the fill factor due to the small area of $5 \mu m \times 5 \mu m$ APS cell. In the layout of Fig. 4(a), the source region of MR is directly connected to the photodiode to save one contact and increase the fill factor. The p-substrate contact has been moved outside the $5 \mu m \times 5 \mu m$ APS cell. The contact at the gate of MR cannot be removed, otherwise the reset operation will be delayed and the dark current in the photodiode will be increased. Only six contacts are used in the layout of the $5 \mu m \times 5 \mu m$ APS cell and the maximum fill factor can be large.

In Fig. 4(a), the photodiode structure of Type P1 is used in the $5 \mu m \times 5 \mu m$ APS cell. SN- is used to embrace the bird's beak completely except for the two edges of A and B because the source region of MR should be implanted by N+. Although N+

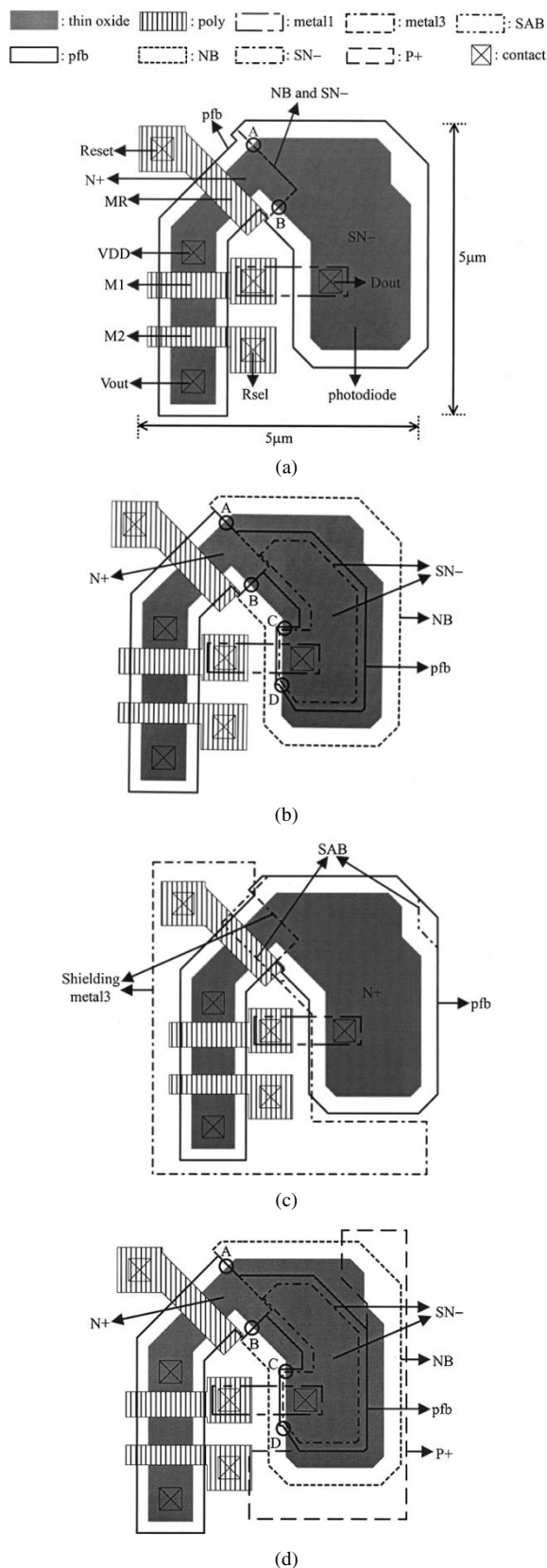


Fig. 4. Layout of photodiode in $5 \mu m \times 5 \mu m$ APS cell. (a) Type P1: fill factor = 32%. (b) Type P2: fill factor = 15%. (c) Type C1: fill factor = 32%. (d) Type C4: fill factor = 15%.

is used to embrace the regions of bird's beak at the two edges, some bird's-beak regions are still located in the depletion region

of the p-substrate/N+ junction because the depth of N+ is shallower than that of FOX below the thin oxide. This will increase the dark current. The distance between pfb and the edge of the thin oxide is designed according the design principle mentioned in the previous section. The fill factor in this structure is large because all regions of the thin oxide in the Type P1 are implanted by SN-. The fill factor is designed to be 32% in the layout of Fig. 4(a).

The regions of the photodiode should be covered by the SAB (silicide block) mask to remove the silicide from the top of photodiode due to its optically opaque and undesirably large leakage [1], [15], [19]. However, the large leakage current is induced in the interface of the silicided source region of MR and the nonsilicided region of the photodiode. This situation is prevented by covering the total source regions of the NMOSFET MR by SAB as shown in Fig. 4(c) to reduce the effect of the silicided interface. Regions other than the photodiode should be shielded by metal from light irradiating. Regions covered by metal3 are also shown in Fig. 4(c). The shielding by metal3 and the block of silicide in the detailed layout of the APS cell are shown in Fig. 4(a) and (b).

In Fig. 4(b), the photodiode structure of Type P2 is used in the $5 \mu\text{m} \times 5 \mu\text{m}$ APS cell. The regions of bird's beak are all embraced by the p-field implant except for the four edges A, B, C, and D. The bird's beaks at the two edges of both A and B are embraced by N+ with the p-field implant extended under N+ because the source region of MR must be implanted by N+. Thus, some bird's-beak regions at the two edges of A and B will be located in the depletion region of the p-field/N+ junction. The regions of bird's beak will be located in the depletion region of the p-field/SN- junction at the two edges of C and D because the contact in the photodiode should be embraced by SN- and both regions of the p-field implant and SN- are extended outside the thin-oxide edge. Although the contact in the photodiode can be put in the right side of the current position, this will reduce the fill factor due to the shielding effect of metal. The distance between the two edges of the pfb mask and the thin-oxide mask as well as the distance between the two edges of the pfb mask and the SN- mask are designed according to the optimal value as determined in Fig. 1(b). The fill factor is designed to be 15% in the layout of Fig. 4(b).

The layouts of photodiode structures in both Type C1 and Type C4 for comparisons in $5 \mu\text{m} \times 5 \mu\text{m}$ APS cell are shown in Fig. 4(c) and (d), respectively. In Fig. 4(c), the conventional photodiode structure of Type C1 uses N+ to embrace the bird's beak. The mask of the p-field implant is the same as that of the layout in Fig. 4(a). Some regions of the bird's beak will be located in the depletion region of the p-substrate/N+ junction as referred to Fig. 2(a). The fill factor in this layout is the same as that of Type P1. The layouts of Type C2 and Type C3 are the same as those of Type P1 and Type P2, respectively, except that SN- is replaced by SN+. In Fig. 4(d), the layout of Type C4 is the same as that of Type P2 except that P+ implant is added to embrace the bird's beak. P+ cannot be used to embrace all bird's-beak regions in Fig. 4(d) because pn-junction breakdown will be caused if the distance between P+ and N+ is too short. The bird's beak at the four edges of A, B, C, and D are still located in the depletion region of the pn-junction as referred to

Fig. 4(b). The fill factor in this layout is the same as that of Type P2.

IV. EXPERIMENTAL RESULTS

In the conventional measurement method of dark currents [11], the dark current in each pixel is integrated at the node of APS cell for a certain period of time and determined from the integrated voltage. The variations of dark currents among pixels of the entire imager array can be observed in this method. In this work, the experimental dark-current characteristics of different photodiode structures versus reverse-biased voltages are required for comparisons. The main focus is not on the variation of dark current in each pixel. Thus, the measurement method with large number of photodiodes in parallel is used.

The interconnection in the APS cell is changed to that shown in Fig. 3(b) to measure directly the dark current of the photodiode. R_{sel} and V_{out} are connected to ground and V_{dd} , respectively. Thus, no current flows in the NMOSFETs of M1 and M2. If Reset is set to ground to turn off MR, then the relationship of current to voltage (I - V) at D_{out} under the reverse bias of the dark photodiode represents the characteristics of the dark current of the photodiode. However, the current in a single APS cell is too small to be measured. Thus, an APS cell array with all the Reset (D_{out}) nodes connected together is used to increase the current. There are 25 600 APS cells for each new photodiode structure. The I - V characteristics of each new photodiode structure can be obtained by dividing the measured total current by 25 600. The dark current measurements were taken at room temperature (300 K), which is kept constant.

The dark current of an APS cell can be represented in the form of $(dV(t)/dt)$ at D_{out} of Fig. 3(b). The effective dark current of $(dV(t)/dt)|_{V=V_0}(= (I(V_0)/C(V_0)))$ can be obtained by measuring $I(V_0)$ and $C(V_0)$ at the fixed bias V_0 where $I(V_0)$ and $C(V_0)$ represent the current and capacitance at D_{out} under the reverse-biased voltage of V_0 and no light irradiating. Note that $I(V_0)$ and $C(V_0)$ of an APS cell can be obtained from the corresponding measured data of the parallel APS cell array by dividing those data by 25 600. All the measured data are obtained from the statistical average of different measured chips.

The method for measuring the spectral response of photodiodes is the same as the proposed method except that the regions of the photodiode should be irradiated by monotonic light with the wavelength between 400 nm and 700 nm.

A. Dark Current

The chip photograph of the fabricated parallel-connected APS cells with one new photodiode structure is shown in Fig. 5. The capacitance of the dummy PAD must be measured and subtracted from the measurement results of $C(V)$ to derive the capacitance at D_{out} in Fig. 3(b).

The measured $I(V)$ and $C(V)$ at D_{out} for the Type P1 photodiode structure are shown in Fig. 6(a) and (b), respectively, when the Reset is set to 0 volts as shown in Fig. 3(b). The effective dark current (dV/dt) , of an APS cell with the photodiode structure of Type P1 can be derived from the results in Fig. 6(a) and (b). The dark current of an APS cell for other photodiode structures can also be derived from the $I(V)$ and $C(V)$.

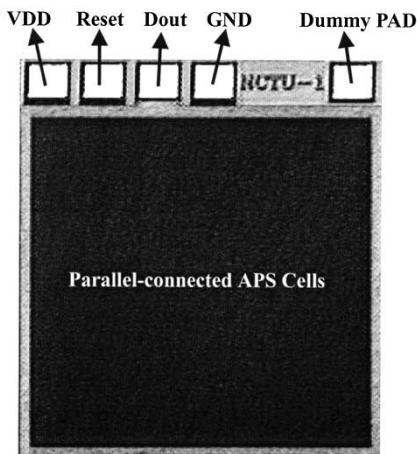
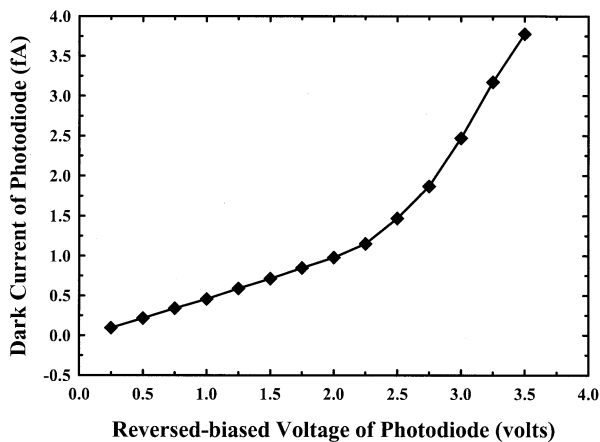
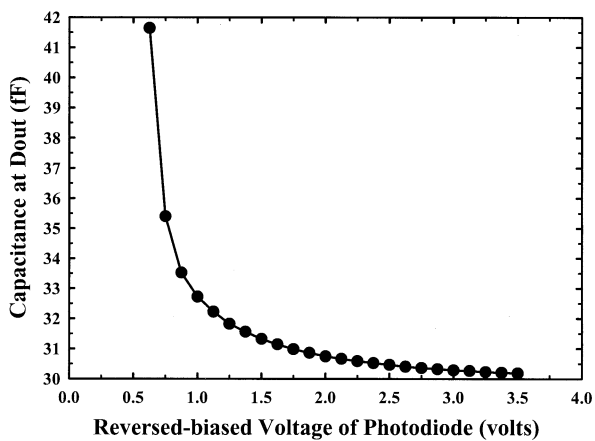


Fig. 5. Photograph of one photodiode structure in test chip.



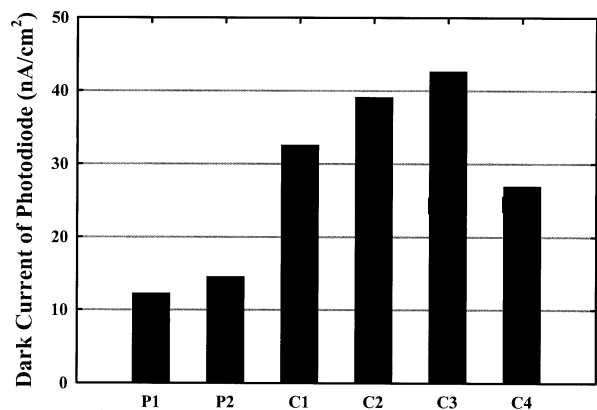
(a)



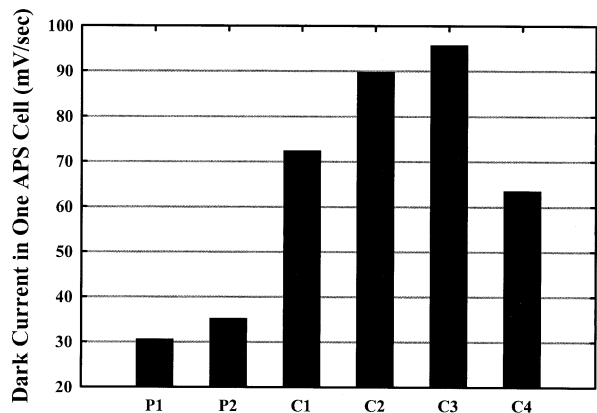
(b)

Fig. 6. Dark current characteristics of photodiode in an APS cell with the photodiode of Type P1. (a) Current to voltage curve: $I(V)$. (b) Capacitance to voltage curve: $C(V)$.

The measured dark current in $5\ \mu\text{m} \times 5\ \mu\text{m}$ APS cells with the two proposed new photodiode structures and four other structures for comparisons are shown in Fig. 7(a) and (b). The reverse-biased voltage of the photodiode under the measurement is equal to 2 V, i.e. $V_0 = 2\ \text{V}$. The dark current of one photodiode per unit area is shown in Fig. 7(a), whereas the effective dark current of one APS cell is shown in Fig. 7(b). The



(a)



(b)

Fig. 7. Measurement results of dark current at the reverse-biased voltage of 2 V. (a) One photodiode. (b) One APS cell for imager applications.

dark currents of Type P1 and Type P2 photodiode structures are $12.25\ \text{nA/cm}^2$ and $14.55\ \text{nA/cm}^2$, respectively. The dark currents of one APS cell with Type P1 and Type P2 photodiode structures are $30.6\ \text{mV/s}$ and $35.2\ \text{mV/s}$, respectively. The proposed photodiode structure of Type P1 has the smallest dark current because all of the bird's-beak regions are embraced by SN- and the surface damage is low by using the low doping concentration of SN-. Furthermore, the first source of dark current in the photodiode structure of Type P1 is the lowest by using SN- and p-substrate as photodiode. The surface damage in the regions of the p-field implant below the thin oxide is slightly greater than that in SN- because the p-field implant has a higher doping concentration than that of SN-. Thus, the dark current in the Type P2 structure is slightly larger than that in the Type P1 for photodiodes with the same area because the surface damage in the Type P2 is slightly greater than that of Type P1. Furthermore, the regions of bird's beak at the two edges of C and D in the layout of Type P2 are located in the depletion region of the p-field/SN- junction as shown in Fig. 4(b). This slightly increases the dark current in the Type P2. The measurement results of dark-current variations of the fabricated Type P1 and Type P2 photodiodes at the reverse-biased voltage of 2 V for seven different chips have been measured and shown in Fig. 8. The variations among different chips are small as shown in Fig. 8. Thus, the effect of mask misalignment in the two proposed photodiode structures is not significant. Moreover, the dark current of Type

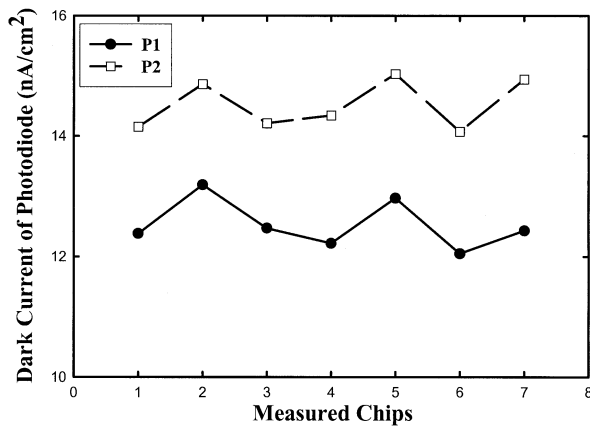


Fig. 8. Measurement results of dark current variations of Type P1 and P2 at the reverse-biased voltage of 2 V among seven different chips.

P1 is smaller than Type P2, even with variations. Thus, the statistically averaged dark current obtained from the measured data on different chips can represent the true result as shown in Fig. 7.

The surface damage in the Type C4 is greater than that in the Type P2 because of the addition of P+ to embrace the bird's beak. Thus, the dark current in the Type C4 is larger than that in the Type P2. Some bird's-beak regions in the Type C1 photodiode structure are located in the depletion region of the p-substrate/N+ junction because N+ cannot be used to embrace the entire regions of bird's beak as referred to Fig. 2(a). Furthermore, the surface damage in the Type C1 is serious because of the high doping concentration of N+. Thus, the dark current in the Type C1 structure is larger than that in the Type C4.

The surface damage in the Type C2 is less than that in the Type C1 because SN+ has a lower doping concentration than N+. However, the dark current in the Type C2 is larger than that in the Type C1 because more bird's-beak regions are located in the depletion region of the pn-junction in the Type C2 structure than in the Type C1 structure. Type C3 has the largest dark current because most regions of the bird's beak are located in the depletion region of the p-field/SN+ junction since SN+ has higher doping concentration than the p-field implant. The effect of surface damage in the Type C3 is also serious due to the use of the high doping concentration of SN+. The measurement results of the dark current, the fill factor, and pixel capacity in the two proposed new photodiode structures and the four structures for comparisons are given in Table II.

B. Spectral Response

The spectral responses of Type P1, Type P2, Type C1, Type C2, and Type C3 are shown in Fig. 9. The spectral response in the Type C4 structure is the same as that in the Type P2. In the photo-sensitivity for light of long wavelength as shown in Fig. 9, the Type P1 has the best performance because all regions of the photodiode are composed of the deep p-substrate/SN- junction. The performance of Type P2 is worse than that of Type P1 because regions of deep pn-junction in the Type P2 are smaller than those in the Type P1. Although the p-substrate/SN+ junction in the Type C2 can be used to absorb photons for light of

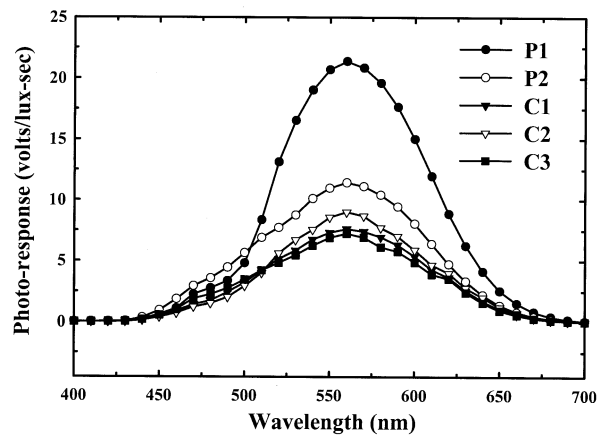


Fig. 9. Spectral responses in the photodiode structures of Type P1, Type P2, Type C1, Type C2, and Type C3.

long wavelength, its efficiency is not as good as that of SN- because the junction depth of SN+ is shallower than that of SN-. Thus, the performance in the Type C2 is worse than that in the Type P2. The performance in the Type C1 is worse than that in the Type C2 because the junction depth of N+ is shallower than that of SN+. The performance in the Type C3 is slightly worse than that in the Type C1 because more N+ regions in the Type C1 can be used to absorb photons for light of long wavelength than the regions of SN+ in the Type C3 even although the junction depth of N+ is shallower than that of SN+.

In the photo-sensitivity for light of short wavelength, the performance of Type P2 is better than that of Type P1 because the regions of the shallow pn-junction composed of p-substrate and the side diffusion of SN- in the Type P2 are larger than that of Type P1. Type P1 has better performance than Type C1 because longer side diffusion length in SN- than that in N+ can be used to absorb photons for light of short wavelength although the junction depth of N+ is shallower than that of SN-. The performance in the Type C1 and Type C3 is almost the same because the junction depth of N+ is shallower than that of SN+ but the side diffusion length of N+ in the Type C1 is shorter than that of SN+ in the Type C3. The Type C2 structure has the worst performance because the junction depth of SN+ is deeper than that of N+ and the side diffusion length of SN+ in the Type C2 is not long enough.

The measurement of dark current was performed by using the instruments of probe station, HP E3610A dc power supply, HP 4156B precision semiconductor parameter analyzer, and HP 4284A precision LCR meters. The measurement of spectral response was performed by using the instrument of monotonic light generator with its wavelength from 400 nm to 700 nm.

From the above measurement results, the two proposed new photodiode structures applied in the $5\ \mu\text{m} \times 5\ \mu\text{m}$ APS cell show lower dark current and higher overall spectral response than the conventional structure and the other structures for comparisons. With the rapid scaling down of the CMOS process and the future requirements for a high quality imager, the $5\ \mu\text{m} \times 5\ \mu\text{m}$ APS cell of the CMOS imager using the two proposed structures of Type P1 and Type P2 can be applied in the high resolution and high quality imager systems.

TABLE II
FILL FACTOR, DARK CURRENT, AND PIXEL CAPACITY IN $5\ \mu\text{m} \times 5\ \mu\text{m}$ APS CELLS AT REVERSE-BIASED VOLTAGE OF 2 V

Type	Fill Factor	Dark Current (nA/cm ²)	Dark Current (mV/sec)	Dark Current (electrons/sec)	Pixel Capacity (electrons)
P1	32%	12.25	30.6	0.98×10^{-15}	51.25×10^{-15}
P2	15%	14.55	35.2	0.55×10^{-15}	25.01×10^{-15}
C1	32%	32.56	72.4	2.59×10^{-15}	57.46×10^{-15}
C2	32%	39.12	89.8	3.13×10^{-15}	55.78×10^{-15}
C3	15%	42.63	95.8	1.59×10^{-15}	26.72×10^{-15}
C4	15%	26.94	63.5	1.01×10^{-15}	25.46×10^{-15}

Because the CMOS technology used in the experimental results of this paper is 0.35- μm single-poly-triple-metal (1P3M) 3.3-V CMOS process with LOCOS structure, the LOCOS structure is discussed more in this work. Although the dark currents of photodiode structures with STI (shallow trench isolation) are smaller than those with LOCOS, the proposed photodiode structure can also be used to further improve the performance of dark current and spectral response.

V. CONCLUSION

Two new photodiode structures with low dark current and high spectral response are proposed and analyzed in this paper. The p-substrate and the SN- implant are used as the pn-junction photodiode in both new structures. Regions of the bird's beak in the two proposed structures are embraced by either the SN- implant or the p-field implant and are kept away from the depletion region of the pn-junction. The surface damage can be lowered by using the low doping concentration of the SN-implant. Thus, in the two new photodiode structures, the dark current generated in the regions of bird's beak can be lowered and the increase of the dark current due to the effect of surface damage can be avoided. The spectral responses of the two structures can be improved by utilizing the shallow side diffusion and deep bottom diffusion of SN- to absorb the photons for light of short and long wavelengths, respectively.

The layout of the $5\ \mu\text{m} \times 5\ \mu\text{m}$ APS cell designed using the two proposed new photodiode structures are implemented in the 0.35- μm 1P3M 3.3-V CMOS technology. It has been verified by experimental results that the two proposed photodiode structures have lower dark current and higher overall spectral response as compared to other photodiode structures. Because the CMOS technology used in the experimental results of this paper is 0.35- μm single-poly-triple-metal (1P3M) 3.3-V CMOS process with LOCOS structure, the LOCOS structure is discussed more in this work. However, the proposed photodiode structures can also be applied to improve the performance of dark current and spectral response in CMOS technologies with STI. Thus, the two new photodiode structures can be applied to the design of high-performance CMOS imagers with small pixel size, high resolution, low dark current, and high spectral response. Future research will be conducted to design such high-performance CMOS imagers.

ACKNOWLEDGMENT

The authors would like to thank PixelArt Imaging, Inc., and UMC, Ltd., for their valuable discussions and suggestions.

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