High-Voltage and High-Temperature Applications of DTMOS With Reverse Schottky Barrier on Substrate Contacts

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***Abstract*—In this letter, for the first time, application of dynamic threshold voltage MOSFET (DTMOS) with reverse Schottky barrier on substrate contacts (RSBSCs) for high voltage and high temperature is presented. By this RSBSC, DTMOS can be operated at high voltage (>0.7 V), and exhibits excellent performance at high temperature in terms of ideal subthreshold slope, low threshold voltage and high driving current.**

***Index Terms*—Dynamic threshold voltage MOSFET (DTMOS), Schottky substrate junction, temperature effect.**

I. Introduction

DYNAMIC threshold voltage MOSFET (DTMOS) proposed by Assaderaghi *et al.* [1] is attractive for high-speed applications. By shorting the gate to the body, the threshold voltage ($V_{\rm TH}$) operating under DT mode is reduced due to the forward biasing of the substrate, so the current drive can be drastically improved under the on state. Since the device exhibits the same normal-mode $V_{\rm TH}$ under the off state (because $V_{\rm G} = V_{\rm BS} = 0$), low standby power consumption is maintained. Subthreshold slope and short channel effects are also significantly improved due to the dynamics substrate bias [2]. However, the PN diode between substrate and source would turn on as gate/substrate bias larger than 0.7 V for n-channel DTMOS. Considerably large leakage current due to the turn-on diode current between substrate and source terminals is a disaster under dynamic threshhold (DT) mode. Therefore, the power supply voltage for DTMOS applications is restricted to 0.7 V due to the turn-on behavior between the substrate and source junctions. Some reports [3]–[5] proposed a Schottky barrier contact formation on the substrate contact for silicon-on-insulator (SOI) devices. However, the body potential is limited to a value lower than forward Schottky diode voltage drop (~0.4 V). This also limits the DTMOS in high voltage operation. In this paper, DTMOS with $CoSi_2$ reverse Schottky barrier on substrate contact (RSBSC) is present. Using this structure, DTMOS can operate at high voltage and exhibit excellent performance at high temperature.

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II. Device Fabrication

N-channel MOS transistors with channel length down to 0.8 μm were fabricated on 6-in silicon wafers with resistivity of 15–20 $\Omega-$cm using a conventional nMOSFET baseline. Local oxidation of silicon (LOCOS) was used for device isolation. A BF_2 channel implant (at 50 keV, 1×13 cm^{-2}) was used for $V_{\rm TH}$ adjustment of all transistors. Gate dielectric thickness of 2.8 nm was grown in N_2O ambient followed by a 200-nm poly-Si deposition. The width is 100 μm. Shallow source/drain (S/D) extensions were formed by As^+ implant at 10 keV to a dose of 4×10^{14} cm^{-2}. After the formation of TEOS sidewall spacer (200 nm), deep S/D junctions were formed by As^+ implantation at 20 keV to a dose of 5×10^{15} cm^{-2}. Wafers were then annealed by a rapid thermal annealing (RTA) at 1020 °C for 20 s. A 25-nm Co film was sputtered followed by a 5-nm capping layer of TiN. Two-step RTA (first at 550 °C for 30 s and second at 850 °C for 30 s) was used for Co-salicidation. Finally, a 550-nm-thick TEOS by plasma-enhanced chemical vapor deposition (PECVD) was deposited and etched for contact holes. A Ti/TiN/Al-Si-Cu/TiN four-layer metal was deposited and patterned to complete contact metallization. Electrical characterizations were carried out with a HP4156 system, and the measurement temperature was 27, 75, and 100 °C, respectively.

III. Results and Discussion

Fig. 1(a) shows the cross section of DTMOSFETs with RSBSCs (RSBSC) and equivalent circuit [Fig. 1(b)]. From the figure, it can be seen that the gate to substrate connection was through n^+ poly-Si gate, Co-Schottky barrier and to p^- substrate. Since Co-Schottky barrier is reversed biased when $V_{\rm G}$ is larger than 0.7 V, the pn junction of substrate/source (S/S) will not turn on when $V_{\rm G} > 0.7$ V. Fig. 2(a) shows the normal DTMOS without RSBSC. It is clear that as $V_{\rm G} > 0.7$ V, significant leakage happens through the turnon S/S junction. On the other hand, when using RSBSC, voltage will drop on the reverse Schottky barrier. The junction of S/S does not turn on as $V_{\rm G} > 0.7$ V. Fig. 2(b) shows the drain current versus drain voltage for device $L/W = 0.8$ μm/100 μm for normal mode operation (i.e., $Vsub = 0$ V) and DTMOS (i.e., $V_{\rm G} = Vsub$) at room temperature, where $V_{\rm G}$ is from 1 to 3 V, with a 0.5 V step. It is very interesting that the leakage current behavior due to the

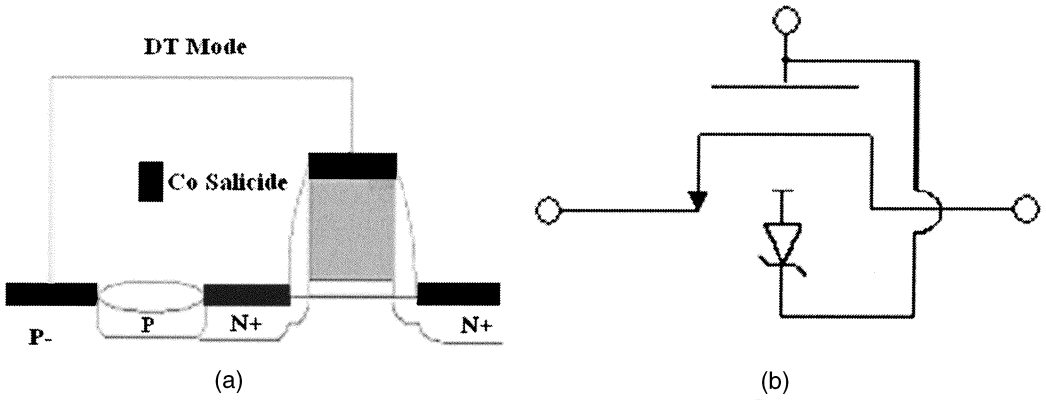

Fig. 1. (a) Connections of MOSFET under the DT mode, and the reverse substrate contact was Schottky substrate contacts (Co salicide-p$^-$ substrate). (b) Equivalent circuits.

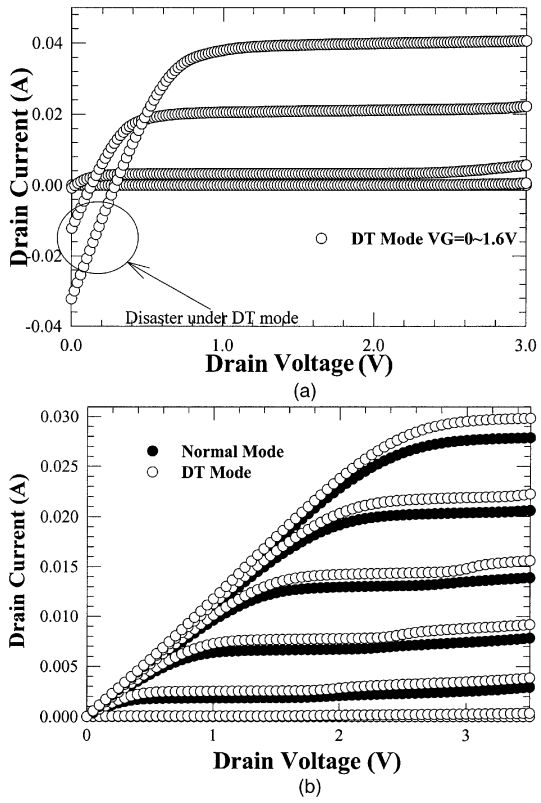

Fig. 2. Drain current versus drain voltage, which gate length was equal to 0.8 μm with width equal to 100 μm. (a)DT-mode without RSBSC. (b) DT-mode with RSBSC and normal modes at room temperature.

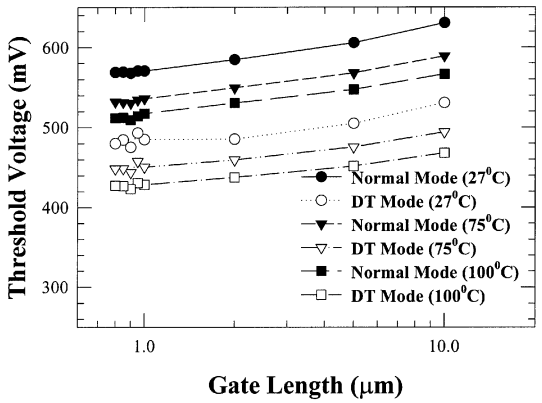

Fig. 3. Threshold voltage versus gate length under both the normal and DT mode for different temperatures. Gate length varies from 10 to 0.8 μm, with a fixed width of 100 μm. The temperature was at 27, 75, and 100 °C.

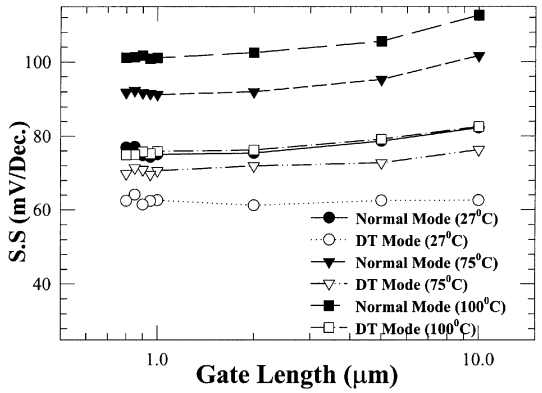

Fig. 4. SS versus gate length under both the normal and DT modes for different temperatures. Gate length varies from 10 to 0.8 μm, with a fixed width of 100 μm. The temperature was at 27, 75, and 100 °C.

turnon S/S diode do not exit for DTMOS with RSBSC scheme. In addition, the saturation current under DT mode at high drain voltage was larger than that under normal mode. Therefore, DTMOS with RSBSC can be operated at $V_{\rm G} > 0.7$ V. Due to the limited forward diode voltage drop, and the threshold voltage would be also decreased about 90 mV. The drain current under DT mode in Fig. 2(b) is larger than that under normal mode due to the reduction threshold voltage. However, the magnitude of improvement was lower than normal DTMOS without RSBSC due to the smaller magnitude of the dynamic threshold voltage reduction. The gate capacitance increases since it is tied to the substrate. To reduce this effect, the Schottky barrier contact can be formed only through the smallest size of contact hole in substrate. The $V_{\rm TH}$ versus gate length under different temperature was shown in Fig. 3. The reduction of $V_{\rm TH}$ under DT mode at 27 °C was about 90 mV (from 570 to 480 mV for 0.8 μm), and the reduction of $V_{\rm TH}$ of DTMOS with RSBSC at higher temperature at 75 and 100 °C shows the same result. The subthreshold behavior at high temperature of DTMOS with RSBSC shows excellent performance, an ideal subthreshold slope (SS) value was found and shown in Fig. 4. The ideal values of SS at 27 °C, 75 °C, and 100 °C deduced from KT/q(ln10) are 60, 68, and 74 mV/dec. respectively. The value of SS under normal mode increases from 78 to 102 mV/dec. as temperature increases from 27 to 100 °C. However,

the SS under DT mode with RSBSC at 27, 75, and 100 °C are 62, 70, and 78 mV/dec., which were almost close to ideal value. The difference of SS between normal and DT modes increases as temperature increases. The reason for excellent SS of DTMOS with RSBSC at elevated temperature is due to the reduced magnitude of $1 + (C_D/C_{OX}) + (C_{it}/C_{OX})$ under DT-mode operation [6].

IV. Conclusion

DTMOS with RSBSC has been presented for high voltage and high temperature operations. Due to the reverse Schottky diode between gate and substrate, the operation voltage can be larger than 0.7 V. Both the saturation current and subthreshold slope could be improved by this scheme. We found that DTMOS with reverse Schottky barrier substrate contacts exhibit excellent performance operating at high temperature in terms of ideal substrate swing and increased driving current. Furthermore, the leakage current as $V_{\rm G} = 0$ V was the same for all devices due to the substrate bias $V_{\rm SUB} = 0$ V for DT devices.

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