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Improved Characteristics of Ultrathin CeO_2 by Using Postnitridation Annealing

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This work demonstrates the improved characteristics of an ultrathin CeO_2 dielectric by using the post-N_2O plasma treatment with additional rapid thermal N_2 annealing. The CeO_2 after the treatment exhibits superior characteristics such as a small effective oxide thickness (~2.25 nm), a low leakage current (5.4×10^{-4} A/cm^2), a high breakdown electric field (−24 MV/cm), a long projected 10 yr lifetime (−12 MV/cm), a small capacitance-voltage hysteresis (25 mV), and a high barrier height for Frenkel-Poole emission (0.55 eV). These good properties are attributed to the nitrogen incorporation into the dielectric to eliminate the traps after annealing. The postnitridation annealing appears to be a very useful treatment for future ultrathin metal-oxide gate dielectrics.
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Recently, many high-dielectric-constant (high-*k*) materials like Al_2O_3, ZrO_2, and HfO_2[1-3] have been widely studied to replace the silicon dioxide due to the inevitability of its high leakage as the thickness scales down. The good candidate gate dielectrics for the next-generation deep submicrometer metal-oxide-semiconductor field-effect-transistor (MOSFET) should be ones with a high dielectric constant, a low interface state density, and a good thermal stability. Cerium dioxide (CeO_2), which has been extensively researched for its use as a buffer layer for $YBa_2Cu_3O_{(7-x)}$ (YBCO) on sapphire,[4] a buried insulator for silicon-on-insulator (SOI)[5] and $PbZrTiCeO_3$ (PZT) ceramics,[6] has lately been used and researched as the gate dielectric material.[7-9] Many superior properties of cerium dioxide, such as a sufficiently high dielectric constant (~26), a lattice constant nearly matched to that of silicon (a = 0.5411 nm), and a high thermal stability on silicon, makes it a promising candidate for this application. However, there are also some undesirable properties of cerium dielectrics, such as high hysteresis,[7-8] making it a material necessary for research for the application. The rapid thermal annealing (RTA) process at various temperatures in various ambients has been generally used to improve the electrical characteristics of high-*k* dielectrics.[10-12] Also, it was widely reported that the plasma nitridation process has been found to improve the characteristics of dielectrics and thin-film transistors.[13-15] In this study, these two processes are investigated to be applied to cerium dielectrics and improved characteristics, especially on the hysteresis, are observed. This makes CeO_2 a promising candidate to be used as the gate dielectric for deep submicrometer MOSFETs.

Experimental

For the experiment, Al/TaN/CeO_2/p-Si capacitors were fabricated on 4 in. p-type (100)-oriented Si wafers. All samples were first cleaned by a standard RCA clean, then deposited a 5 nm CeO_2 film by electron-beam evaporation. Before this deposition, some samples were treated in an NH_3 ambient at 700°C for 5 min in a low-pressure chemical vapor deposition (LPCVD) system. These samples were termed as the surface nitridation pretreatment (SN) samples. Then samples were furnace annealed in an N_2 ambient at 400-800°C for 15 min. This process is then termed the FA process. For the samples which were not SN treated, some of them were applied by an N_2O plasma at 20 W for 5 min in a high-density plasma (HDP) system (these samples are termed as PN samples), and some of them were rapid thermal annealed in N_2 at 400-800°C for 1 min (these samples are termed as RTA samples). Hence, four groups of samples, namely, FA, SN + FA, PN, and PN + RTA samples, were prepared. They are compiled in Table I with the steps of treatments and the key processes. The reason for preparing so many splits of samples is for comparative study. Then a TaN film of 25 nm was deposited on each sample by use of a sputter, and a 500 nm Al film was deposited on the TaN film by use of a thermal coater. After that, the gate of the capacitor of an area of 7.85×10^{-5} cm^2 was defined lithographically. Finally, a 500 nm Al film was also deposited on the back side of the wafer to form the ohmic contact. The effective oxide thickness (EOT) was estimated by the high-frequency (0.1 MHz) capacitance *vs.* gate voltage (C-V) curve in the strong accumulation region without considering quantum mechanical effects. The physical thickness was checked by high-resolution transmission electron microscopy (HRTEM). The electronic spectrum-scope for the chemical analysis (ESCA) spectra of these samples were measured using a PHI 1600 spectrometer. Moreover, the electrical properties were measured by using an HP 4156B semiconductor parameter analyzer and an HP4284A precision LCR meter.

Results and Discussion

Figure 1 plots the change of EOT, ΔEOT, *vs.* the postannealing temperature of the cerium dielectrics for the FA, SN + FA, and PN + RTA treatment, respectively. From the figure it can be seen that the FA treatment increases EOT, but the presurface treatment in NH_3 (SN) helps to retard this phenomenon. However, the PN + RTA samples not only exhibit the best thermal stability but also reduce EOT of the dielectrics. Figure 2 shows the negative current-density *vs.* gate voltage (-*J*-*V*) characteristics of As, FA4, SN + FA6, PN, and PN + RTA8 samples, where As, FA4, SN + FA6, and PN + RTA8 represent that the samples were as-deposited, annealed at 400, 600, and 800°C, respectively, and PN indicates that the sample was N_2O plasma treated in HDP. It can be

Table I. Splits of samples of different treatments for comparative study.

Sample	FA	SN + FA	PN	PN + RTA
Pretreatment		NH_3 700°C 5 min in LPCVD		
Post-treatment	N_2 15 min 400-800°C in furnace	N_2 15 min 400-800°C in furnace	N_2O 20 W 5 min in HDP	N_2O 20 W 5 min in HDP; N_2 30 s 400-800°C in RTP
Key process	Al/TaN / CeO_2 / p-Si ← FA	Al/TaN / CeO_2 / p-Si ← FA ← SN	Al/TaN / CeO_2 / p-Si ← PN	Al/TaN / CeO_2 / p-Si ← PN +RTA

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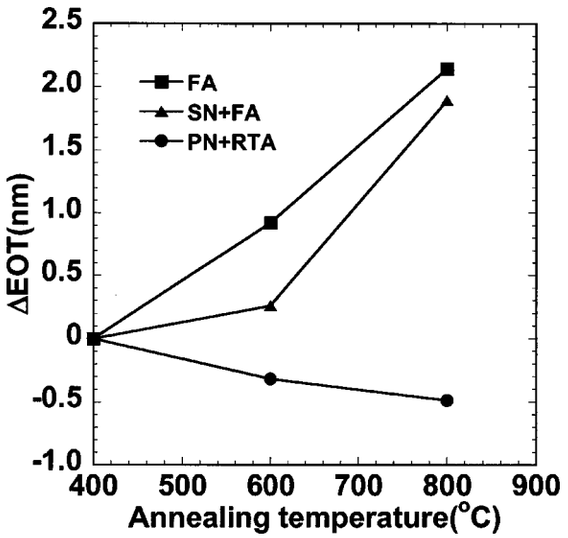

Figure 1. Plots of the increase of EOT (Δ EOT) *vs.* the postannealing temperature of CeO_2 with FA, SN + FA, and PN + RTA treatments. The PN + RTA samples exhibit the best thermal stability.

seen that SN, postnitridation (PN), and annealing (FA and RTA) processes improve the *J-V* characteristics as compared to the as-deposited characteristics, while the SN + FA6 sample has the most improvement and the PN + RTA8 sample has the highest breakdown voltage. Figure 3 shows the high-frequency C-V characteristics of (a) FA4 and SN + FA6 samples, and (b) PN and PN + RTA8 samples, respectively, where the C-V characteristics were measured by sweeping the gate voltage from accumulation to inversion and then sweeping back (-3.0 V $\rightarrow$ $+1.0$ V $\rightarrow$ -3.0 V). No characteristics of the As sample are shown because the sample was so leaky that its C-V curve could not be measured. Figure 3a reveals that the SN + FA6 sample (dashed line) exhibits a hysteresis of about 220 mV, which is much larger than that of the FA4 sample

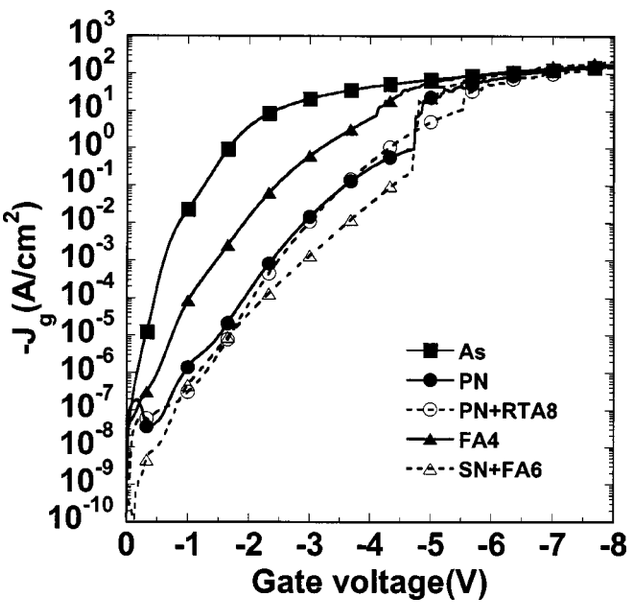

Figure 2. Plots of negative current density *vs.* gate voltage (*-J-V*) characteristics of As, FA4, SN + FA6, PN, and PN + RTA8 samples, respectively.

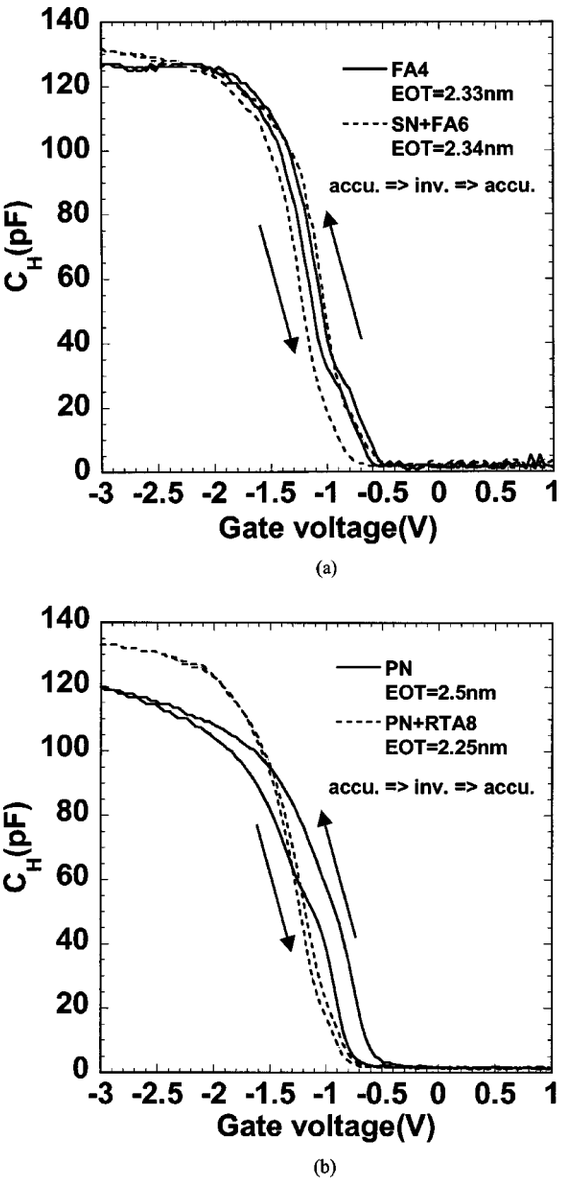

Figure 3. Plots of high-frequency capacitance *vs.* gate voltage (C-V) characteristics of (a) FA4 and SN + FA6 samples, and (b) PN and PN + RTA8 samples, respectively. All C-V curves were measured by sweeping the voltage from accumulation to inversion and then sweeping back (-3.0 V $\rightarrow$ $+1.0$ V $\rightarrow$ 3.0 V) again.

(solid line). In Fig. 3b it is seen that the PN sample has the highest EOT and the largest hysteresis, and the PN + RTA8 sample has the least hysteresis, only 25 mV.

Figure 4 shows the cross-sectional HRTEM images of (a) as-deposited, (b) FA4, (c) SN + FA6, (d) PN, and (e) PN + RTA8 samples. For all the samples, the deposited CeO_2 film on each sample varies somewhat, although the film was deposited at the same time. This means that the pretreatment and post-treatment on the surface and the deposited film do affect the deposited film. Among all the samples, it seems that the PN + RTA8 samples has the least CeO_2 thickness. Particularly, when comparing the (d) PN sample with the (e) PN + RTA8 sample, we find that there is an approximately 10% reduction in CeO_2 thickness, meaning that the RTA at 800°C densifies the film in reducing its thickness. Also there is an interfacial layer between the deposited CeO_2 film and the Si

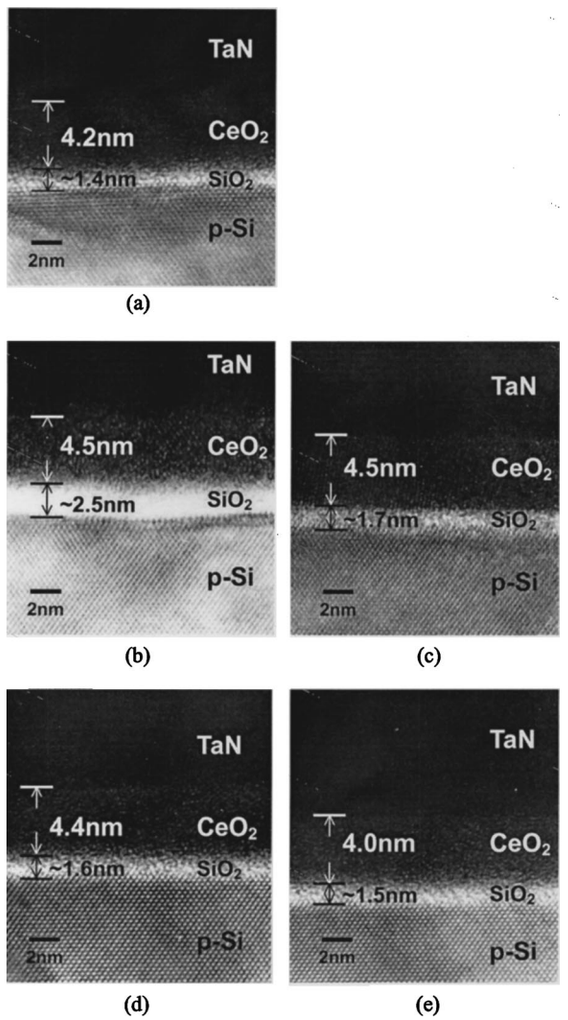

Figure 4. The cross-sectional HRTEM images of (a) as-deposited, (b) FA, (c) SN + FA, (d) PN, and (e) PN + RTA samples, respectively.

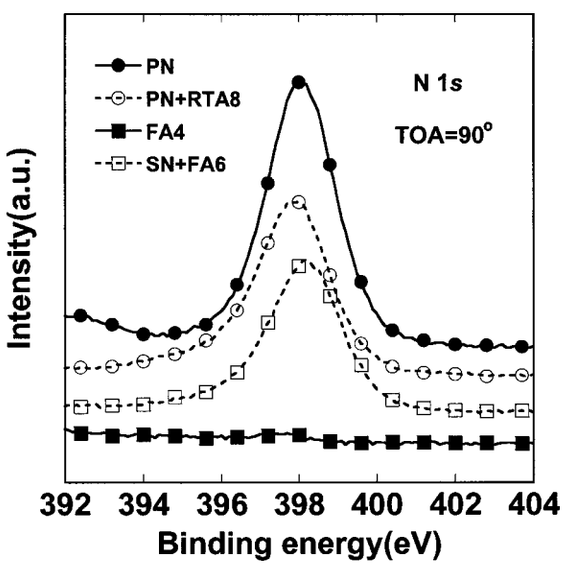

Figure 5. The chemical analysis (ESCA) spectra of the N 1s electronic spectra of FA4, SN + FA6, PN, and PN + RTA8 samples, respectively, where the N 1s peak is at 397.9 ± 0.2 eV.

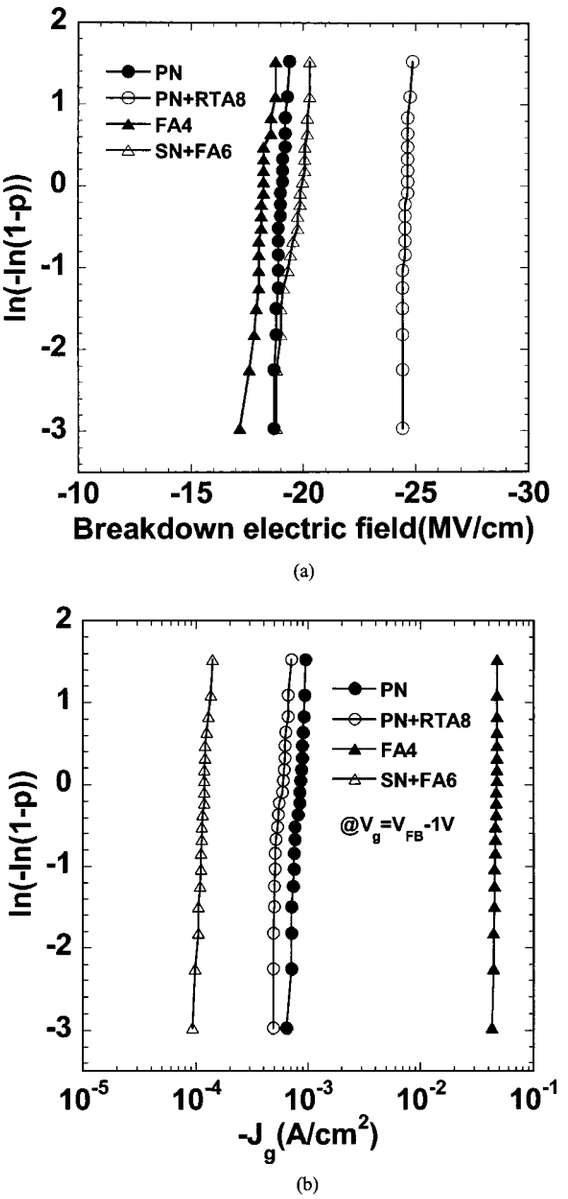

Figure 6. The Weibull plots of (a) the breakdown electric field and (b) the leakage current density at the gate voltage equaling V_{FB} − 1 V for FA4, SN + FA6, PN, and PN + RTA8 samples, respectively.

substrate for all samples and this layer is thought to be SiO_2 or silicate.[7-9] For the SN + FA6 and PN + RTA8 samples, this layer is oxynitride, because SN and PN processes offer nitrogen species into the dielectrics. Furthermore, for the PN + RTA8 sample, the following 800°C RTA further activated bondings between oxygen and silicon in the interface, making this layer a more defect-free and nonstoichiometry oxide. This, in conjunction with the more densified CeO_2 mentioned previously, makes the film have better improved electrical characteristics,[16,17] which are shown later. For the PN + RTA8 sample, the composite thickness of the CeO_2 and interfacial layer is estimated to be 5.5 nm and the effective dielectric constant of the composite dielectrics is nearly 9.53, which can be derived from the electrical thickness of 2.25 nm, obtained from the high-frequency C-V characteristics shown in Fig. 3. Also, the interfacial layer of the FA4 sample (Fig. 4b) was the largest, approximately 2.5 nm, among all the samples, due to the residual oxygen in

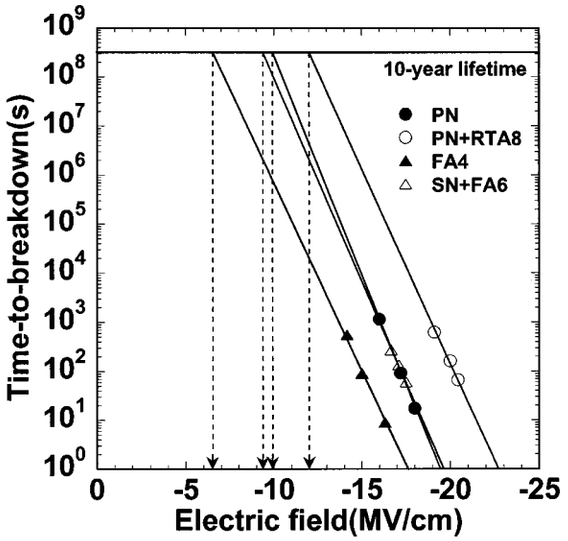

Figure 7. TDDB lifetime projection for FA4, SN + FA6, PN, and PN + RTA8 samples, respectively. The projected lifetime operation of about −12 MV/cm is observed for the PN + RTA8 sample.

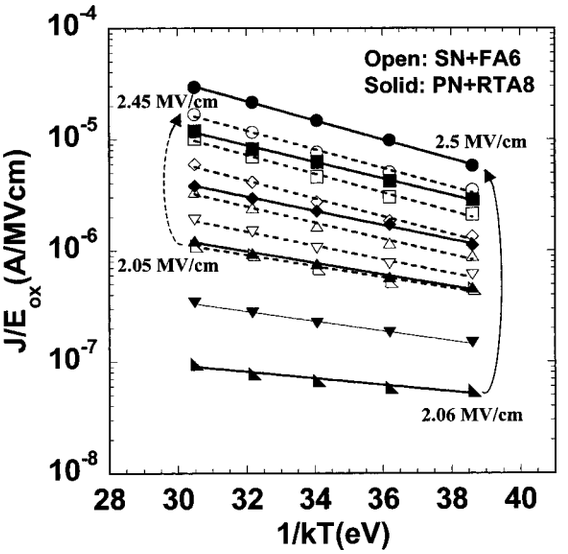

Figure 9. Arrhenius plots of gate current density at different electric fields for SN + FA6 and PN + RTA8 samples. The measurement temperature ranges from 300 to 380 K.

the furnace during a long time annealing. However, for this sample, the effective dielectric constant derived is 11.7, which is larger than that of the PN + RTA8 sample. Besides, all the processes, SN, PN, and PN + RTA, where nitrogen is involved have some effect in suppressing this interfacial layer.[18] This fact can be further supported by the data in Fig. 5 where the N 1s ESCA spectra of these samples are shown. A take-off angle of 90° was used to measure the ESCA spectra. In Fig. 5, for all samples, except the FA4, the distinct N 1s peak at 397.9 ± 0.2 eV can be observed. It is seen that the SN and PN processes can introduce nitrogen atoms into the dielectrics. Furthermore, the N 1s peak still exists even after 800°C annealing. This implies that the post-N_2O plasma and additional RTA at 800°C, in addition to densifying the structure of CeO_2 and oxynitride, may also evaporate nitrogen atoms somewhat from the CeO_2 film and the interface.

Figure 6 shows the Weibull plots of (a) the breakdown electric field and (b) the leakage current density at the gate voltage of V_{FB} − 1 V for FA4, SN + FA6, PN, and PN + RTA8 samples, respectively. The characteristics for SN + FA6, PN, and PN + RTA8 samples are all improved. Among these plots, the PN + RTA8 sample shows a breakdown electric field up to nearly 25 MV/cm and a leakage current density lower than 5.4×10^{-4} A/cm^2 at $Vg = V_{FB} - 1$ V. This is lower than the value of 1×10^{-3} A/cm^2 of International Technology Roadmap for Semiconductor (ITRS) pro-

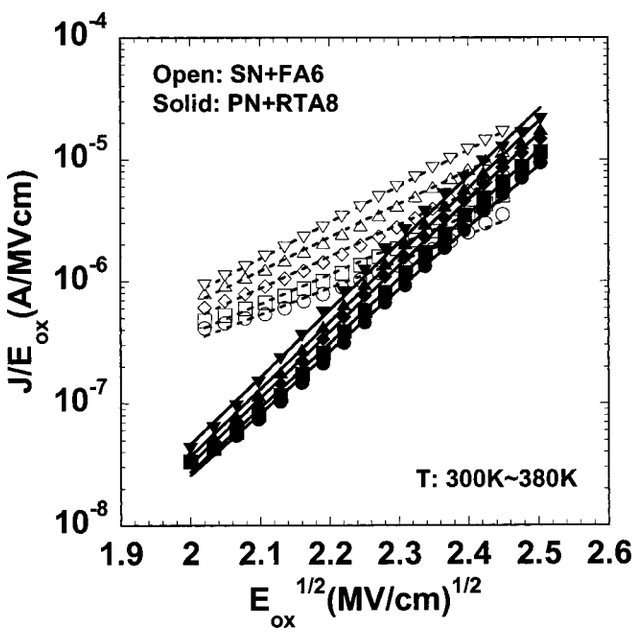

Figure 8. F-P plots of current density *vs.* oxide electric field at five measurement temperatures for SN + FA6 and PN + RTA8 samples. Linear fitting and strong temperature dependence imply F-P emission, given by $J = E_{ox} \times \exp\{-q[\phi_B - (qE_{ox}/\pi\varepsilon_i)^{1/2}]/\kappa T\}$.

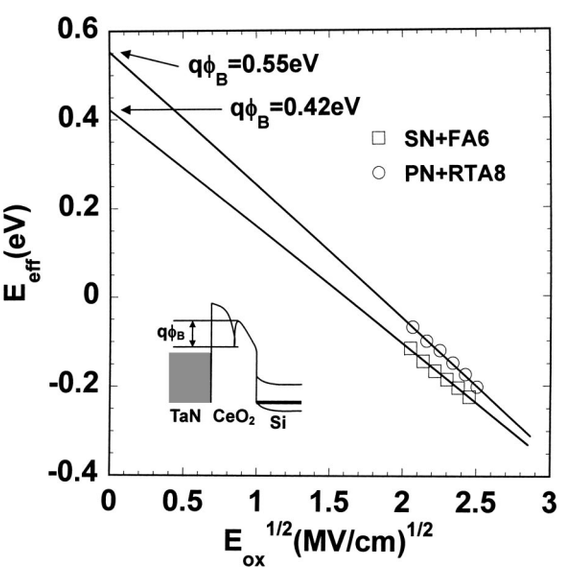

Figure 10. Graphical extrapolation of the F-P barrier height from the dependence of the effective activation energy, $E_{eff} = q[\phi_B\text{-}(qE_{ox}/\pi\varepsilon_i)^{1/2}]$, on the square root of the electric field. The barrier heights of SN + FA6 and PN + RTA8 samples are 0.43 and 0.55 eV, respectively.

Table II. Summaries of the characteristics for FA4, SN + FA6, PN, and PN + RTA8 samples. The PN + RTA8 sample exhibits superior properties in EOT, leakage current, breakdown electric field, projected 10 yr lifetime, hysteresis, and barrier height.

	EOT (nm)	E_{bd} (MV/cm)	$-J_g@V_g = V_{FB}$-1V (A/cm^2)	E_{10y} (MV/cm)	ΔV_{FB} (mV) (Hysteresis)	$q\phi_B$ (eV)
FA4	2.33	−18.24	4.6×10^{-2}	−6.5	80	0.32
SN + FA6	2.34	−19.87	1.1×10^{-4}	−9.3	220	0.42
PN	2.5	−19	7.13×10^{-4}	−9.9	240	0.5
PN + RTA8	2.25	−24.67	5.4×10^{-4}	−12	25	0.55

jection and is much lower than 0.1 A/cm^2 for pure SiO_2 with similar EOT.[19,20] These improvements are believed to be attributed to the nitrogen incorporation by the N_2O plasma and the consequent RTA that improves the dielectrics. On the plots, it can also be observed that the SN + FA6 samples have a higher breakdown electric field and a lower leakage current density than those of the FA4 samples. This is also believed to be due to the introduction of nitrogen atoms in CeO_2 and the interfacial layer. Figure 7 shows the time-dependent dielectric breakdown (TDDB) lifetime projection for these samples. In the figure, similarly, we can see large increment in the projected electric field for the 10 yr lifetime when comparing the SN + FA6 sample with the FA4 sample, and a electric field of approximately −12 MV/cm for the 10 yr lifetime operation for the PN + RTA8 sample.

Figure 8 show the Frenkel-Poole (F-P) plots of current density *vs.* the oxide electric field for SN + FA6 and PN + RTA8 samples at the measurement temperature ranging from 300 to 380 K. The linear lines suggest that the carrier transport mechanism for these samples is the F-P mechanism.[21] Figure 9 presents the Arrhenius plots for the samples of Fig. 8 for currents at several electric fields. The thermally activated behavior further supports that the carrier transport is F-P emission. The effective barrier heights, ϕ_B, derived for these two samples are shown in Fig. 10 to be 0.43 and 0.55 eV for SN + FA6 and PN + RTA8, respectively.[22] This implies that nitrogen in CeO_2 introduced by the post-N_2O plasma can effectively increase the barrier height for carrier transport under the F-P emission.

Table II summarizes the characteristics of FA4, SN + FA6, PN, and PN + RTA8 samples. The PN + RTA8 sample exhibits all the superior characteristics in EOT, leakage current, breakdown electric field, projected 10 yr lifetime, hysteresis, and barrier height.

Conclusions

In conclusion, CeO_2, when considered to be used as the gate dielectrics, can exhibit electrical characteristics which meet the deep submicrometer very large-scale integrated requirements, as it is applied by a post-N_2O plasma treatment followed by an RTA at 800°C. For the CeO_2 dielectrics, superior characteristics in EOT (2.25 nm), leakage current density (5.4×10^{-4} A/cm^2), breakdown electric field (−24 MV/cm), projected 10 yr lifetime (−12 MV/cm), hysteresis (25 mV), and barrier height (0.55 eV) are obtained. The reasons for these achieved characteristics are believed to be due to the nitrogen incorporation into the CeO_2 and the interfacial layer during post-N_2O plasma treatment, then the following RTA which densifies and improves the CeO_2 dielectrics.

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