

A Vario-Power ME Architecture Using Content-Based Subsample Algorithm

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Abstract —The Motion estimator is a key element in many video compression systems and it tends to dominate the power consumption in them. With increasing demand of portable, power-aware multimedia devices, an architecture that can be flexible in both power consumption and compression quality is essential. To meet this requirement, this paper presents a novel power-aware architecture, called the Vario-Power Architecture, for the motion estimation. Based on a semi-systolic array with the content-based subsample algorithm, the architecture real-time disables some processing elements to reduce power consumption. By performing the edge extraction first, a threshold is then set as the criterion of whether to enable or disable processing elements and thus the switch activities of the system can be reduced. As the simulation shows, the architecture may operate at different power consumption modes according to the remaining capacity of the battery pack giving little quality degradation and the power overhead under 0.36%.¹

Index Terms —motion estimation, VLSI architecture, video compression, power-aware architecture, subsample.

I. INTRODUCTION

The technique of motion estimation has been widely used in the video compression system for years. As the demand of portable, power-aware multimedia devices increases, an architecture that can be flexible in both power consumption and compression quality is essential. This paper presents a power-aware architecture, called the Vario-Power Architecture, which provides real-time switching of power consumption mode for conserving battery life² while it maintains the compression quality in high level. The proposed architecture is driven by the content-based subsample algorithm which maintain acceptable quality degradation when the system works at different power consumption modes; that is, the proposed architecture can perform trade-offs between power consumption and compression quality as the battery status changes. Because the control mechanism and data sequences at different power consumption modes are the same, the vario-power architecture can perform the switching of power consumption mode very smoothly. The block diagram shown in Fig.1 illustrates a typical

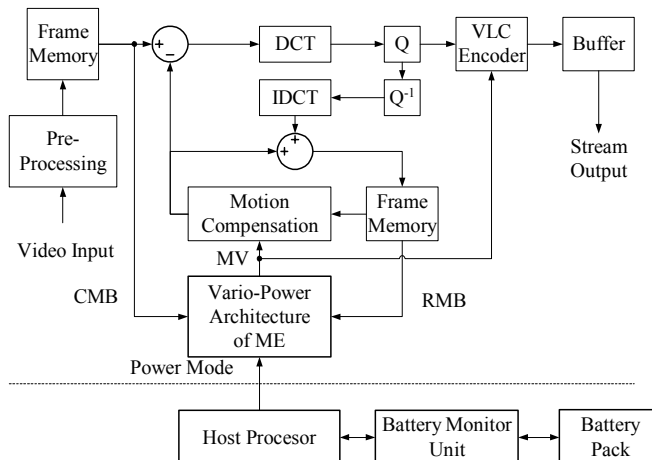


Fig. 1. A typical application of the vario-power ME architecture in a video compression system.

application of the vario-power architecture for motion estimation in a video compression system. The host processor monitors the remaining capacity of the battery pack and switches the operation mode of the vario-power element to maintain the performance of the compression system better.

Lots of published papers presented efficient algorithms for the VLSI implementation of motion estimator either on high performance or low power design. Yet, most proposed algorithms cannot adapt their system to different power consumption modes. Among these proposed algorithms, the Full-Search Block-matching (FSBM) algorithm with Sum of Absolute Difference (SAD) criteria is the most popular approach for motion estimation because of its considerably good quality. There are many types of architecture which have been proposed for the implementation of FSBM algorithms [2] [3] [4] [5]. However, a huge number of comparison/difference operations result in high computational load and significant power consumption. To reduce the computational complexity of FSBM, researchers have proposed various fast algorithms by reducing the searching steps [6] [7] [8] [9] [10]. Unfortunately, these fast algorithms suffer from irregular block-matching scheme and much worse quality than FSBM, and they are not suitable for the implementation of vario-power architecture. Papers in [11] and [12] may reduce the computational load without degrading the compression quality; nevertheless, they both require additional operations for each search step and cannot adapt themselves to different power consumption modes. The Novel Early-Jump-Out (NEJO) technique in [13] addressed the low-power architecture with some quality degradation. However, the EJO also requires extra operations for each search step and is not feasible enough for vario-power architecture.

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² The idea is motivated from the SpeedStep™ technology of Intel [1].

Articles in [14] and [15] present subsample algorithms to significantly reduce the computation cost with low quality degradation. The reduction of computational cost implies saving of the power consumption, and the power consumption can be reduced by simply increasing the subsample rate; thus, the subsample algorithms are very suitable for implementing the vario-power architecture. However, applying the subsample algorithms for the vario-power architecture may suffer from aliasing problem for high frequency band. The aliasing problem makes compression quality degrading rapidly as the subsample rate increases. To alleviate the problem, we extend the traditional subsample algorithm to a novel algorithm, which is called the content-based subsample algorithm. In our approach, we first use edge extraction techniques to separate the high-frequency band from a macro-block and then perform subsampling within the low-frequency band only. Based on the architecture proposed by Hsieh and Lin [4], we present a semi-systolic architecture which is driven by the content-based subsample algorithm. The proposed architecture can real-time alter the subsample rate as the power consumption mode changes. As the result shows, our methodology successfully switches the power mode while the quality degradation is a little.

II. GENERAL SUBSAMPLE ALGORITHM

The FSBM algorithm with SAD criteria is the most popular approach for motion estimation because of its considerably good quality and many published papers presented efficient architectures for the VLSI implementation of it [2] [3] [4] [5]. To determine the motion vector, the algorithm uses (1) and (2) to compare each current macro-block (CMB) of the frame with all the reference macro-blocks (RMB) in searching area.

$$SAD(u, v) = \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} |S(i+u, j+v) - R(i, j)|, \quad (1)$$

where $-p \leq u, v \leq p-1$.

$$SAD_{\overline{MV}} = \min_{-p \leq u, v \leq p-1} SAD(u, v) \quad (2)$$

and $\overline{MV} = (u, v) \Big|_{\min_{-p \leq u, v \leq p-1} SAD(u, v)}$

where the macro-block size is N -by- N , $R(i, j)$ is the luminance value at (i, j) in the current macro-block (CMB). The $S(i+u, j+v)$ is the luminance value at (i, j) of the reference macro-block (RMB) which is offset (u, v) from the CMB in the searching area which size is $2p$ -by- $2p$.

Many researches addressed subsample techniques for motion estimation to reduce the computation load of FSBM [14] [15]. Liu and Zaccarin, as pioneers of the subsample algorithms, significantly reduced the computational load by applying the 4-to-1 alternative subsampling to FSBM. As the simulation results show, the subsample algorithm reduces the computational load by a factor of 8 or 16 while the quality is similar to that of exhaustive search [14]. Here, we present the general subsample algorithm in which the subsample rate ranges from 4-to-1 to 1-to-1 for the vario-power architecture.

The general subsample algorithm shown in (3) uses the matching criterion which is called subsample sum of absolute difference (SSAD). In (3), the $SM_{8:m}$ which is generated from (4) is the subsample mask for the subsample rate 8-to- m .

$$SSAD_{8:m}(u, v) = \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} |SM_{8:m}(i, j) \cdot (S(i+u, j+v) - R(i, j))| \quad (3)$$

for $-p \leq u, v \leq p-1$,

where $SM_{8:m}(i, j)$ is the mask for 8-to- m subsample and

$$SM_{8:m}(i, j) = BM_{8:m}(i \bmod 4, j \bmod 4)$$

$$BM_{8:m} = \begin{bmatrix} u(m-2) & u(m-5) & u(m-2) & u(m-6) \\ u(m-3) & u(m-7) & u(m-4) & u(m-8) \\ u(m-2) & u(m-5) & u(m-2) & u(m-6) \\ u(m-3) & u(m-7) & u(m-4) & u(m-8) \end{bmatrix} \quad (4)$$

where $u(n)$ is a step function; that is, $u(n) = \begin{cases} 1, & \text{for } n \geq 0 \\ 0, & \text{for } n < 0 \end{cases}$

Using the general subsample algorithm, the power consumption can be reduced by simply increasing the subsample rate in which way the reduction of computation cost implies the saving of power consumption. Obviously, the general subsample algorithm is very suitable to implement the vario-power architecture. However, the algorithm is rather content independent and suffers from aliasing problem in high frequency band. To enhance the performance, we introduce a content-dependent technique to the general subsample algorithm as addressed in the following section.

III. CONTENT-BASED SUBSAMPLE ALGORITHM

As mentioned above, the general subsample algorithm has aliasing problem when it is in high subsample rate. The aliasing problem leads to considerable quality degradation because the high frequency band is messed up. To alleviate the problem, we use edge extraction techniques to separate the edge pixels from a macro-block and then perform subsampling to the remaining pixels.

Fig. 2 describes the procedure of the content-based subsample algorithm. The algorithm first determines edge pixels of the current macro-block and then generates the content-based subsample mask (CSM). Upon the CSM generated, we are able to calculate SSAD values and find the best motion vector. The determination of edge pixels starts from applying gradient filter in the current macro-block. In this paper, we use three popular gradient filters which are the high-pass filter, the Sobel filter and the morphological gradient filter to exercise the performance of the content-based algorithm [16]. Equations (5)-(8) illustrate their gradient calculations.

Input current and reference $W \times H$ frames;

```
for(y = 0; y < W/N; y++){
```

```
  for(x = 0; x < H/N; x++){
```

```
    Perform gradient filtering;
```

```
    Calculate the edge threshold according to power mode;
```

```
    Determine edge pixels and edge mask;
```

```
    Generate content - based subsample mask (CSM);
```

```
    SSADmin(x, y) = ∞;
```

```
    for(u = -p; u < p; u++){
```

```
      for(v = -p; v < p; v++){
```

$$SSAD(u, v) = \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} CSM(i, j) \cdot |S(i+u, j+v) - R(i, j)|;$$

```
    if SSADmin(x, y) > SSAD(u, v)
```

```
      {SSADmin(x, y) = SSAD(u, v); MV(x, y) = (u, v); }
```

```
    }//for loop index v
```

```
  }//for loop index u
```

```
}//for loop index x
```

```
}//for loop index y
```

Fig. 2. The procedure of the content-based subsample algorithm.

High-Pass Filter:

$$G_{hpf}(i, j) = |MF(HPF_{mask}, R(i, j))|,$$

$$\text{where } HPF_{mask} = \begin{bmatrix} -1 & -1 & -1 \\ -1 & 8 & -1 \\ -1 & -1 & -1 \end{bmatrix}. \quad (5)$$

Sobel Filter:

$$G_{sobel}(i, j) = |MF(SX_{mask}, R)(i, j)| + |MF(SY_{mask}, R)(i, j)|,$$

$$\text{where } SX_{mask} = \begin{bmatrix} -1 & -2 & -1 \\ 0 & 0 & 0 \\ 1 & 2 & 1 \end{bmatrix}, SY_{mask} = \begin{bmatrix} -1 & 0 & 1 \\ -2 & 0 & 2 \\ -1 & 0 & 1 \end{bmatrix} \quad (6)$$

In (5) and (6), the $MF(\cdot)$ function is the mask filter operation which is shown in (7).

$$MF(M, R(i, j)) = \sum_{p=-1}^1 \sum_{q=-1}^1 M(p+1, q+1) \cdot R(i+p, j+q), \quad (7)$$

where M is a $3-bx-3$ mask

and $R(i, j)$ is the luminance value at (i, j)

Morphological Gradient filter:

$$G_{morphological} = (R \oplus B) - (R \ominus B),$$

$$\text{where } B = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}. \quad (8)$$

The operation ‘ \oplus ’ and ‘ \ominus ’ denote the morphological operation of dilation and erosion respectively.

After obtaining the gradient value G , we first determine the edge threshold of this CMB as defined in (9).

$$\text{threshold} = m_1 \cdot \max\{G(i, j)\} + m_2 \cdot \min\{G(i, j)\}, \quad (9)$$

where m_1 and m_2 are set according to power mode.

Then, the algorithm uses the threshold value as a condition to pick the edge pixels and produces the edge mask by (10).

$$EdgeMask(i, j) = \begin{cases} 1, & \text{for } G(i, j) \geq \text{threshold} \\ 0, & \text{otherwise} \end{cases} \quad (10)$$

Finally, the content-based subsample mask (CSM) is generated from (11) and, therefore, the content-based subsample rate (CSR) is N^2 -to-(the number of 1's in CSM).

$$CSM(i, j) = SM_{sm}(i, j) \text{ OR } EdgeMask(i, j) \quad (11)$$

for $0 \leq i, j \leq N-1$.

Since the higher the threshold value is, the less the edge pixels will be, the CSM is highly dependent on the threshold. Thus, the switching of power mode can be done by adjusting the threshold parameters $m1$ and $m2$.

IV. THE VARIO-POWER ARCHITECTURE

According to the content-based subsample algorithm, we present a semi-systolic architecture which is based on the architecture proposed by Hsieh and Lin [4]. The vario-power architecture shown in Fig. 3 contains an edge-extraction unit (EXU), an array of processing elements (PEs), a parallel adder tree (PAT), a shift register array (SRA), and a motion-vector selector (MVS). Given the power consumption mode, the EXU extracts high frequency pixels (or edge pixels) from the current macro-block (CMB) and generates 0-1 content-based subsample masks (CSM) for the PE array to disable or enable processing elements (PEs). As shown in Fig. 4, the structure of PE array, which is used to accumulate the absolute differences of pixels column by column while the parallel adder tree sum up all the results to generate the subsample sum of absolute difference (SSAD). Finally, The MVS performs compare-and-select operation to select the best motion vector which has a minimum SSAD.

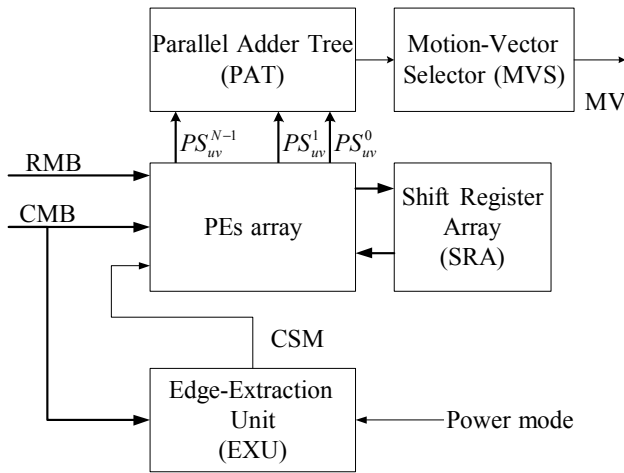


Fig. 3. The system block diagram of the content-based subsample algorithm.

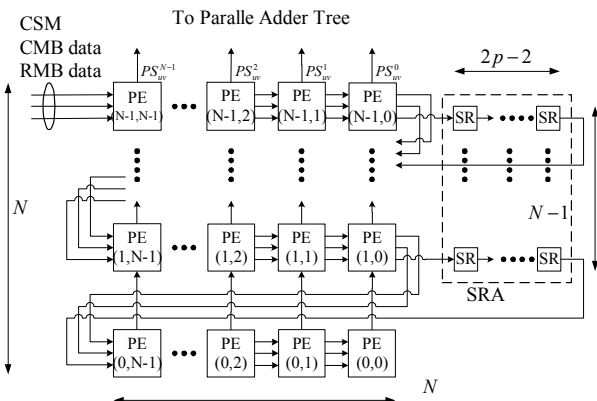


Fig. 4. The architecture of PE array and shift register array.

Since the adder operations which PE achieves dominant significant power consumption in the system, the proposed architecture driven by the content-based subsample algorithm can disable some processing elements to save the switch activity of PE; that is, it can save the power consumption of the system. By performing the edge extraction first, a threshold was then set as the criterion of how many processing elements will be turn-off. Figure 5 shows the structure of the Processing Element and explains how the CSM disables or enables the PE. The absolute difference (AD) unit, which is denoted as $|a-b|$, calculates the absolute difference of CMB and RMB pixels. Then the adder unit accumulates the absolute difference value with the partial sum from the previous PE and conveys the results to the next PE in the same column. In order to reduce the switch activity, the PE receives the CSM signals from the EXU to disable or enable the blocking registers, which is abbreviated as ‘breg’ in Fig. 5, to decide the PE is active or inactive. When the blocking registers are enabled, the data paths of AD unit and the adder unit remains still, that is, the switch activity of this inactive PE is reduced. Thus, the power consumption can be saved.

The edge-extraction unit contains two main blocks which are gradient filter and CSM generator. The implementation of

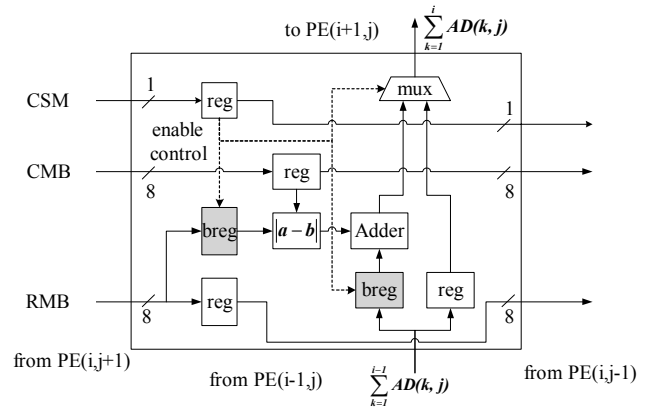


Fig. 5. The PE structure for the vario-power architecture.

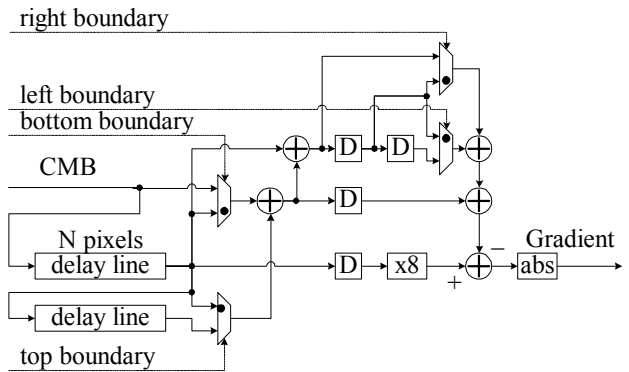


Fig. 6. The architecture to implement the high-pass gradient filter.

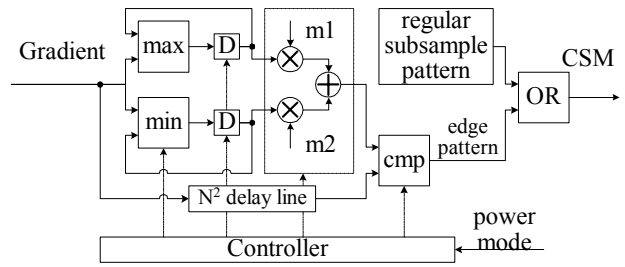


Fig. 7. The architecture of the CSM generator.

gradient filter is based on one of the (5), (6) and (8). Figure 6, for instance, is the structure of the implementation for the high-pass gradient filter. The multiplexers are used to prevent the boundary error for border pixels of the CMB. The black-dot in each multiplexer indicates the switching path when the filter is processing a border pixel. The CSM generator, whose structure is illustrated in Fig. 7, figures out the maximum and minimum of the gradient value in the macro-block and then determines the threshold value according to the power mode as shown in (9). Finally, it generates the CSM by OR-merging the regular subsample pattern and the edge pattern.

The execution of the vario-power architecture has five phases: initial CMB phase, filtering phase, edge-determination phase, initial RMB phase, and SSAD calculation phase. The initial CMB phase is for loading the CMB data into PE array and the initial RMB phase is for filling up PE array in full with RMB data to start the SSAD calculation. Figure 8 illustrates the timing of data flow. Since the execution of edge-extraction

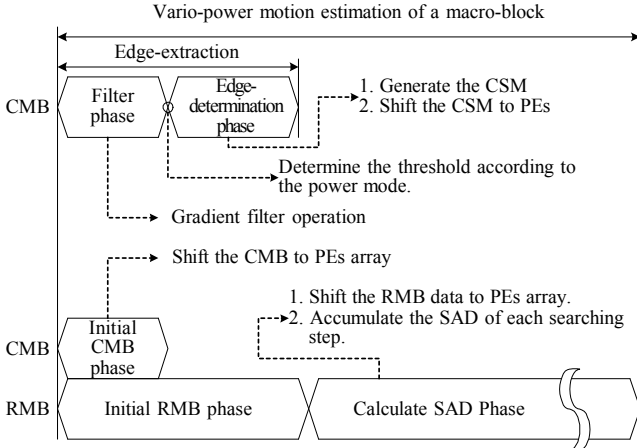


Fig. 8. The data flow of the vario-power architecture.

unit, which includes filtering phase and edge-determination phase, is parallel to the initial RMB phase, the behavior of the proposed architecture is the same as the architecture without vario-power function proposed by Hsieh and Lin [4].

V. ESTIMATION OF POWER CONSUMPTION

From (12), the power consumption of digital VLSI is in proportion to the switch activity, $f \cdot \gamma(0 \leftrightarrow 1)$.

$$P_{gate} = f \cdot C_{gate} \cdot V_{DD}^2 \cdot \gamma(0 \leftrightarrow 1), \quad (12)$$

where $\gamma(0 \leftrightarrow 1)$ is the switching rate of the gate.

Because the addition is the majority of the motion estimation architecture, by referring to [11], this paper uses the number of equivalent additions, denoted as \mathcal{E}_{adder} , as the power measure unit to estimate the power consumption. As per Fig. 5, the calculation of an absolute difference nearly requires $2\mathcal{E}_{adder}$ and each PE consumes $3\mathcal{E}_{adder}$ in each iteration. When the PE array operates at the content-based subsample rate of R_s , it requires $R_s^{-1} \cdot N^2 \cdot (2p)^2 \cdot 3\mathcal{E}_{adder}$. Since the calculation of PAT requires $(N-1) \cdot (2p)^2 \cdot \mathcal{E}_{adder}$, the power consumption of calculating SSADs for all RMBs in searching area is $12R_s^{-1}N^2p^2\mathcal{E}_{adder} + 4(N-1)p^2\mathcal{E}_{adder}$.

As regard to the EXU, three gradient filters which are mentioned in this paper consume $6N^2\mathcal{E}_{adder}$, $9N^2\mathcal{E}_{adder}$ and $8N^2\mathcal{E}_{adder}$, respectively, and the edge-determination consumes $3N^2\mathcal{E}_{adder}$. So the power consumption of the content-based subsample algorithm (P_{CSA}) can be expressed as (13).

$$P_{CSA} \cong 12R_s^{-1}N^2p^2\mathcal{E}_{adder} + 4(N-1)p^2\mathcal{E}_{adder} + \alpha N^2\mathcal{E}_{adder}, \quad (13)$$

where $\alpha \in \{9, 12, 11\}$.

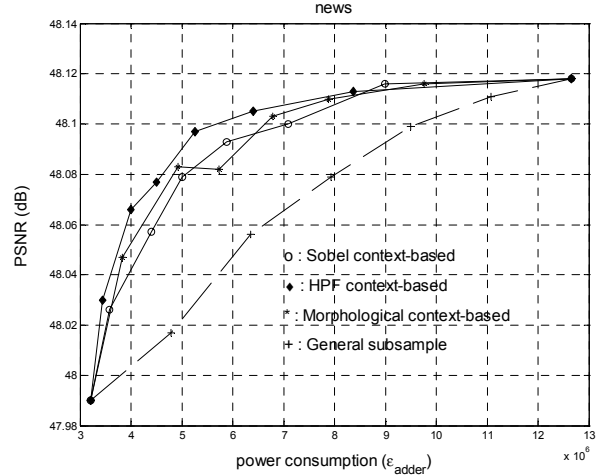


Fig. 9. The PSNR vs. power consumption of the News clip.

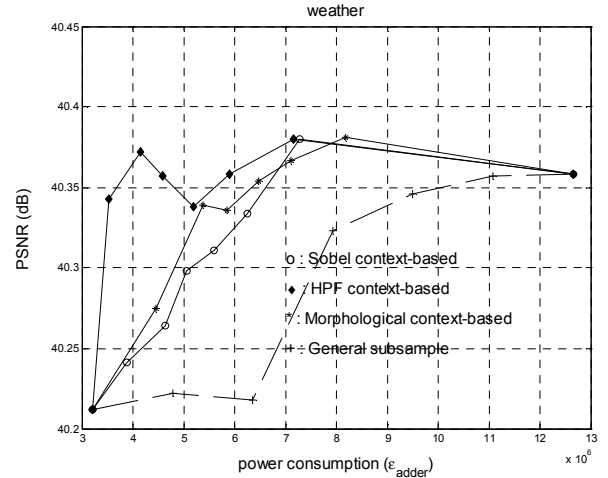


Fig. 10. The PSNR vs. power consumption of the Weather clip.

From (13), we can learn that the power overhead of EXU is a little. For the worst case, when the subsample rate is 4-to-1 and the gradient filter is Sobel-type, the power overhead is only 0.36% for the motion estimation with $N=16$ and $p=32$.

VI. SIMULATION RESULTS

Figure 9 and 10 demonstrate the simulation results of two 352-by-288 MPEG clips for $N=16$ and $p=32$. The dashed lines are the results of the general subsample algorithm and the subsample rates at the bullets are (4:1), (8:3), (2:1), (8:5), (4:3), (8:7), and (1:1), respectively from left to right. The solid lines are the results of the content-based subsample algorithm with three gradient filters and the subsample rate is from (4:1) to (1:1). The threshold parameters, (m_1, m_2) pairs, at the bullets on solid lines are (1,0), (0.75,0.25), (0.5,0.5), (0.4,0.6), (0.3,0.7), (0.2,0.8), (0.1,0.9), and (0,1), from left to right respectively. As the results, the power consumption can be significantly reduced while the quality degradation is little and the power mode can be dynamically switched by simply changing the threshold parameters.

VII. CONCLUSION

We proposed the vario-power architecture based on a novel content-based subsample algorithm. The vario-power architecture provides the real-time capability for the switching of power consumption mode while the quality degrades a little. In the proposed architecture, the edge extraction unit plays a key role to dynamically adjust the power consumption mode and its power overhead can be neglected. As shown in the simulation results, the proposed algorithm successfully improves the compression quality of the general subsample algorithm and switches the power consumption mode by the content dependent technique.

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