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Design optimization of ESD protection and latchup prevention for a serial I/O IC

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Abstract

ESD/latchup are often two contradicting variables during IC reliability development. Trade-off between the two must be properly adjusted to realize ESD/latchup robustness of IC products. A case study on SERIAL Input/Output (I/O) IC's is reported here to reveal this ESD/latchup optimization issue. SERIAL I/O IC features a special clamping property to wake up PC's during system standby situation. Along with high voltage operation, Input/Output (I/O) protection design of this IC becomes one of the most challenging tasks in the product reliability development. In the initial development phase, ignorance of latchup susceptibility resulted in severe Electrical Overstress (EOS) damage during latchup tests, and also gave a false over estimate of ESD protection threshold through parasitic latchup paths. The latchup origin is an output PMOS and floating-well ESD triggering NMOS beside the PMOS, and the main fatal link is this high-voltage (HV) NMOS connecting to a bi-directional SCR cell. This fatal link led to totally five latchup sites and three latchup paths clarified through careful and intensive FIB failure analysis, while this powerful SCR ESD device without appropriate triggering mechanism still could not provide sufficient product-level ESD hardness. Owing to there being no design window between ESD and latchup, the original several protection schemes were all abandoned. Using this bi-directional SCR ESD cell and proper triggering PNP bipolar transistors, a new I/O protection circuit could sustain at least ESD/HBM 4 kV and latchup triggering current 150 mA tests, thus accomplish the best optimization of ESD/latchup robustness.

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1. Introduction

In the failure mode distribution of modern commercial IC products, Electrostatic Discharge/Electrical Overstress (ESD/EOS) has always been the main part of reliability issue. As the process technology scales down into smaller feature size and higher integration density, ESD/EOS problem becomes more important and challenging. In the on-chip ESD protection design of integrated circuit chips, gate-grounded NMOS transistor (GGNMOS) and semiconductor controlled rectifier (SCR) are two commonly used protection elements. There have been many researches developing both ESD protection capabilities [1–5]. Both devices utilize bipolar actions to operate at low holding/snapback point. The low power value of the holding/snapback points is excellent to shunt ESD stress current and clamp ESD voltage. Specifically, ESD protection in a high voltage process is more difficult to handle. Its high voltage operation results in the weak reverse-biased drain junction for all N-type carrier devices such as NPN BJT and NMOS [6]. These devices all suffer from EOS damage

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after junction breakdown. Thus the ESD protection device options are far less than the standard logic process. High voltage operation also leads to high power value for an ESD protection device during its snapback region and this high power may damage devices/circuits more easily. Its latchup immunity is also more difficult to achieve because its high voltage power supply needs a high latchup holding voltage. In practical applications, ESD/latchup are often two contradicting variables during IC reliability development and further deteriorate ESD/latchup protection difficulty in the high voltage technology. Trade-off between the two must be carefully handled to obtain high ESD/latchup hardness.

In this paper, a design optimization example of ESD/latchup performance using SCR protection devices on SERIAL I/O IC's is presented. The ESD/latchup protection mission of this IC is not only to protect the circuits from ESD/latchup damage, but also prevent high voltage (HV) input from special input clamping effect during IC operation. The ESD/latchup requirement is inherently more difficult to obtain in the high voltage process; this ESD/latchup protection design becomes one of the toughest tasks of all developed products. Section 2 describes the original ESD/latchup design style in special environment. Section 3 gives careful and intensive FIB failure analysis to locate latchup sites and paths. Section 4 addresses the multi-chip solutions to overcome the ESD/latchup problem and obtain the best optimization.

2. Product specifications and early ESD/latchup protection style

SERIAL I/O is a CMOS Input/Output Transceiver IC for Personal Computer (PC) applications and fabricated in 0.8 μm 30 V N-sub. process to implement high voltage functions between ±12 V. Because this IC is to be applied to PC I/O noisy environment, the ESD/latchup capability must be robust enough. Its ESD protection specification is ESD Human Body Model (HBM) 3 kV at least and latchup immunity should be larger than 100 mA. The standard ESD tests complied with MIL-STD-883D standard are divided into four kinds: PS, PD, NS, and ND modes. In PD and ND modes tested IC pins are zapped by ESD pulses positively and negatively with respect to Vdd power pins, respectively, and in PS and NS modes tested IC pins are zapped by ESD pulses positively and negatively with respect to Vss ground pins, respectively. The latchup test specifications comply with the EIA/JEDEC standard 78.

In addition to the aforementioned special application environment of a high voltage process, there is another very unique clamping specification. Because this IC is the input/output port connected to an outside modem or other network device, its high voltage input will be stressed by outside wake-up signal during power-down of PC power saving status. One possible extreme situation is that PC power is intentionally switched off and a SERIAL I/O IC under power off condition might suffer from outside wake-up signal stress for an unlimited length of time. The high voltage (HV) input devices/circuits have to withstand this input signal when all IC power pins are shorted to ground. Therefore, the HV input circuits cannot introduce any PN junction directly connected to the input pads, otherwise they will forward bias the input signal and clamp the outside wake-up signal to ground. This requires that all active devices directly connected to HV input pads must be located in floating wells to isolate input clock signal.

The most difficult part of I/O protection design in SERIAL I/O IC's is the HV input pads. They need robust ESD/latchup protection scheme with no clamping effect during IC power off. The critical point of the HV input protection is that the floating well used to isolate the wake-up signal acts as a charging capacitance during ESD zapping. During ESD charging period the ESD devices behind this capacitance will respond slower than in usual situations. Under this circumstance, ESD protection devices cannot show their effectiveness at the right time. In the first several trials either clamping requirement was not satisfied or ESD performance was not enough. After several cycles of failure analysis and layout revision, the early ESD/latchup design schematics of version A are shown in Fig. 1(a) and (b), and the I–V curve of the bi-directional SCR is shown in Fig. 1(c). In Fig. 1(a) the circuit block enclosed in the dashed line box is for ESD protection purpose and the detail circuit cross-sectional view is illustrated in Fig. 1(b). The ESD protection circuit is composed of a bi-directional SCR as a primary ESD protection device and a HV NMOS as a secondary protection device to trigger the bi-directional SCR. The bi-directional SCR device exhibits symmetrical I–V shape and very good negative-resistance behavior [7]. Its ESD threshold level can be as high as 8 kV. Nevertheless, the response time of a standalone bi-directional SCR is too slow to protect internal circuit even though it can withstand ESD/HBM 6–8 kV zapping itself. Thus an HV NMOS connected to the floating well of the bi-directional SCR acts as an early triggering device to push bi-directional SCR into turn-on state during ESD events. This similar protection circuit has been applied in an analog product 27 MHz radio transceiver successfully [8]. Four P^+/N^+ guard rings circle the bi-directional SCR in order to prevent latchup during operation. The other poly and NDDD well resistors are primarily used for input impedance adjustment of IC specifications.

The high voltage (HV) output protection follows the normal high voltage ESD/latchup design rule and the schematic is shown in Fig. 1(d). It is composed of a HV PMOS with $W/L = 500/1.2$ μm as a pull-up element,

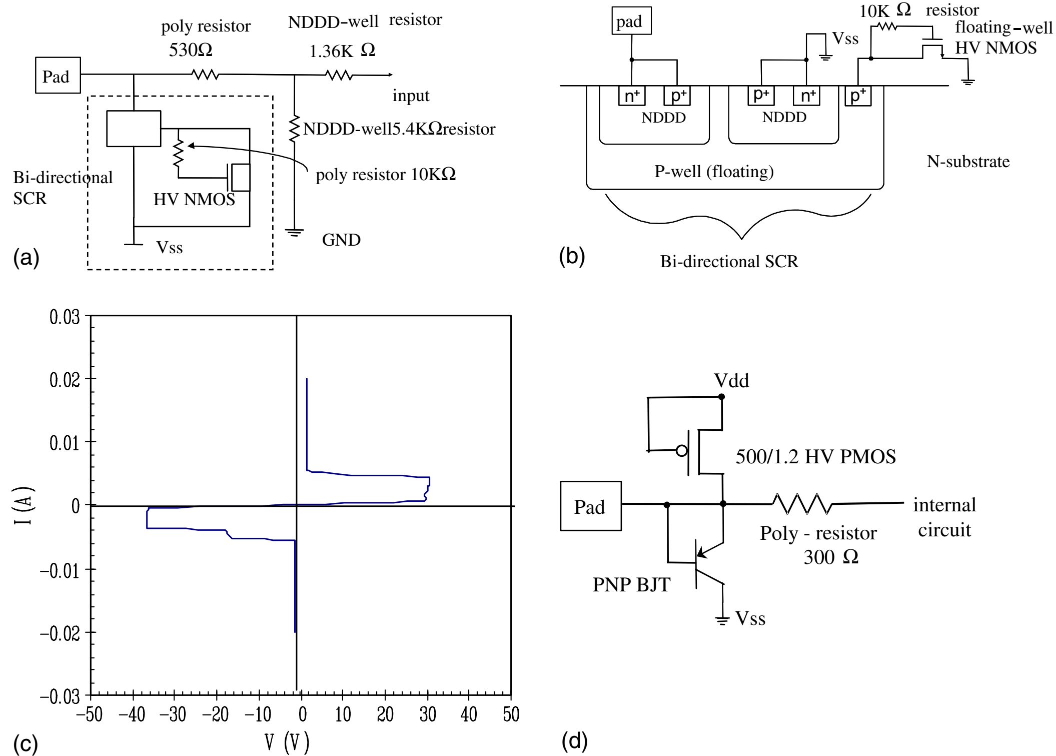

Fig. 1. (a) HV input protection circuit schematics of SERIAL IO version A. The circuit block enclosed in the dashed line box is for ESD protection purpose. The ESD protection circuit is composed of a bi-directional SCR as a primary ESD protection device and a HV NMOS as a secondary protection device to trigger the bi-directional SCR; (b) detail ESD protection cross-sectional illustration of SERIAL IO version A; (c) the *I–V* curves of the bi-directional SCR device. The bi-directional SCR device exhibits symmetrical *I–V* shape and very good negative-resistance behavior. Its ESD threshold level can be as high as 8 kV and (d) HV output protection circuit schematics of SERIAL IO version A. It is composed of a HV PMOS with $W/L = 500/1.2$ μm as a pull-up element, and a PNP BJT with emitter size 40×13 μm^2 as a pull-down element. After the two devices a 300 Ω poly resistance is connected to the pad in series into the internal circuit.

and a PNP bipolar junction transistor (BJT) with emitter size 40×13 μm^2 as a pull-down element. After the two devices a 300 Ω poly resistance is connected to the pad in series into the internal circuit. As for low voltage region, low voltage (LV) NMOS with $W/L = 500/1.2$ μm and PMOS with $W/L = 500/1.0$ μm are used for the input protection; a LV NMOS with $W/L = 450/1.2$ μm and a PMOS with $W/L = 450/1.0$ μm are used for the LV output protection. Both HV output and LV input/output region protection are implemented with the normal scheme; and they can pass ESD/HBM 2 kV and latchup 100 mA test at least. The whole chip layout of version A is demonstrated in Fig. 2(a). The central core circuit part of the layout is intentionally blank.

3. ESD/latchup failure analysis

Owing to a new phenomenon from parasitic PNPN path, SERIAL I/O version A latchup test failed and had large power pin current damage during pin #5, 6, and 8 positive current triggering; although its ESD/HBM threshold can reach 5 kV. The failure analysis method was to cut off the interconnections at the suspected latchup locations one at a time by means of focused ion beam (FIB), and then the FIB samples were tested to verify their latchup immunity. The five latchup sites identified are illustrated in Fig. 2(a). As shown in Fig. 2(b), the first failure analysis started with cutting HV NMOS sources NS1, NS4 metal contacts and vias of five input pin #2, 3, 4, 7, 9, and HV PMOS source PS1 of the neighboring output pins. Latchup test after FIB steps found that no latchup occurred from 100 to 150 mA current triggering except pin #8 only. Further triggering test up to 190 mA with five HV input pins floating showed no latchup. The floating test is intended to prevent the bi-directional SCR from turn-on and conduction. In summary, the first latchup sites are supposed to be the PNPN paths composed of the sources NS1, NS4 of the HV NMOS and sources PS1 of the neighboring

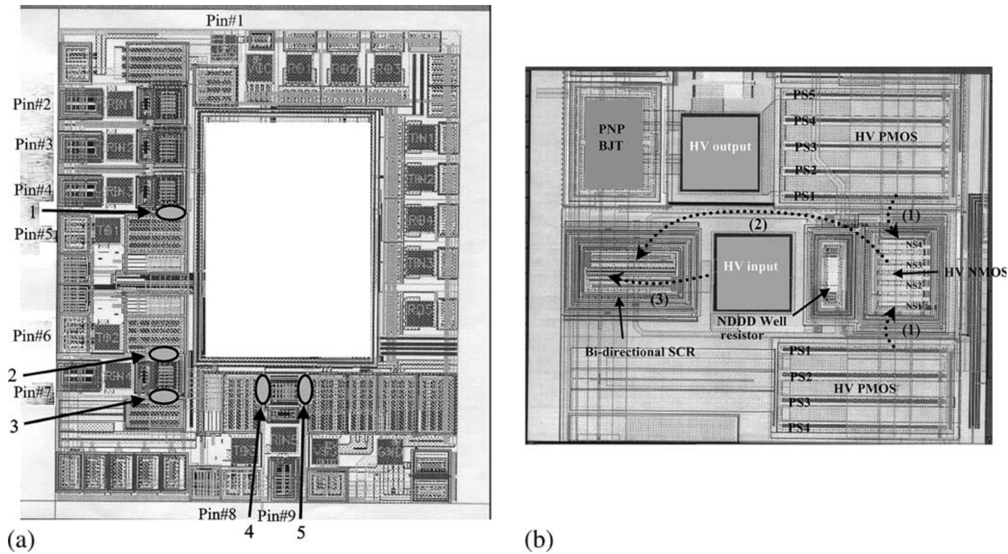

Fig. 2. (a) Whole chip layout and its latchup failure sites of the SERIAL IO version A. Its latchup test failed at pin #5, 6, and 8 positive current triggering and (b) layout of the SERIAL IO version A and its FIB cutting items for latchup FA at sites #2 and 3 marked in Fig. 2(a). The first suspected latchup sites are the PNPN paths composed of the sources NS1, NS4 of the HV NMOS and source PS1 of the neighboring HV PMOS. Next sites are the HV input bi-directional SCR's. The three latchup paths are also demonstrated by the dashed-line vectors.

HV PMOS, which are marked in Fig. 2(a) and (b). Next sites are the HV input bi-directional SCR's. In the ESD part, ESD/HBM performance of the samples after FIB cutting reduced to ND mode 3 and 4 kV function failures.

In order to fully clarify any potentially unknown failure cause, further FA steps continued to investigate the original latchup problem of SERIAL I/O version A as shown in Table 1. A total of seven FIB experimental splits were carried out as shown in the first part of Table 1. The test results of the seven split conditions are listed in succession. In the test result table the first column shows the operating AC current at ±12 and 5 V power pins after latchup test; the second column shows the results of the circuit function test after latchup test; and the third column shows the instantaneous latchup triggering status during latchup test. A circle mark represents that the result is normal as compared with that before latchup test; otherwise the abnormal values are recorded in the table to indicate the exact failure status. At first the experiment was FIB cutting the HV NMOS or PMOS several source fingers in the five latchup sites as demonstrated in Fig. 2(a) and (b); the main goal is to extract the appropriate P^+/N^+ spacing so that no latchup occurs in these PNPN paths. However, as shown in the experiment split 1–2 of Table 1, the results failed at least one of the function tests, AC power pin current values, and instantaneous latchup triggering status. Latchup still happened though several HV NMOS sources were cut out. This reveals that there were still potential latchup paths that were not found.

The second batch of FIB experiments are listed in split 3–7 of Table 1. This time FIB sites extend to the whole HV NMOS connection in protection circuits and other devices such as N Double Diffused Drain (NDDD) well resistors, power clamp ESD devices. The condition split 4 is the same as split 3 but was carried out after split 3 successively. Both split 3 and 4 results combined to give a quite low latchup occurrence rate. But latchup damage still happened even if all HV NMOS sources were cut out, although the occurrence rate became reduced. In split 5–7 all latchup criteria were satisfied. The common factor is the all HV NMOS sources/drains being deleted. Hence, it is very possible that the main critical points are HV NMOS drains connecting to floating well bi-directional SCR's. The other ever suspected elements are not the critical parts. Cutting power clamp devices in split 3 and 4 still cannot avoid latchup damage occurrence. Cutting NDDD well resistances in split 6 seemed to obtain a latchup-free status. But in view of split 5–7, retaining the resistances just gave the same latchup free results. The overall experiment results are summarized in Fig. 3(a) and (b). The first part of the chart is the comparison of the latchup threshold levels. The latchup thresholds are at most 50 mA for all split 1–4 cases, while for split 5–7 the thresholds are promoted to at least 100 mA. This implies that split 5–7 have eliminated all the possible latchup

Table 1
FIB split conditions to solve version A latchup issue and their FIB experiment results of the FIB splits

(1)	Cutting NMOS-S4 and PMOS-S1
(2)	Cutting NMOS-S2 and S4
(3)	Cutting NMOS all sources and power clamp devices
(4)	Cutting power clamp devices and all NMOS sources
(5)	Cutting all NMOS drains/sources
(6)	Cutting all NMOS drains/sources and input NDDD-well resistor
(7)	Cutting all NMOS sources and bi-directional SCR ± nodes

	AC power current			Function after test	Current triggering result
	+12 V	−12 V	+5 V		
Split-1 cutting NMOS-S4 and PMOS-S1 (50,100 mA triggering pin #5, 6, and 8)					
1-1	14.15 mA	−16.51 mA	O	O	#6 latchup during 100 mA trigger
1-2	O	O	O	O	No latchup during trigger
Split-2 cutting NMOS-S2 and S4					
2-1	7.57 mA	0.1362 mA	O	X	No latchup during trigger
2-2	O	O	O	O	No latchup during trigger (50 mA only)
2-3	1.3208 mA	1.451 mA	5.651 mA	X	#5 latchup during 100 mA trigger
2-4	13.308 mA	−15.277 mA	O	O	#6 latchup during 100 mA trigger
2-5	13.82 mA	−16.05 mA	O	O	#5 latchup during 100 mA trigger
Split-3 cutting NMOS all sources and power clamp devices					
3-1	O	O	4.7 mA	X	No latchup during trigger
3-2	O	O	O	O	No latchup during trigger
Split-4 cutting power clamp devices and all NMOS sources					
4-2	O	O	O	O	No latchup during trigger
4-3	O	O	O	O	No latchup during trigger
Split-5 cutting all NMOS drains/sources					
5-2	O	O	O	O	No latchup during trigger
5-3	O	O	O	O	No latchup during trigger
Split-6 cutting all NMOS drains/sources and input NDDD-well resistor					
6-1	O	O	O	O	No latchup during trigger
6-2	O	O	O	O	No latchup during trigger
6-3	O	O	O	O	No latchup during trigger
Split-7 cutting all NMOS sources and bi-directional SCR ±nodes					
7-1	O	O	O	O	No latchup during trigger
7-3	O	O	O	O	No latchup during trigger

causes. In the second part, the failure rate percentage data have a tendency that decreases with the progress of the FIB experiments. For split 1 and 2, there were 50–100% high failure rates, and reduced to 25% in split 3 and 4. The failure rates further vanished to zero for next split 5–7. As a whole, the data show that cutting HV NMOS drain metal connection to the bi-directional SCR cell can eliminate final latchup occurrence. The NDDD well input resistors and the power clamp ESD devices are irrelevant to latchup failure.

The basic latchup physical model is further illustrated in Fig. 4(a). Fig. 4(a) shows latchup I–V curve of a PNPN structure inserted in the same figure. The N^+/N Double Diffused Drain (NDDD), P^+/P Double Diffused Drain (PDDD) source diffusions of the HV NMOS and HV PMOS, the HV p-well, and the N-substrate form a pair of lateral and vertical parasitic bipolar transistors as inserted above Fig. 4(a). An inherent PNPN SCR structure results from these two BJT with one collector connected to the other base. This parasitic SCR structure stays in the high impedance condition normally. Under certain abnormal conditions, the emitter–base junction may be forward biased and the BJT may be triggered to ON state at the switching point (V_S, I_S) in Fig. 4(a). If the current gain is sufficiently large to cause positive feedback, the PNPN structure is switched to a low impedance, low voltage, high current state and stay above the holding point (V_H, I_H) in Fig. 4(a). This status is defined as latchup and is self-sustaining whenever the power supply is available [10,11]. In high voltage

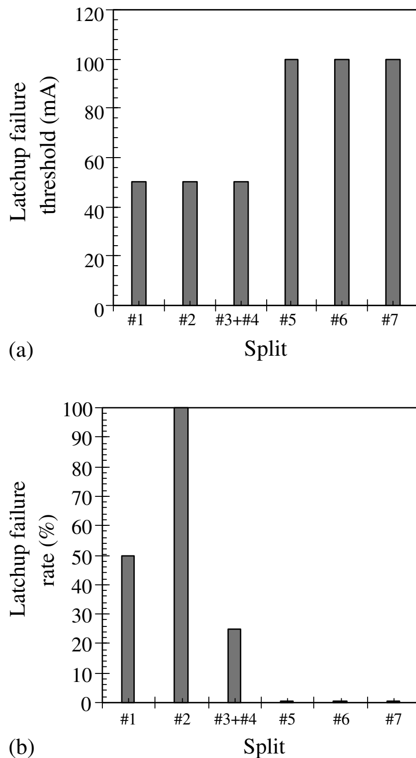

Fig. 3. (a) Latchup failure threshold distribution plot, and (b) latchup failure rate distribution plot extracted from the data of the FIB FA experiments in Table 1.

technology, the latchup power is large enough to destroy the whole structure instantly due to its high voltage and current. At the switching point between (V_S, I_S) and (V'_S, I'_S), its I–V curve trace will be shifted by various external triggering sources to become easily latchup, which is just the same as the present case in this work.

Based on careful investigation and intensive analysis, the following three latchup paths are proposed as illustrated in Figs. 4(b) and 2(b):

Path (1). This is the original path proposed in the first FIB experiment; it is from output PMOS sources to input floating well NMOS sources.

Path (2). This is the second path found based on the suggestion of the early version layout experiment. It is from output PMOS sources to input NMOS drains to bi-directional SCR Vss; which is just like an SCR in series with a forward diode.

Path (3). The latchup path (2) itself can also trigger the bi-directional SCR as well because the bi-directional SCR is much more sensitive than paths (1) and (2). Latchup path (3) is from input through bi-directional SCR to Vss, just the same as the normal path for ESD use. This path was also the second suspected target in the first FIB experiment; any trigger noise from anywhere may trigger this latchup path.

In the path (1) the triggering source, i.e., the HV PMOS drain, is just located at the close neighbor of the latchup path, i.e., HV PMOS sources; it is no doubt that the latchup susceptibility is very significant. These three latchup paths are strongly coupled chain reactions. The damage scale is very serious due to multiplication of these chain reactions in the high power operation environment. They could hardly be clarified without intensive experiments and analyses. The three paths seem complex due to their long listing; but the implication behind is quite simple: the floating well trigger NMOS is originally designed to trigger bi-directional SCR during ESD event, but now it also provides latchup path at the same time, although there are four guard rings surrounding the SCR cell. This reason can also be realized from the results of the past versions. Starting from the early version, the ESD threshold of the standalone bi-directional SCR cells cannot reach 3 kV but latchup property is normal. In the version A, a triggering HV NMOS with 10 kΩ resistor coupled to the gate was connected to the floating p-well of the bi-directional SCR cells. This time ESD threshold reached 5 kV, but latchup failed even for 50 mA triggering tests. In the further FIB test split only one pair of NMOS/PMOS sources were deleted, the latchup issue was not completely solved yet ESD threshold had decreased to 2 kV again. Considering this situation, the actual critical link is the HV NMOS connecting to the SCR floating well. This fatal link significantly reduces the latchup switching point to (V'_s, I'_s) as shown in Fig. 4(a). The latchup paths provide a conduction route during ESD event, when the latchup paths are removed latchup immunity improves but ESD level decreases. ESD and latchup are frequently two competing factors that must be taken into account all together; otherwise the ESD protection approach should be modified in order to satisfy both the requirements.

4. Multi-chip ESD/latchup solutions and discussions

As a whole, FA results showed that both ESD and latchup performance are strongly coupled together. The past protection schemes all exhibited inadequate design window. Based on this consideration, the final decision is proposed to try different kinds of layouts simultaneously for any possible resolution. One resolution is to eliminate latchup paths only by separating P^+/N^+ spacing, and ESD protection remained unchanged. New ESD protection split was also included in case the original protection design did not work. These design splits were taped out in a single mask set together in order that all possible solutions have been included without further cycle time consumption. The multi-chip split plan is as follows. (1) Version B—HV PMOS P^+ source/HV NMOS N^+ source spacing 100 μm with only two guard

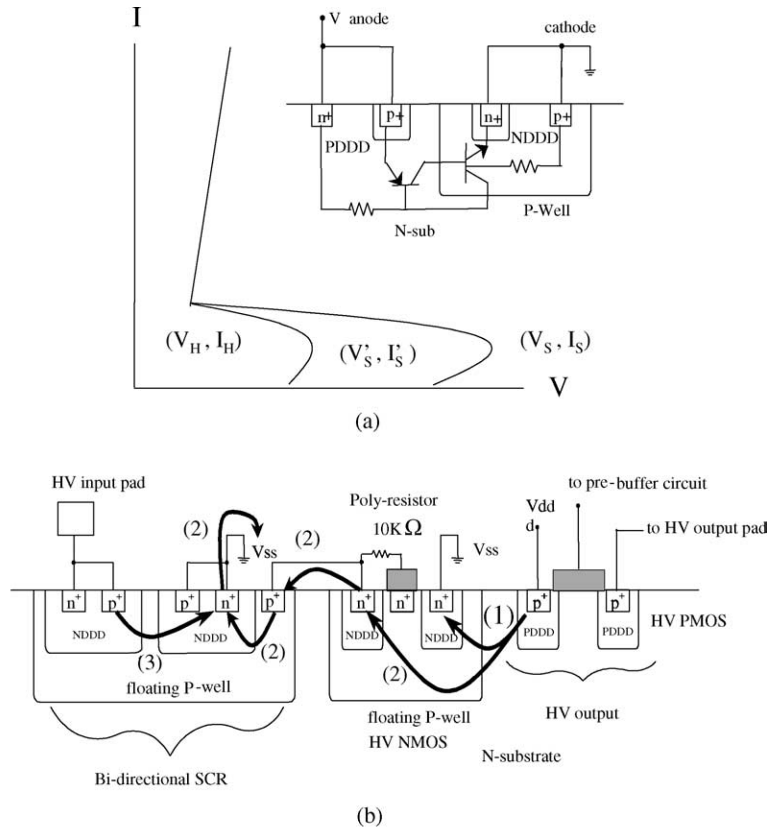

Fig. 4. (a) Latchup current–voltage curve of a PNPN structure which is inserted above this curve. At the switching point between (V_S, I_S) and (V'_S, I'_S), its I–V curve trace will be shifted by various external triggering sources to become easily latchup and (b) Input/output protection cross-sectional view to show the three latchup and triggering paths of version A. The main fatal link is the floating-well HV NMOS connecting to the bi-directional SCR cell.

rings between them. (2) Version C—HV input trigger NMOS' are replaced by floating-well PNP BJT's as a different triggering scheme. The HV input ESD protection circuit schematic of version C is shown in Fig. 5. A floating-base pull-up and pull-down PNP BJT are put into the I/O protection circuit. The pull-up PNP BJT is used for ESD ND and PD mode protection. The floating base of the PNP BJT is intended to meet the clamping test requirement. A PNP BJT itself has no latchup node and would not interact with a PMOS as a latchup path. It is also immune to EOS junction failure of normal HV N-type devices. The input series resistor 1.36 kΩ is already available as a part of input circuit specification. Here it is utilized at the same time to raise the pad voltage after pull-down PNP BJT breakdown and push the SCR cell to switch on earlier.

The final ESD/latchup test results are shown in Table 2. The new protection design of version C all passed ESD/HBM 2/3/4 kV, and latchup ±150 mA test. The other just passed ESD 2 kV. Further margin tests on version C showed that in ESD 5 kV test only ND mode

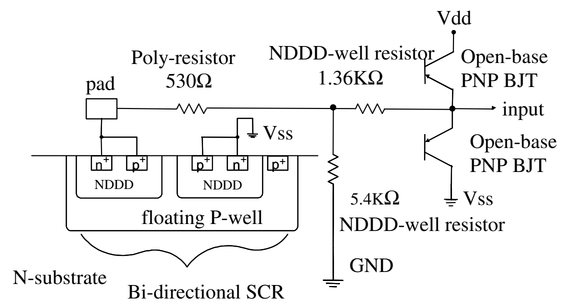

Fig. 5. Input/output protection schematics of the version C in the multi-chip layout. HV input triggering NMOS is replaced by floating-well pull-up and pull-down PNP BJT's as a different triggering scheme. The pull-up PNP BJT is used for ESD ND and PD mode protection.

1/3 failed at slightly larger power pin current but still within product power consumption limit, and other test items were all normal. Its 5 kV result can be regarded

Table 2
Final ESD/latchup test result summary of multi-chip splits and the previous version

Layout version	ESD/HBM test	Latchup test
Version A BSD circuit in Fig. 1	2–5 kV passed	±50 mA failed
Version B	2 kV passed	±100 mA passed
P^+/N^+ spacing 100 μm with two guard rings	3 kV ND failed	
Version C new BSD circuit in Fig. 5	2–4 kV passed	±150 mA passed

as a pass actually. It becomes the final layout for mass production.

At the beginning of the FA process, there are thousands of parasitic PNPN sites in a whole chip layout. The starting points where to apply FIB technique are somewhat difficult to select and require strong device sense and experience. One important technique is to implement various kinds of device-level latchup testkeys in terms of the typical layout styles that frequently appear in the real chips. These testkeys are primarily designed to extract latchup design rule and may be very beneficial to practical integrated circuit FA. During layout rule extraction, any PNPN structure with floating substrate/well pickup is found to be very sensitive to noise triggering, latchup will even be induced by triggering current of order as low as nA. This is because in the floating-pickup substrate/well, the substrate/well resistance can be regarded as very large to infinity. A large well/substrate resistance will enhance latchup susceptibility. This corresponds to the very low voltage/current switching point in Fig. 4(a). Hence, the first action was naturally started from these most vulnerable locations, i.e., the floating-well input pins. The FIB experiments later have proved this validity exactly.

There are five HV input pins with exactly the same layout as shown in Fig. 2(a), but the identified latchup sites involved with only three of them. The triggering injectors are the HV PMOS drains located just beside three latchup sites. Hence latchup failures happened only at these vulnerable locations. In the ESD respect, it seems that zapping each of the five HV inputs yielded the same threshold level no matter all five HV inputs exhibited two different kinds of latchup behavior. In the past FA example of other flash memories, it was ever found that latchup sites of EMMI hot spots can be about thousands microns away from the triggering pin location. This is assumed to be a chain reaction that latchup is first initiated at the area near the triggering pin, and then spread out to other high latchup susceptibility locations merely by power bus transportation. This distant spreading behavior is now applicable here. Thus, during ESD zapping at the five HV inputs the latchup incident spreads out through the five highly sensitive paths by chain reaction, and results in an abnormally high ESD threshold level.

The bi-directional ESD cell exhibits very good ESD robustness by itself but shows no special ESD protection level when applied to this IC product. The device-level ESD performance is far different from whole product-level or chip-level performance. This is a common experience to those dealing with ESD/latchup protection design [9]. Here a bi-directional SCR is good enough to withstand ESD stress itself but it responds slowly with respect to ESD transient pulse waveform. It cannot absorb ESD power promptly, and this power flows into internal circuits and leads to permanent damage due to its high switching voltage. For ESD/Charged Device Mode (CDM) this situation is supposed to deteriorate further. Hence careful tailoring of triggering schemes for protection circuits is essential to fully exploit the ability of an ESD device and vital to ESD robustness in products.

During FA process the product function test also found that the old input/output design cannot pass clamping test even for normal dies after several minutes or even 10–30 s pulse stress at input pins. A series of FIB FA experiments were done to find out clamping failure sites. After cutting the triggering HV NMOS connection to bi-directional SCR cells, the clamping decay problem disappeared. The failure origin is caused by the bi-directional SCR cell turn-on induced by the HV NMOS at the HV input. The reason is that HV NMOS injects carriers into the bi-directional SCR floating p-well through triggering metal line during continuous AC input waveform stress. When the floating p-well has collected sufficient charge amount, the potential will drive carriers to trigger the bi-directional SCR into turn-on. From this result, the HV NMOS connecting to the floating well of the bi-directional SCR is the weakest link in the chip, which is exactly the same as the ESD/latchup failure origin.

5. Conclusion

The works of different development teams in the past few years tried many different kinds of protection devices and schemes for the SERIAL I/O IC, but never reached the final goal successfully. The latchup problem not only led to severe EOS damage but also gave a false high ESD threshold level. Detailed and intensive failure analyses have been carried out to solve its ESD/latchup failure problem. Its latchup failure sites have been found

to be located at the HV NMOS of the HV input pads and the HV output ESD protection PMOS beside the HV input, and the main fatal link is this HV NMOS connecting to a bi-directional SCR cell. Because the trade-off design window had been pushed to the limit, the original HV input protection schemes were all abandoned. A new ESD protection circuit was implemented into the SERIAL I/O chip, and exhibited robust ESD/latchup hardness as well as qualified clamping property. From the lesson given by this example, a powerful ESD protection device does not automatically guarantee a good product-level ESD threshold, the final product ESD hardness will be possible only when proper triggering mechanisms applied to the primary protection devices. Those who deal with input/output protection work should fine tune the protection design parameters in order to achieve ESD/latchup robustness in products.

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