Journal of The Electrochemical Society, **151** (2) G144-G148 (2004)
0013-4651/2004/151(2)/G144/5/$7.00 © The Electrochemical Society, Inc.

Effects of Process and Gate Doping Species on Negative-Bias-Temperature Instability of p-Channel MOSFETs

Da-Yuan Lee,[a] Tiao-Yuan Huang,[a] Horng-Chih Lin,[b,z] Wan-Ju Chiang,[a] Guo-Wei Huang,[b] and Tahui Wang[a]

[a] *Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan*
[b] *National Nano Device Laboratories, Hsinchu 300, Taiwan*

The effects of poly-Si gate doping type and species as well as thermal treatments on negative-bias-temperature instability (NBTI) of p-channel metal-oxide-semiconductor field effect transistors (MOSFETs) were investigated. We found that devices with n^+-poly-Si gate depict a smaller threshold voltage shift after bias-temperature stressing, compared to their p^+-poly-Si-gated counterparts. By carefully controlling the thermal budget to suppress boron penetration, NBTI can be reduced by fluorine incorporation in p^+-poly-Si-gated devices. Finally, NBTI is found to be aggravated in devices subjected to H_2 postmetal-annealing, highlighting the important role of hydrogen bonds.
© 2004 The Electrochemical Society. [DOI: 10.1149/1.1639168] All rights reserved.

Manuscript submitted April 23, 2003; revised manuscript received August 29, 2003. Available electronically January 9, 2004.

For aggressively scaled deep submicrometer complementary oxide semiconductor (CMOS) ultra large scale integrated (ULSI) technologies, an ultrathin gate oxide is essential for achieving high current drive under low power operation. The integrity and reliability of such gate oxides are therefore crucial for ULSI manufacturing. Recently, negative-bias-temperature instability (NBTI) has been identified as a major reliability concern for deep sub-micrometer p-channel metal-oxide-semiconductor (MOS) transistors.[1-4] Large numbers of interface states and positive fixed charges are generated during bias-temperature stressing (BTS), and cause an unwanted negative threshold shift in device characteristics, which could potentially lead to circuit failure. This phenomenon becomes even more pronounced as the oxide is thinned down, and may become the limiting factor for the device lifetime. It has also been shown that NBTI could be further aggravated by process-induced damages such as plasma charging,[4-6] and boron penetration.[2,4] Special attention should therefore be paid to exploring and understanding the influence of different processing steps and treatments on device characteristics.

In this paper, we characterized the NBTI of devices with different process treatments. Dependences of gate-doping types, gate, and source/drain (S/D) doping species, and postmetal annealing treatments were investigated. Some interesting findings were obtained, which could help clarify the role of different species incorporated in the device.

Experimental

Complementary MOS (CMOS) transistors used in this study were fabricated on 6 in. silicon wafers with a resistivity of 10-25 Ω cm. After local oxidation of silicon (LOCOS) isolation and threshold voltage (Vth) adjustment implantation, the gate oxide was thermally grown in a diluted O_2 ambient at 900°C. Oxide thickness measured by a n&k analyzer (and also confirmed by capacitance-voltage, C-V measurements that took into account the poly-depletion effect) on the monitor wafers before poly-Si deposition was around 3.0 nm. Undoped poly-Si layer was then deposited by low-pressure chemical vapor deposition (LPCVD). For p-MOS devices with n^+-poly-Si gate, As^+ ions (5×10^{15} cm^{-2}) were implanted immediately after poly-Si gate deposition. While for the p^+-gated p-MOS devices, gate and source/drain (S/D) implants were performed simultaneously by either BF_2^+ or B^+ (both with a dose of 2.5×10^{15} cm^{-2}) implantation. The post-S/D implant thermal treatments were carefully controlled to ensure that boron penetration was effectively suppressed in our samples.

[z] E-mail: hclin@ndl.gov.tw

Details of the structural parameters and process conditions for devices characterized in this study are summarized in Table I. In this work, we focus our attention on the NBTI characteristics of devices with different gate-doping types and species as well as post-metal annealing treatments. To evaluate degradations due to the bias-temperature stress, devices were subjected to stress conditions with negative gate bias (−3.5-−4.5 V) at 150°C. During stressing, drain/source and substrate were all grounded, as shown in Fig. 1. To evaluate the role of hydrogen atoms in the NBTI, the post-metal anneal (PMA) performed in a forming gas was intentionally skipped for some samples. Device parameters, including threshold voltage, subthreshold swing (SS), transconductance, and gate leakage current, were measured using an HP4156A parameter analyzer both before and after the BT stressing.

Results and Discussion

Effects of poly-Si gate doping type.—Threshold voltage shift as a function of bias temperature (BT) stressing time for samples 1 and 2 is shown in Fig. 2. It can be seen that Vth degradation obeys the power law[7,8]

$$\Delta Vth(t) = At^{b} \quad [1]$$

The extracted A and b values for the measured data as well as the initial gate current under the stress conditions, are summarized in Table II. The extracted b values are around 0.25-0.30 for all devices. These results are consistent with previous reports,[7] implying that the incorporated As^+ ion in the poly-Si gate would not effectively change the mechanisms of NBTI. Note that the initial stress current for sample 1 (n^+-gated) is about an order of magnitude higher than that of sample 2 (p^+-gated). From Fig. 2, it can be seen that the n^+-gated device shows a much smaller Vth shift under BTS than its p^+-gated counterpart, albeit with a similar b value. Figure 3 compares the pre-BTS gate leakage current for fresh samples 1 and 2. For a given gate voltage (V_g), sample 1 (*i.e.*, n^+-gated) exhibits a higher leakage current. This could be explained by the band diagrams shown in Fig. 4. For sample 1, the leakage current is dominated by the electron Fowler-Nordheim (F-N) tunneling from the n^+-gate (Fig. 4b), which has a much higher probability than either the gate valence-band electron direct-tunneling or the substrate hole-tunneling process for sample 2 (Fig. 4a).[9] Though the higher electron injection flux from the n^+-gate would result in almost the same time dependence (Table I), the Vth shift is much smaller than that of the p^+-gated device, indicating that the electron tunneling current plays only a minor role in the NBTI degradation. Also note in Fig. 4, the oxide field is stronger for the p^+-gated device. This also supports the argument that the oxide field plays a key role in NBTI degradation.[10]

Downloaded on 2014-04-27 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

Table I. Major structural parameters and process conditions for the test samples.

Sample no.	1	2	3	4	5
L_{gate}			0.8 μm		
W_{gate}			10 μm		
T_{ox}			2.9-3.1 nm		
Gate doping type	n^+	p^+	p^+	p^+	p^+
Deep S/D implant (2.5×10^{15} cm^{-2})	BF_2^+	BF_2^+	B^+	B^+	BF_2^+
S/D extension (5×10^{14} cm^{-2})	BF_2^+	BF_2^+	BF_2^+	B^+	BF_2^+
PMA	Yes	Yes	Yes	Yes	No

Table II. Fitting parameters for Eq. 1 and the initial stress gate leakage for all samples.

Sample splits and BTS condition	*Vth* of fresh devices (V)	*A*	Exponent *b*	J^a (A/cm^2)
Sample 1, −4 V	1.629	1.32	0.28	369nm
Sample 1, −4.5 V	1.622	3.05	0.30	3.31μm
Sample 2, −4 V	0.615	5.56	0.27	46.8 nm
Sample 2, −4.5 V	0.616	9.89	0.28	876nm
Sample 3, −4 V	0.636	12.32	0.24	40.3 nm
Sample 4, −4 V	0.623	11.84	0.25	42.6 nm
Sample 5, −4 V	0.639	4.87	0.26	43.2 nm

[a] Initial gate current under BT stressing.

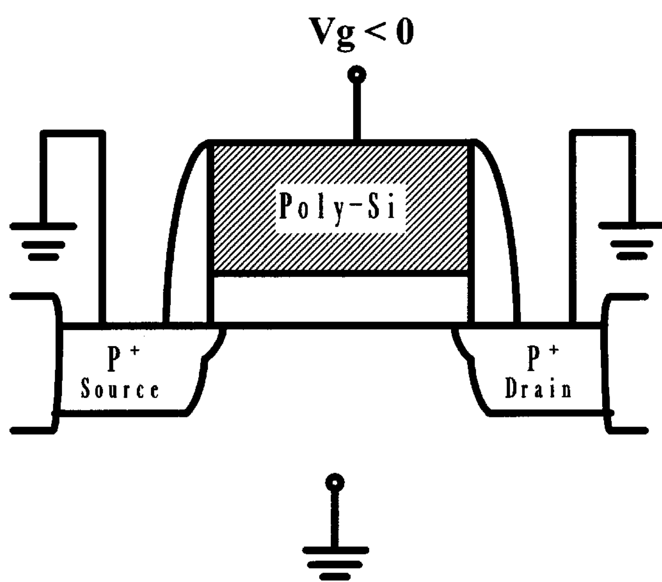


Figure 1. Configuration for NBTI stressing.

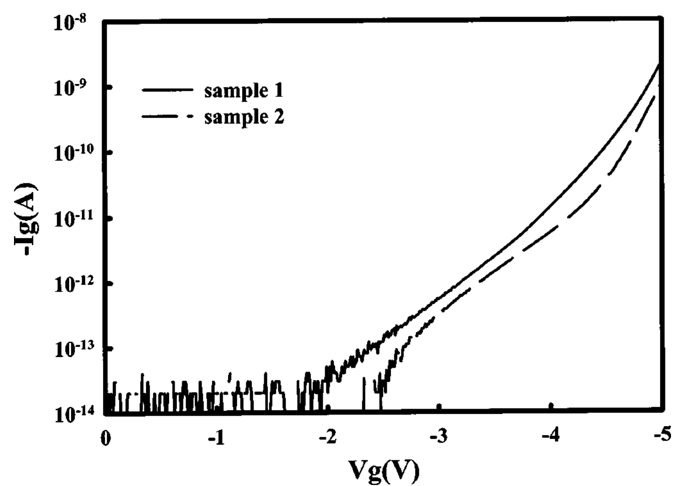


Figure 3. Gate leakage current *vs.* gate bias for samples 1 and 2.

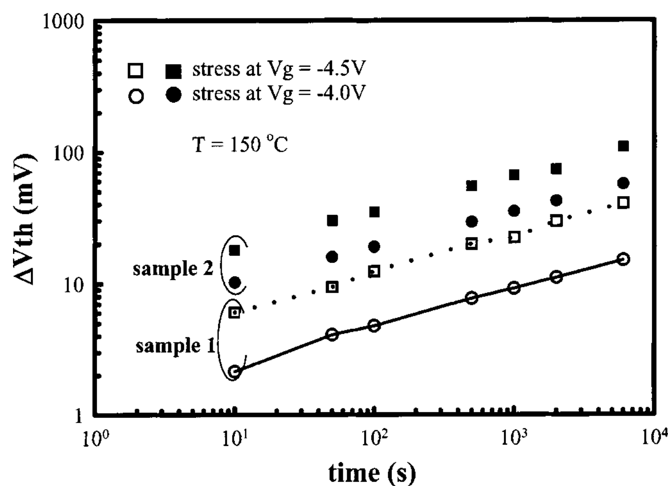


Figure 2. Threshold voltage shift as a function of BT stressing time for devices with different gate doping types (solid line for n^+-gated sample 1 and dashed line for p^+-gated sample 2).

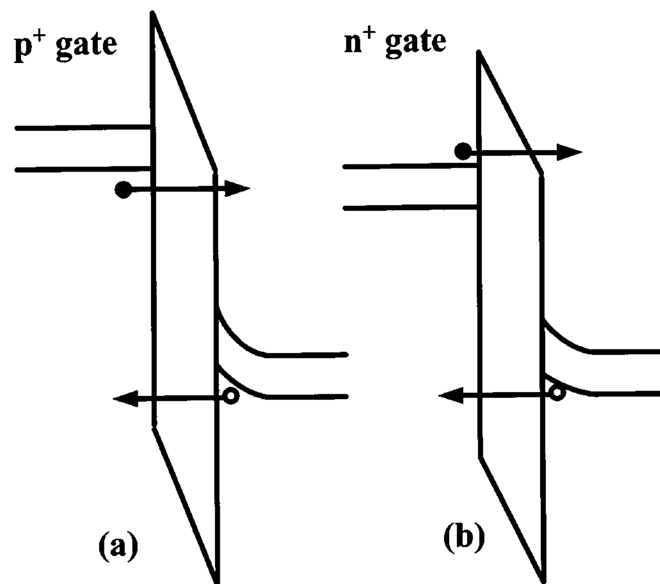


Figure 4. Band diagrams of (a) p^+-gated (sample 2) and (b) n^+-gated (sample 1) p-MOSFETs with n-substrate, biased at $Vg = -4$ V.

Downloaded on 2014-04-27 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

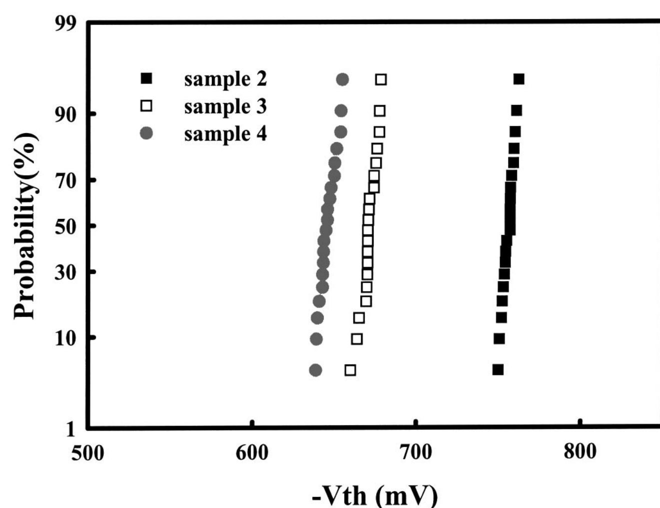


Figure 5. Cumulative probability of the threshold voltages (Vth) for sample 2 (with highest fluorine incorporation, ■), sample 3 (with intermediate fluorine incorporation, □), and sample 4 (without any deliberate fluorine incorporation, ●).

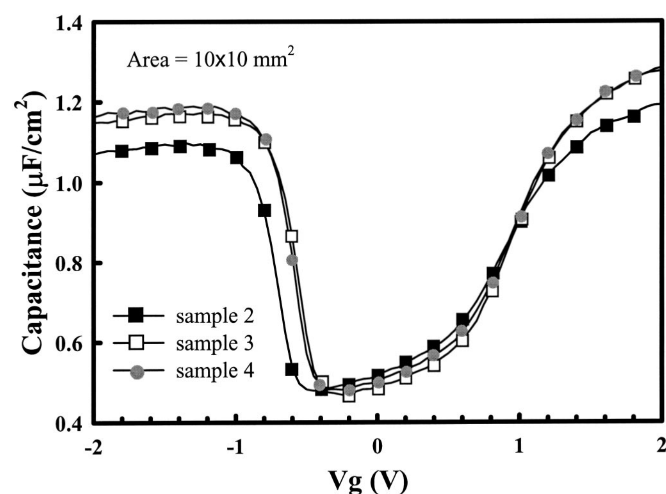


Figure 6. High frequency C-V characteristics for sample 2 (with highest fluorine incorporation, ■), sample 3 (with intermediate fluorine incorporation, □), and sample 4 (without any deliberate fluorine incorporation, ●).

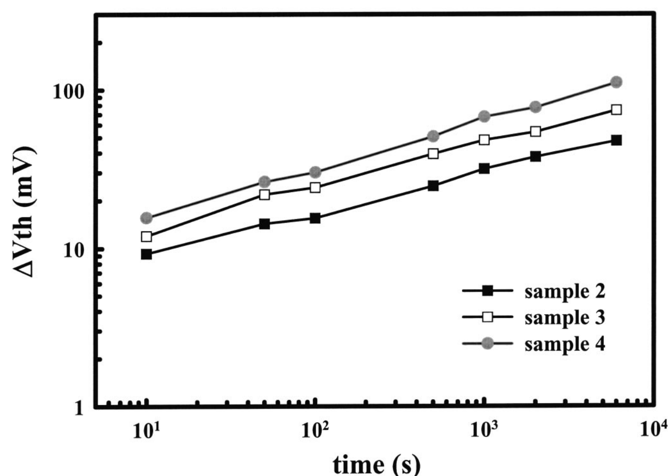
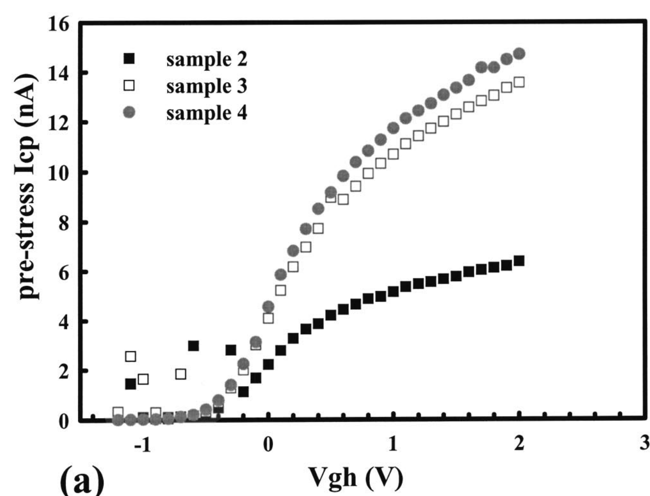


Figure 7. Vth shift as a function of stress time, stressed at 150°C, $Vg = -4$ V.



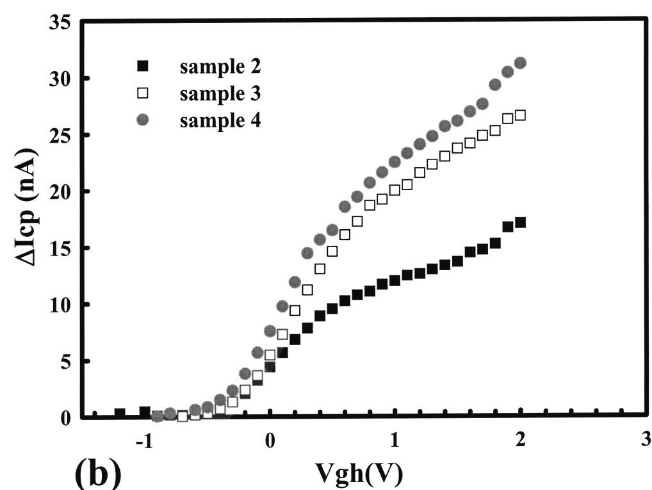


Figure 8. (a) Fresh and (b) post-BTS charge-pumping currents for sample 2 (with highest fluorine incorporation, ■), sample 3 (with intermediate fluorine incorporation, □), and sample 4 (without any deliberate fluorine incorporation, ●).

Effects of fluorine incorporation.—In this study, fluorine was incorporated during the deep and/or S/D extension implant steps (Table I). Various amounts of fluorine incorporation could thus be obtained, and the resultant effects on the device performance were explored. Figure 5 shows the cumulative probability of the threshold voltages (Vth) for the fabricated devices. The tight Vth distribution in Fig. 5 indicates that there is no noticeable boron penetration effect induced in these devices. Figure 6 shows the prestress C-V curves. Equivalent oxide thickness (EOT) of the samples is extracted using a simulator that takes quantum mechanical and poly-depletion effects into consideration. An EOT of around 2.9 nm is obtained for the devices without or with only a small amount (*i.e.*, through a medium dose BF_2 extension implant) of fluorine incorporation. EOT

Table III. Extracted pre- and post-BTS interface state density (*Dit*) for samples with different S/D implant conditions.

Sample splits	*Dit* (pre-BTS)	ΔDit (post-BTS)
Sample 2	4.03×10^{10} (1/eV cm^2)	9.34×10^{10} (1/eV cm^2)
Sample 3	8.35×10^{10} (1/eV cm^2)	1.56×10^{11} (1/eV cm^2)
Sample 4	9.16×10^{10} (1/eV cm^2)	1.76×10^{11} (1/eV cm^2)

Downloaded on 2014-04-27 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

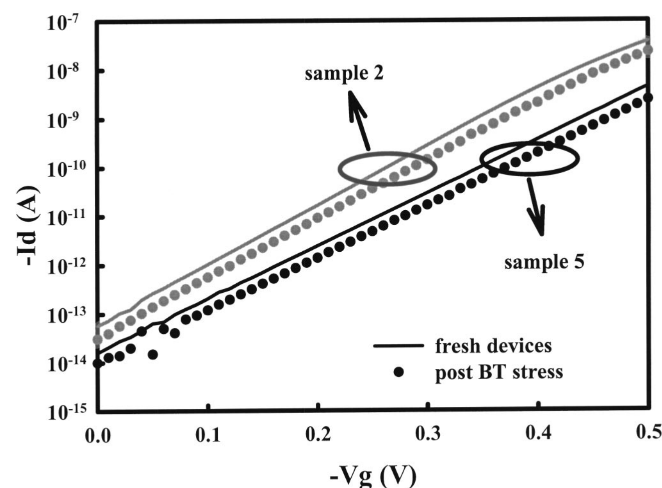


Figure 9. Pre- and post-BTS subthreshold characteristics for sample 2 (with PMA) and sample 5 (without PMA).

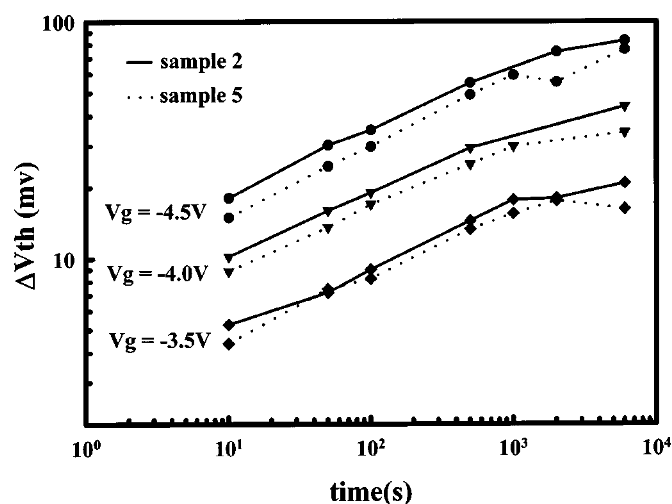


Figure 10. *Vth* shift *vs.* BT stress time for sample 2 (with PMA) and sample 5 (without PMA).

increases to 3.1 nm when a high-dose BF_2^+ implant is performed. The apparent oxide thickness increase with high fluorine incorporation is consistent with previous reports.[10,11]

In Fig. 7, the *Vth* shift as a function of stress time is shown for devices with different S/D implant conditions (*i.e.*, samples 2, 3, and 4, respectively, see Table I). As can be seen in this figure, the NBTI could be reduced effectively by increasing fluorine incorporation, although the slope is almost identical among all splits. To gain insight into the effect of fluorine incorporation at the Si/SiO_2 interface, a charge-pumping technique was also performed for detail analysis. Figure 8a shows the results for fresh devices. All transistors are with a width-length of 5 μm/0.8 μm. The results indicate that the addition of fluorine reduces the interface states. Figure 8b shows charge-pumping current increments after BT stressing. The interface state density extracted from the results shown in Fig. 8a and 8b is summarized in Table III. Again, charge-pumping current decreases with increasing fluorine incorporation, and the sample with the highest fluorine incorporation (*i.e.*, sample 2 that received fluorine incorporation both from BF_2^+ S/D extension and deep S/D BF_2^+ implants) indeed shows the best performance. The ratios of the increased *Dit* among the splits are close to those of the *Vth* shift. This result indicates that the incorporated F atoms, which could replace hydrogen-related sites at the Si/SiO_2 interface, tend to passivate the interface dangling bonds. Since the Si—F bonding energy (5.73 eV) is higher than that of Si—H bond (3.18 eV),[12] proper fluorine incorporation at the Si/SiO_2 interface could improve NBTI immunity.

It should be noted that fluorine incorporation has been previously reported to cause enhanced boron penetration, which in turn could enhance the NBTI.[2,7] Since the thermal budget is carefully controlled to prevent the occurrence of boron penetration, proper fluorine incorporation actually strengthens the interface[10,13] and thus improves the NBTI immunity in our study.

Effects of PMA.—PMA in a forming gas was widely used for passivation of the interface dangling bonds. However, the passivated Si—H bonds tend to break more easily during subsequent NBTI stressing. The released hydrogen atoms could diffuse into the oxide bulk, and cause a threshold voltage shift.[1] To understand the effects of passivated Si—H bonds at SiO_2/Si interface during BT stress, NBTI immunity of devices both with (*i.e.*, sample 2) and without (*i.e.*, sample 5) PMA treatments were measured and compared. Figure 9 shows the subthreshold characteristics of the test samples. The pre- and poststress subthreshold swings for both devices are summarized in Table IV. Although the device without PMA shows poorer initial subthreshold characteristics, it depicts a smaller subthreshold swing degradation (about 1.66%) during BTS, compared to the device with PMA treatment (2.75%). This is ascribed to more Si—H bond breaking during BTS for the PMA-treated device. Figure 10 shows the *Vth* shift as a function of BTS stress time. Indeed the device with PMA shows more severe NBTI degradation. These results unambiguously highlight the important role of hydrogen in the NBTI degradation process.

Table IV. Pre- and post-BTS SS for samples with and without post-metal anneal.

Sample splits	Sample 2 (with PMA)	Sample 5 (wt % PMA)
Before BTS	81.21 mV/dec	91.14 mV/dec
After BTS	83.44 mV/dec	92.65 mV/dec

Conclusions

The effects of gate doping species and thermal treatments on negative-bias-temperature instability (NBTI) of p-MOSFETs were conducted. Devices with n^+-poly-Si gate exhibit less NBTI degradation, compared to their p^+-gated counterparts. Our analysis indicates that the electron FN tunneling current during stressing plays only a minor role in the NBTI degradation. By contrast, the oxide field strength is critical for the NBTI degradation process. Our results also indicate that fluorine incorporation by a S/D implant step is beneficial for improving the NBTI immunity. The incorporated fluorine could replace hydrogen-related sites at the SiO_2/Si interface, which could act as precursors for the generation of interface traps responsible for NBTI degradation.

The effects of PMA on device characteristics were also investigated. We found that, although the incorporated hydrogen atoms could reduce the pre-BTS interface states, the passivated hydrogen could be released during BTS, causing aggravated NBTI degradation.

Acknowledgments

The authors thank the staff at National Nano Device Laboratories for their assistance in device fabrication. This work was supported in part by the National Science Council of the Republic of China under contract no. NSC90-2215-E009-079.

National Nano Device Laboratories assisted in meeting the publication costs of this article.

Downloaded on 2014-04-27 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

References

1. T. Yamamoto, K. Uwasawa, and T. Mogami, *IEEE Trans. Electron Devices,* **46**, 921 (1999).
2. N. Kimizuka, T. Yamamoto, T. Mogami, K. Yamaguchi, K. Imai, and T. Horiuchi, in *Proceedings of Symposium on VLSI Technology*, 73 (1999).
3. N. Kimizuka, K. Yamaguchi, K. Imai, T. Iizuka, C. T. Liu, R. C. Keller, and T. Horiuchi, in *Proceedings of Symposium on VLSI Technology*, 92 (2000).
4. A. T. Krishnan, V. Reddy, and S. Krishnan, *Tech. Dig. - Int. Electron Devices Meet.,* **2001**, 865.
5. D. Y. Lee, H. C. Lin, M. F. Wang, M. Y. Tsai, T. Y. Huang, and T. Wang, in *Proceedings of Solid State Devices and Materials*, 204 (2001).
6. F. E. Pagaduan, J. K. J. Lee, V. Vedagarbha, K. Lui, M. J. Hart, D. Gitlin, T. Takaso, S. Kamiyama, and K. Nakayama, in *Proceedings of the 39th IEEE Annual International Reliability Physics Symposium*, 315 (2001).
7. C. H. Liu, M. T. Lee, C. Y. Lin, J. Chen, K. Schruefer, J. Brighten, N. Rovedo, T. B. Hook, M. V. Khare, S. F. Huang, C. Wann, T. C. Chen, and T. H. Ning, *Tech. Dig. - Int. Electron Devices Meet.,* **2001**, 861.
8. K. O. Jeppson and C. M. Svensson, *J. Appl. Phys.,* **48**, 2004 (1977).
9. Y. Shi, T. P. Ma, S. Prasad, and S. Dhanda, *IEEE Trans. Electron Devices,* **45**, 2355 (1998).
10. T. B. Hook, E. Adler, F. Guarin, J. Lukaitis, N. Rovedo, and K. Schruefer, *IEEE Trans. Electron Devices,* **48**, 1346 (2001).
11. P. Wright and K. C. Saraswat, *IEEE Trans. Electron Devices,* **36**, 879 (1989).
12. C. C. Chen, H. C. Lin, C. Y. Chang, C. C. Huang, C. H. Chien, T. Y. Huang, and M. S. Liang, in *Proceedings of Symposium on Plasma Process Induced Damage*, 121 (2000).
13. K. A. Keiko, W. Kikuo, U. Jiro, and M. Eiichi, *Appl. Phys. Lett.,* **81**, 4362 (2002).

Downloaded on 2014-04-27 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).