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Thin Solid Films 447–448 (2004) 524–530
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# CMP of ultra low-*k* material porous-polysilazane (PPSZ) for interconnect applications

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**Abstract**

In this article, we investigated the impact of chemical mechanical polishing (CMP) on an ultra low dielectric constant (ultra low-*k*) material Porous-Polysilazane (PPSZ) with slurries of metal polishing during interconnect manufacture process. Since the CMP processing of metals such as TaN and Cu are inevitable steps for interconnect fabrication, we have utilized two types of slurries (marked as TaN and Cu slurries) to evaluate their effects on the dielectric properties of PPSZ films. Electrical and material analyses have shown surface planarity and dielectric properties of PPSZ films will not be degraded during these metal CMP processes. This indicates that the ultra low-*k* PPSZ films are promising for inter-level dielectric (ILD) applications in ultra large-scale integrated circuits (ULSI) technology.


*Keywords:* Chemical mechanical polishing; Ultra low-*k*; Porous-polysilazane films; Copper

## 1. Introduction

Shrinking device dimensions associated with ultra large scale integrated circuits is highly effective in achieving high speed performance and in increasing yields at lower cost per chip. In order to assure the performance of the high-speed circuits, continuous efforts have been devoted for incorporating copper or low-dielectric constant (low-*k*) materials into multilevel interconnections for reducing the major part of circuit delay, cross talk, and power consumption [1–3]. For integrating Cu and low-*k* materials into integrated circuits (ICs), the damascene technique [4,5] (shown in Fig. 1) with chemical mechanical polishing (CMP) [6,7] is the most suitable approach towards using copper in a multilevel metallization scheme. Furthermore, it is reported that Cu easily diffuses into most low-*k* materials during interconnect manufacture processes and reliability testing [8,9]. Therefore, the barrier metal such as TaN has been extensively used between Cu and low-*k* materials to protect Cu from diffusing into low-*k* materials. The polishing processes, for removing excess copper or TaN on damascene structures and associated with a resultant flat surface [10,11] is crucial for building-up multilevel interconnects scheme. Although a lot of studies have been focused on the planariability and topography of multilevel interconnection after CMP process [12–15], little attention has been paid to investigate the dielectric properties of low-*k* materials after metal CMP process, especially for the influence of CMP slurries. In this study, an ultra low-*k* material ($k \sim 2.2$), which is Porous-Polysilazane (PPSZ) available form Clariant Inc in Japan, is used to investigate if it would be compatible with CMP process during Cu damascene interconnect manufacture. Based on electrical and material analyses, this study will give to a better understanding of PPSZ materials for applications system of ICs.

## 2. Experimental procedure

The substrates used in this study were 150 mm p-type (11–25 Ω-cm) single crystal silicon wafers with

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doi:10.1016/j.tsf.2003.07.028

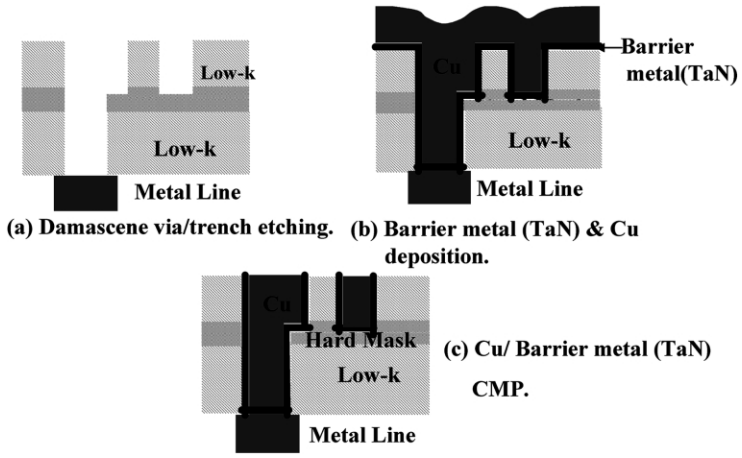



Fig. 1. Typical process flow of Cu damascene architecture integrated with low-*k* material. Step (a) low-*k*/hard mask/low-*k* were deposited sequentially, and then the via and trench were formed by lithography and etching process. Step (b) Barrier metal and Cu was deposited in via and trench in turn. Step (c) Finally, Cu and TaN CMP were utilized to manufacture Cu damascene structure.

(100) orientation. Before film deposition, they were boiled in $H_2SO_4+H_2O_2$ solution and heated to 120 °C for 20 min to remove particles on the surfaces. These wafers were spin-coated with ultra low-*k* Porous-Polysilazane (PPSZ) solution at a spin speed of 2000 rev./min for 30 s on a model 100CB spin coater. Then, it was followed by baking steps, sequentially on hot-plates at 150 and 280 °C for 3 min. The coated wafers were then followed by a hydration treatment. They were left in cleanroom for 48 h. For the polymer-structure to be transformed to porous methyl-silsesquioxane through hydrolysis and condensation process as shown in the following [16,17]:

*Hydrolysis*:

$$\equiv \text{Si-NH-Si} \equiv + H_2O \rightarrow \equiv \text{Si-NH}_2 \equiv + \text{HO} - \text{Si} \equiv$$

$$\equiv \text{Si-NH}_2 + H_2O \rightarrow \equiv \text{Si-OH} + NH_3$$

*Condensation*:

$$\equiv \text{Si-OH} + \text{HO-Si} \equiv \rightarrow \equiv \text{Si} - \text{O} - \text{Si} \equiv + H_2O$$

Afterward, the resulted wafers were cured in a quartz furnace at 400 °C for 30 min under $N_2$ ambient. The final PPSZ films (called as-cured PPSZ) were formed with a thickness of 400 nm (the final structure is shown in Fig. 2). The thickness of the deposited PPSZ films was measured at n and k 1200 analyzer, manufactured by the n and k company, by comparing the theoretical reflectance with the actual measurement of broad-band reflectance. After film formation, the CMP process was applied to the as-cured PPSZ films. The CMP experiment was carried out on an IPEC/Westech 372M CMP processor with a Rodel IC 1400 pad on the primary polishing plated and Rodel Politex Regular embossed pad on the final buffering plated. A Rodel R200-T3 carrier film was used to provide buffer between the

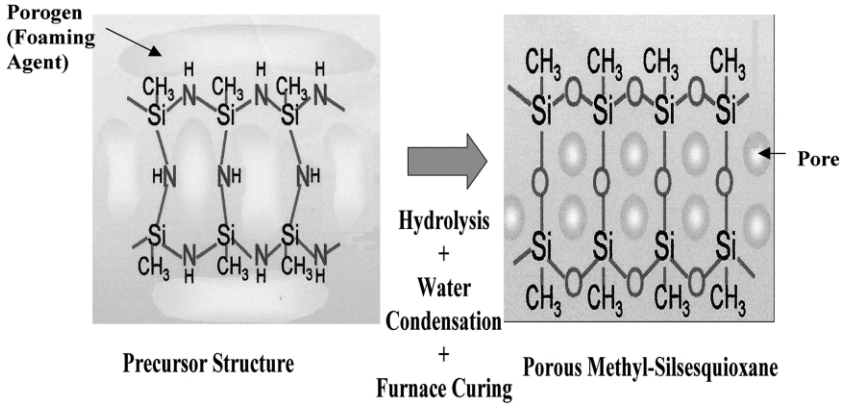



Fig. 2. Method of precursor structure transfer to final porous-polysilazane (PPSZ) structure.

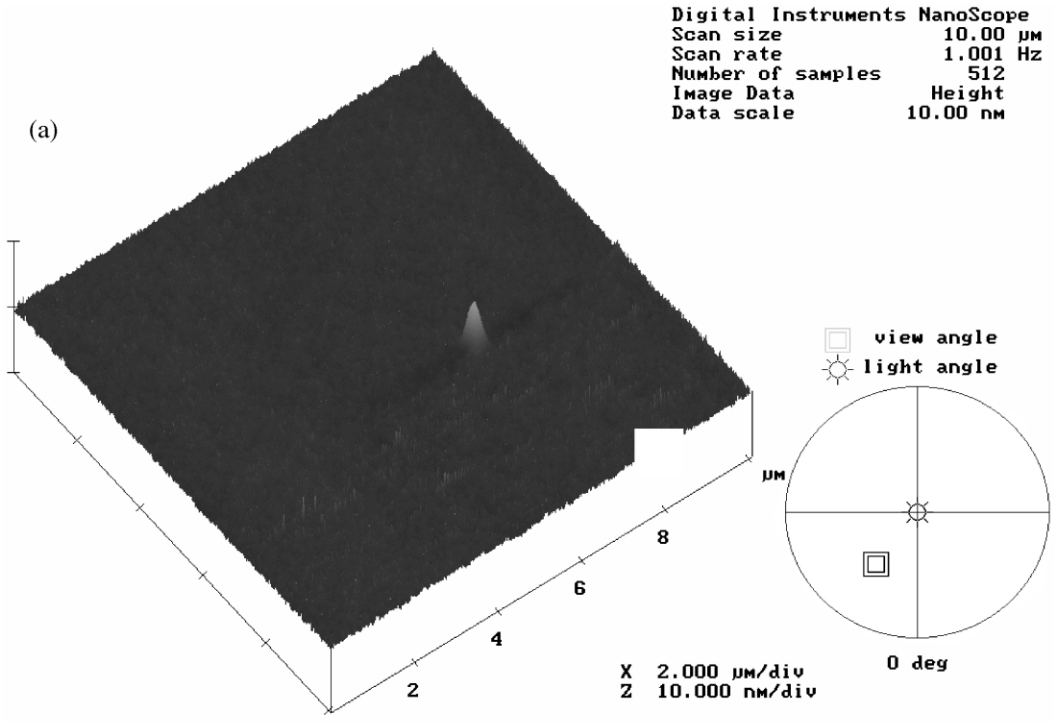
Table 1
Polished parameters of ultra low-*k* PPSZ in IPEC/Weatech 372M CMP polisher

| Polisher: *IPEC372M* | 1st step (only) | |
|---|---|---|
| | Phase 1 | Phase 2 |
| Platen/Carrier speed | 50/60 rev./min | 30/40 rev./min |
| Down force | 3.0 psi | 1.5 psi |
| Back pressure | 2.0 psi | 0 |
| Slurry flow rate | 150 ml/cm | Rinse |
| Polishing pad | Rodel politex regular E.™ | |
| Carrier film | Rodel R200-T3™ | |
| Slurry formation | Cu slurry<br>2 vol.% $HNO_3$,<br>$5\times10^{-2}$ M citric acid,<br>3 wt.% $Al_2O_3$ (0.1 μm) | TaN slurry<br>10 wt.% colloidal silica,<br>10 vol.% $H_2O_2$,<br>pH 8.5 |

carrier and wafer. The wafer was mounted on a template assembly for a single 6 in. wafer during the polishing experiment. In this experiment, two types of slurries were implemented separately to investigate the influence on the characteristics of ultra low-*k* PPSZ films. One was the slurry typically used in polishing Cu metal, provided from National Nano Device Laboratory. This slurry consists of 2 vol.% $HNO_3$, $5\times10^{-2}$ citric acid, and 3 wt.% $Al_2O_3$ (0.1 μm), which was marked as Cu slurry. The pH value of Cu-slurry is 0.56. Besides, we investigated another type of colloidal silicate slurry (marked as TaN slurry), which included 10 wt.% colloidal silica and 10 vol.% $H_2O_2$ in DI water liquid. Its pH value is 8.5. In addition, the polishing parameters, such as pad, down force, back pressure, platen and carrier rotation speeds, and slurry flow rate are shown on Table 1 for these two slurries. The structure properties of the PPSZ films were studied using Fourier transform infrared spectroscopy (FTIR). The surface morphologies of the polished films were investigated by atomic force microscopy (AFM). Electrical characteristics of polished PPSZ films were performed on the metal-insulator-semiconductor (MIS) capacitor with metallic copper deposition as the top electrode and aluminum deposition as backside electrode. Leakage current–voltage ($I-V$) and capacitance–voltage ($C-V$) characteristics were also used to analyze the leakage current behaviors and to measure the dielectric constants of polished PPSZ films, respectively. During the operation of IC, it works at higher temperature and bias than its off state. In this situation, the copper may drift into the dielectric much easily. Therefore, high bias and temperature stress (BTS) was performed to evaluate the reliability under IC operation condition. In this work, BTS was performed by applying an electric field at 2 MV/cm on the MIS capacitor at 150 °C for 1000 s. Before BTS testing, the leakage current of polished PPSZ films was measured at room temperature at 150 °C. After BTS testing, the leakage current was measured again at 150 °C and room temperature sequentially.

## 3. Results and discussions

In order to obtain global planarization of multilevel interconnection and desirable pattern, the detection of end point of metal CMP must be concerned in the Cu damascene process. However, it is found that the removal rate of ultra low-*k* PPSZ film with TaN slurry is 17 nm/min, which is lower (68.1 nm/min) than that of polishing TaN with the same slurry. On the other hand, the removal rate of ultra low-*k* PPSZ with Cu slurry is only 3 nm/min, which is much lower than that of polishing Cu with the same slurry. The results indicate that the difference in removal rate of copper or tantalum with respect to PPSZ is high and can distinguish the detection of end point much easily. In addition, the dielectric integrity and surface topography of ultra low-*k* PPSZ films after metal CMP process has to be remained at acceptable region to meet requires of multilevel interconnection. AFM images of PPSZ surface after CMP process with TaN and Cu slurries are shown in Fig. 3a and b, respectively. It indicates that there are smooth PPSZ surface after CMP polishing no matter with TaN or Cu slurries, the roughness (Ra) of PPSZ films is approximately 0.189 and 0.253 nm after TaN and Cu slurries polishing, respectively. This result indicates that the removal rate of copper and tantalum with respect to low-*k* PPSZ film is high and can obtain planarization surface after TaN or Cu CMP process. The FTIR spectra of post-CMP PPSZ with TaN or Cu slurries are given in Fig. 4. It is revealed that the Si–C and C–H bonds intensity of polished PPSZ films are still remanded at high level after metal CMP process. This provides evidence that the chemical structure of PPSZ film would not damage after CMP procedure with these polished slurries. Fig. 5a and b show the leakage current and



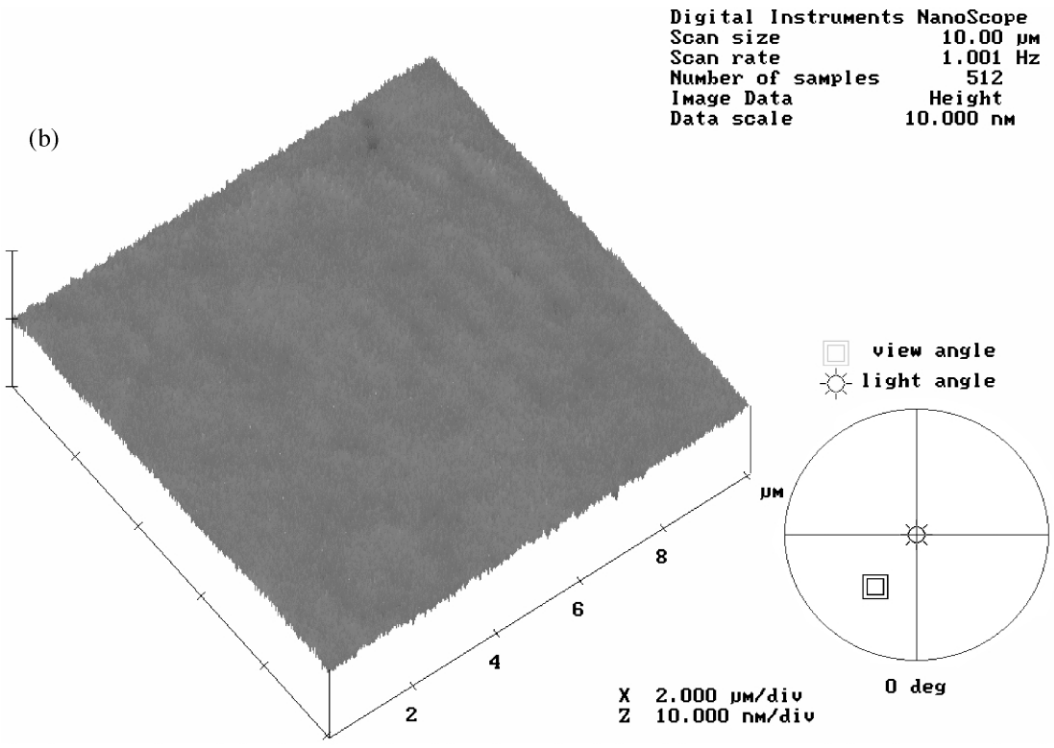




Fig. 3. AFM image of polished PPSZ surface (a) with TaN Slurry; (b) with Cu slurry.

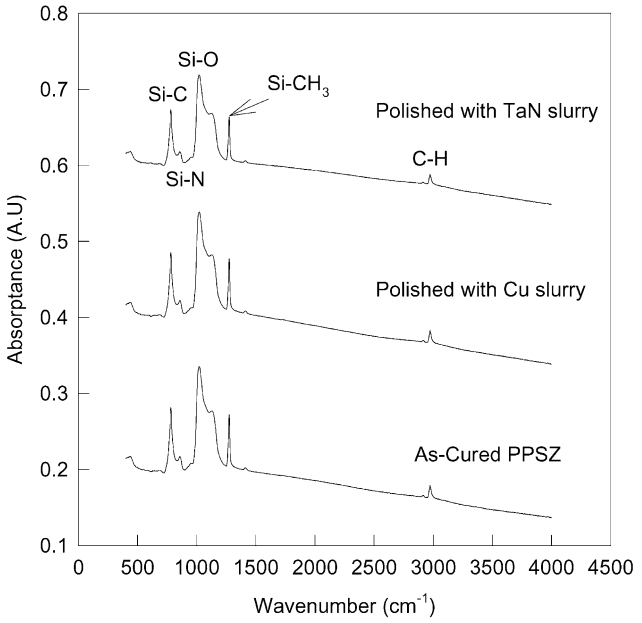



Fig. 4. FTIR spectra of PPSZ films polished with TaN or Cu slurries

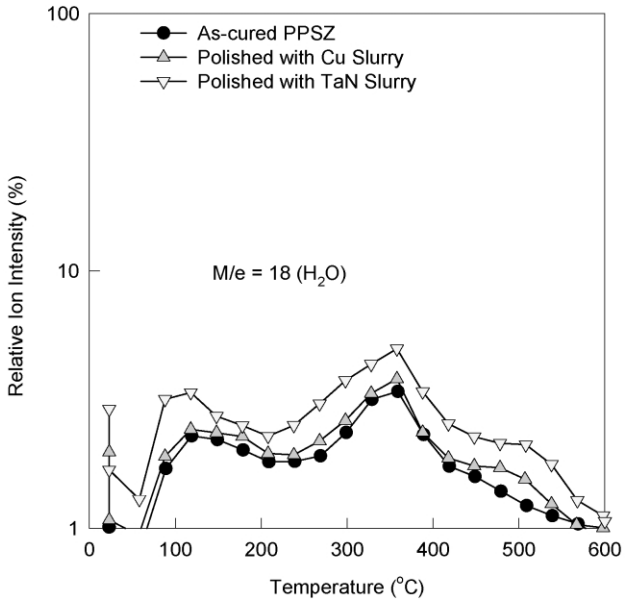



Fig. 6. The TDS moisture desorption spectra of PPSZ polished with TaN or Cu slurries.

dielectric constant of PPSZ after the CMP process with TaN or Cu slurries. The leakage current of post-CMP PPSZ is similar to as-cured PPSZ film regardless of PPSZ films polished with TaN or Cu slurries. The dielectric constants of post-CMP PPSZ films slightly increases from 2.25 of as-cured PPSZ film to the region of 2.3 to 2.4 as well, as shown in Fig. 5b. However, it still accords with the requirement of low-*k* materials. It appears that the electrical properties of PPSZ cannot be degraded during CMP process with TaN or Cu slurries. Fig. 6 reveals the tendency of moisture desorption during the raised temperature period in temperature desorption system. The concentrations of moisture desorption of PPSZ, polished with TaN or Cu slurries are silimar to that of as-cured PPSZ films. This is believed that the film characteristics are not changed after CMP process. This result is consistent with the electrical properties of PPSZ films polished by metal polishing slurries. More-

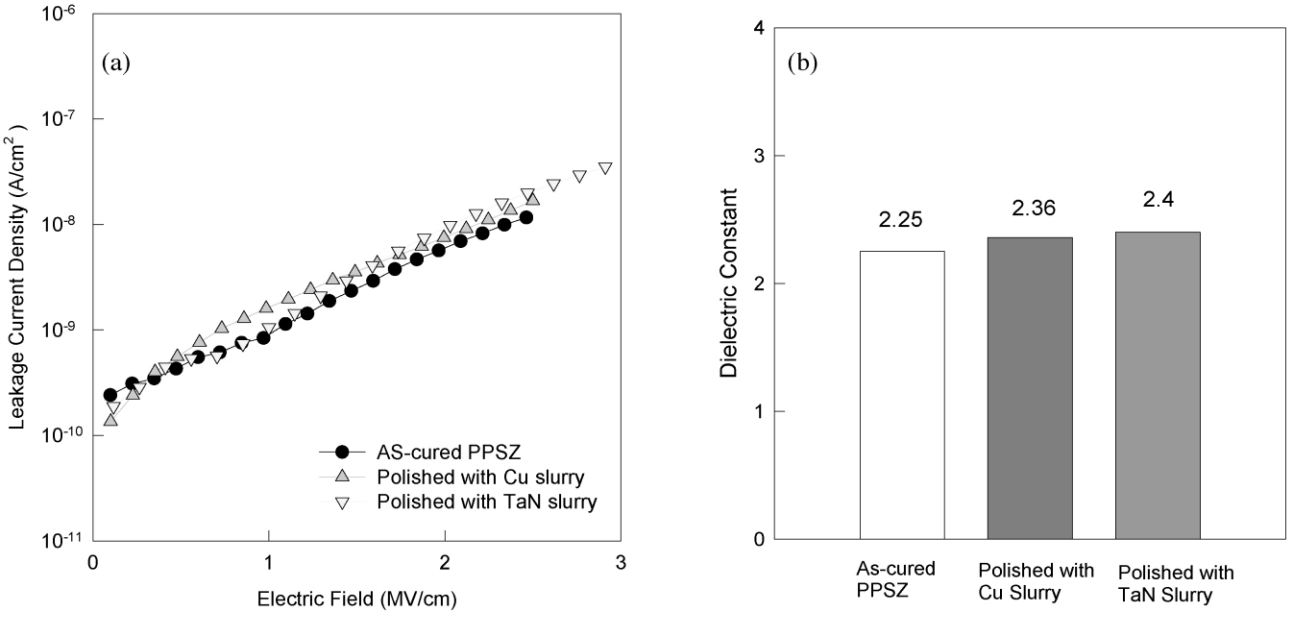



Fig. 5. Dielectric properties of PPSZ films polished with TaN or Cu slurries: (a) Leakage current density of post-CMP PPSZ films as a function of electric field; (b) dielectric constants of post-CMP PPSZ films.

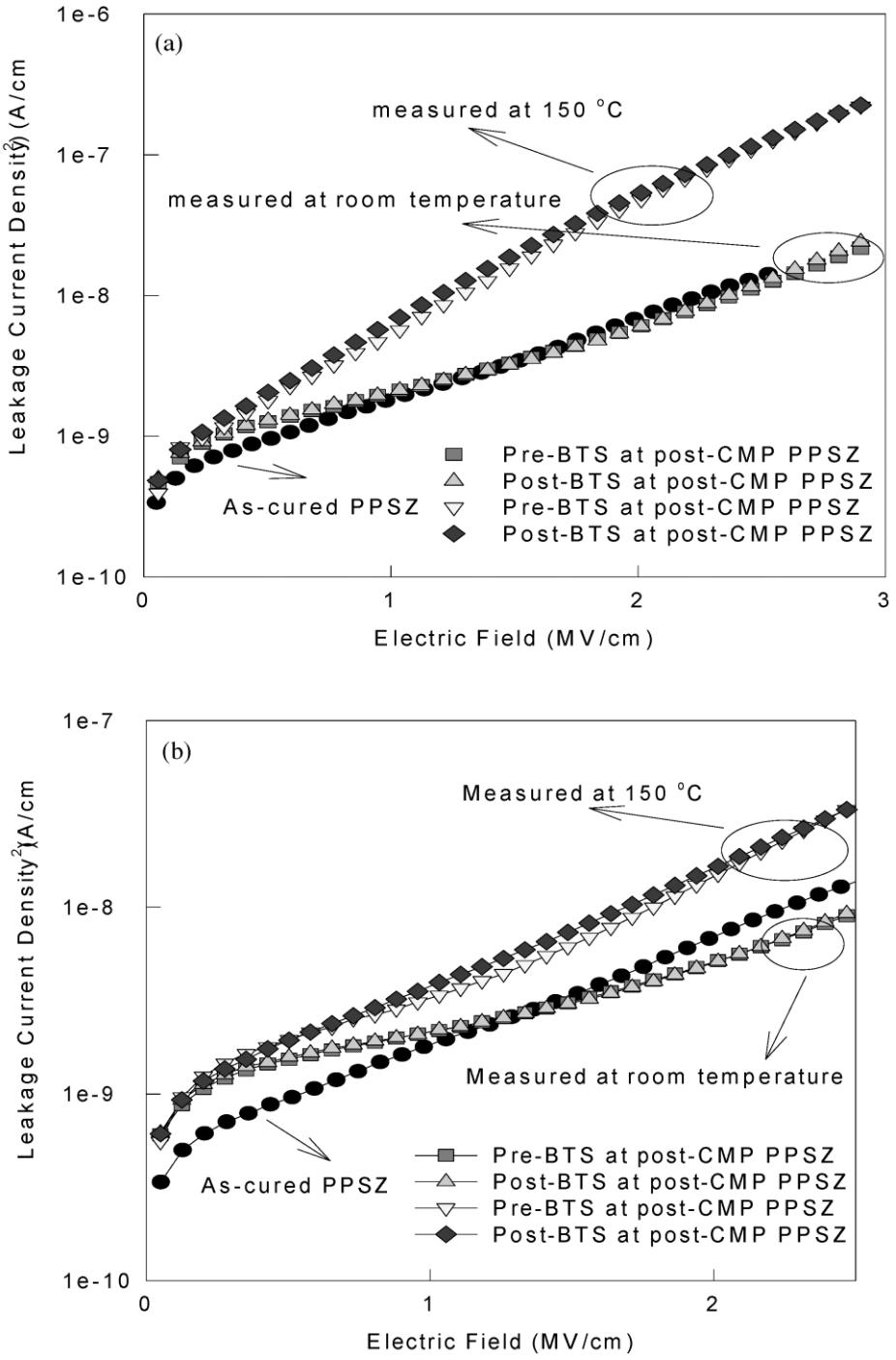



Fig. 7. Leakage current density of Cu-electrode polished PPSZ film after 2 Mv/cm at 150 °C for 1000 sec BTS stress measured at room temperature at 150 °C (a) with TaN slurry (b) with Cu slurry.

over, in order to investigate the reliability of polished PPSZ with copper, the higher temperature measurement and BTS tests were conducted to evaluate the reliability of post-CMP PPSZ. Fig. 7a and b show the leakage current density of these post-CMP PPSZ films before and after BTS test at high and low temperature. The leakage current densities of the post-CMP PPSZ with TaN or Cu slurries donot arise at all after BTS stress (versus pre-BTS stressing post-CMP PPSZ films). With either TaN or Cu slurry, the leakage current of post stressed PPSZ is really close to that of pre-stressing ones and even electrical measurements were implemented at high temperature. This implies that the electrical reliability of PPSZ can be maintained even after metal

CMP process. As a result, the low-*k* PPSZ films after the CMP processes with Cu or Ta slurries will have good resistance to copper drift at high field and temperature operation conditions. These foregoing results suggest that the ultra low-*k* PPSZ film has a lot of potential for application in next generation of IC manufacture.

## 4. Conclusion

The CMP of organic ultra low-*k* ($k \sim 2.2$) PPSZ films with Ta and Cu slurries provided from national nano-device laboratory do not damage dielectric properties of PPSZ. The ultra low-*k* PPSZ materials have low polish rate as regard to the polish of Ta or Cu metal during damasence manufacture, and thus benefits the detection of end point of metal polish much easily. Moreover, the electrical properties of post-CMP PPSZ films can remain in low-*k* characteristics. Even after the high temperature and bias stress condition, the leakage currents do not arise and degrade at all. According to our results a reliable CMP process of damascene manufacture can be obtained by using our proposed TaN or Cu slurry. It is believed that the integration between PPSZ and Cu has promising potential in the next generation of ICs.

## Acknowledgments

This work was performed at National NanoDevice Laboratory and was supported by the Clariant Corporation in Tokyo, Japan, and the National Science Council of the Republic of China under Contract, Nos. NSC92-2112-M-110-020 and NSC92-2215-E-110-006.

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