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Copper surface protection with a completely enclosed copper structure for a damascene process

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Abstract

As integrated circuit manufacture moving to copper interconnection for the most advanced products, protection of copper (Cu) surfaces becomes a major challenge for the back-end-of-line manufacturing process. The damages on Cu, such as Cu corrosion and oxidation, are often observed on wafers when exposing bare Cu surface in the presence of moisture and/or acidic gases. Furthermore, the Cu oxide results in poor adhesion both at Cu/barrier layer and Cu/stop layer interfaces. In this work, a novel Cu dual damascene structure which completely encloses the Cu surface with a tantalum nitride layer is presented. This capping layer avoids the Cu corrosion and oxidation due to its ability to keep moisture and acid off and away from the Cu surface.
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Keywords: Cu; TaN capping process; Corrosion

1. Introduction

As the feature of semiconductor devices move toward narrower gate and reduced interconnect line pitch, a lower resistivity conductor material has to be adopted for the nano-scale-Si gate manufacturing in order to accommodate the faster speed performance requirements. Copper dual damascene interconnection technology is widely studied because it is one of the most promising technologies in reducing the contact resistance (RC) delay of LSIs [1,2]. However, since the device size is reduced, some new problems, such as metal corrosion, poor thermal stability, stress-induced migration and electromigration, emerge and have been observed in real products.

In the dual damascene structure using Cu interconnect, via and line trench is integrated and filled with the conductor after selective dielectric etch. The interconnect consists of a stack of Cu barrier, Cu seed and electro-plating Cu. After chemical mechanical polishing (CMP) process, the overburdens Cu above the surface of dielectric will be polished and the Cu fill remains in via and trench. Although the exposed Cu can immediately react with oxygen to form an oxide film, the film is porous and not of self-protective nature. Therefore, a capping material, such as SiN, is necessary to prevent the corrosion of Cu. Unfortunately, the Cu corrosion depends on the delay time from the CMP polish of Cu to deposition of protective layer. On the production line, the manufacture available time and efficiency are very hard to reach these stiff conditions. The prevention of Cu corrosion hence becomes the major challenge in production to improve the yield. On the other hand, the grains of Cu will enlarge during subsequent thermal processing [3,4]. For instance, the heating during dielectric material deposition would induce the Cu grain growth and generate the voids in Cu due to the surface area diminution of grain boundary. This will result in poor thermal stability of Cu film [5,6].

In Cu CMP process, dishing and erosion are the other problems for the Cu line thickness control. The occurrence of dishing and erosion depends on the line width and density [7,8]. Besides, the CMP parameters such as polishing down force, polish head rotation speed, polish pad elastic properties, slurry flow, polish time, etc., affect the dishing and erosion. Capping with a protective

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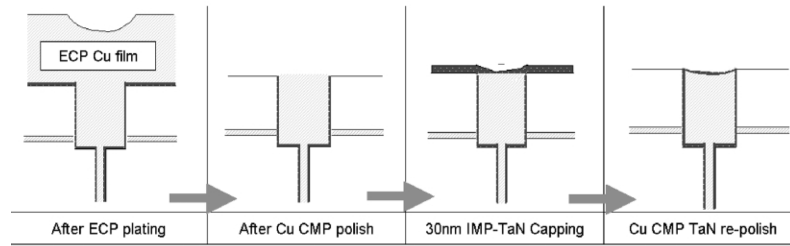

Fig. 1. TaN capping process procedure. 30 nm TaN was capped after Cu CMP and TaN re-polish remains a very thin TaN layer on Cu surface.

layer is the plausible way to avoid dishing and erosion phenomena so as to improve the Cu thermal stability.

This article investigated the dishing and erosion phenomena of Cu in CMP process. The tantalum nitride (TaN) capping on the top of Cu surface is proposed to protect the Cu from corrosion and oxidation. The thermal property of Cu is also examined using stress migration to evaluate its stability.

2. Experimental

A three-metal-level Cu interconnect was prepared for this experimental work. In metal 1, single damascene structure was applied. Dual damascene structure of via 1, 2 and metal 2, 3 was applied. The dual damascene structure adopts via first approach. Ionized metal plasma sputtering (IMP) of TaN was utilized for Cu barrier deposition and self-ionized plasma sputtering of Cu was applied for the seed layer deposition of electro-plating Cu. Overburden Cu was polish in a linear system. Two-step polish (copper and barrier metal were separated polish) system was carried out for Cu CMP process. An aluminum oxide abrasive system was selected in both of the two polishing steps. TaN capping process was carried out after CMP polishing [9,10]. The TaN of 30 nm in thickness was deposited and repolished away at the second step of Cu CMP shown in Fig. 1. Because of the selectivity effect, there remained a very thin TaN layer on the Cu surface. Dishing and erosion were measured by Tencor HRP-20 micro-profiler. The thermal stability of Cu, stress migration, was evaluated in a furnace at 180 °C for 170 h. The resistance of metal, R_s, was measured based on a serpentine test structure and the resistance of via, R_c, was measured based on via chain (totally 1798 via embedded with 2 μm in length and 1.5 μm in width) structure. A KLA-Tencor AIT-II was used to evaluate the defects induced by Cu corrosion.

3. Results and discussion

3.1. Pattern dependence of dishing and erosion phenomena

The influence of pattern density on dishing and erosion was characterized and the results are shown in Figs. 2 and 3, respectively. Fig. 2 illustrates that the Cu pad size and line width affect the dishing. As the Cu pad size increases to 4 times, the dishing increases to approximately 2 times. The erosion exhibits the same trend that it increases with the line width at a fixed oxide spacing of 120 μm, as shown in Fig. 3.

In Fig. 2, the dishing increases in a very fast rate at the small sizes of Cu pad area ranging from 60 to 150 μm^2. In small Cu pads, the oxide plays a very important role in anti-dishing. The higher the ratio of oxide area, the lesser the dishing observed. This is resulted from the high selectivity of oxide in Cu polishing module using the aluminum slurry system. The selectivity of different Cu CMP polishing module is shown in Table 1.

On the other hand, the percentage of Cu over polish will worsen the result. As the percentages of over polish increase, the total polish time increases. This, in turn, immerses the wafer in the slurry for longer times. The additional immersion time caused Cu corrosive by slurry chemical reaction. This explains why more over-polish cause higher degree of dishing.

For the Cu pads larger than 150 μm^2, the dishing increased at a nearly constant rate. In these cases, the CMP polish pad deformation dominated. Because the CMP polish pad is made of polyurethane that would be deformed during polishing and provide the CMP planarization. The limitation of polish pads deformation causes the constant increasing of dishing. As shown in Fig. 3, the erosion also increases at a constant rate. Fixed densities of Cu lines and oxide pitch (120 μm) are the major cause of this phenomenon. Because of the selectivity of Cu to oxide is approximately 200:1 shown in Table 1, the larger oxide area will reduce the erosion amount in small line width. The increase of erosion only depends on the Cu line width at fixed oxide pitch. Besides, the higher over-polish exhibited the same behavior, as observed in dishing experiments, that the slurry chemistry effect is again dominant.

3.2. TaN cap process for Cu corrosion prevention and thermal stability improvement

The dishing and erosion generated by Cu CMP process could be controlled by appropriate Cu to oxide

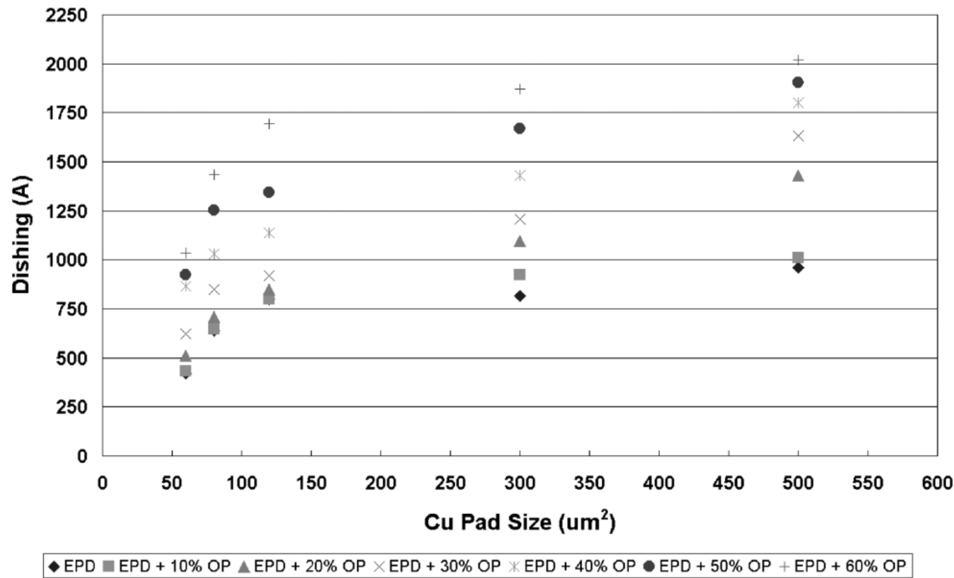

Fig. 2. The effect of Cu pad size and line width on dishing.

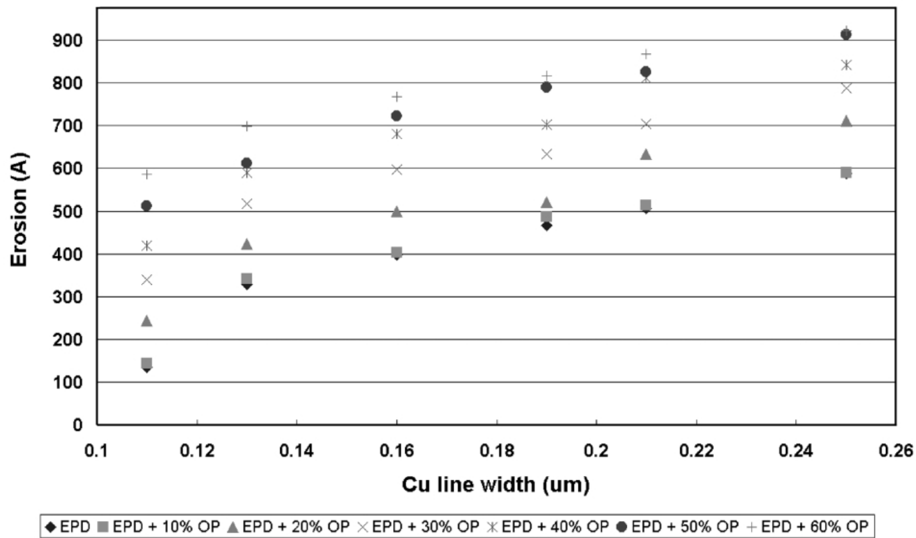

Fig. 3. The effect of Cu line width on erosion at fixed oxide pitch of 120 μm.

area ratio. After Cu polishing, an IMP-TaN layer was sputtered onto the wafer surface. The overburden TaN above the Cu and dielectric was polished away by a TaN module and a cross-sectional view of such a composite structure is given in Fig. 4a. The analysis of capping layer using electron dispersive spectroscopy (EDX) was shown in Fig. 4b. After TaN capping, Cu was isolated from oxidative ambient and its corrosion was thereby prevented. However, the TaN capping raised the resistance of Cu (R_s). Because the composite structure contains high resistivity TaN layer (100 times higher than the Cu), the R_s of Cu containing TaN cap provides 7.9% increment on resistance than that without TaN cap, as shown in Fig. 5. On the other hand, the uniformity of R_s of composite metal is also lower than that without TaN capping. Furthermore, the Cu CMP re-polish would worsen the non-uniformity of R_s.

It is well known that Cu is easier to react with

Table 1
The selectivity of different Cu polish module

CMP polish module	Cu	TaN	FSG	Thermal Ox
1st Module for Cu polish	115	4	0.7	1
2nd Module for TaN polish	1	5.8	3	2.3

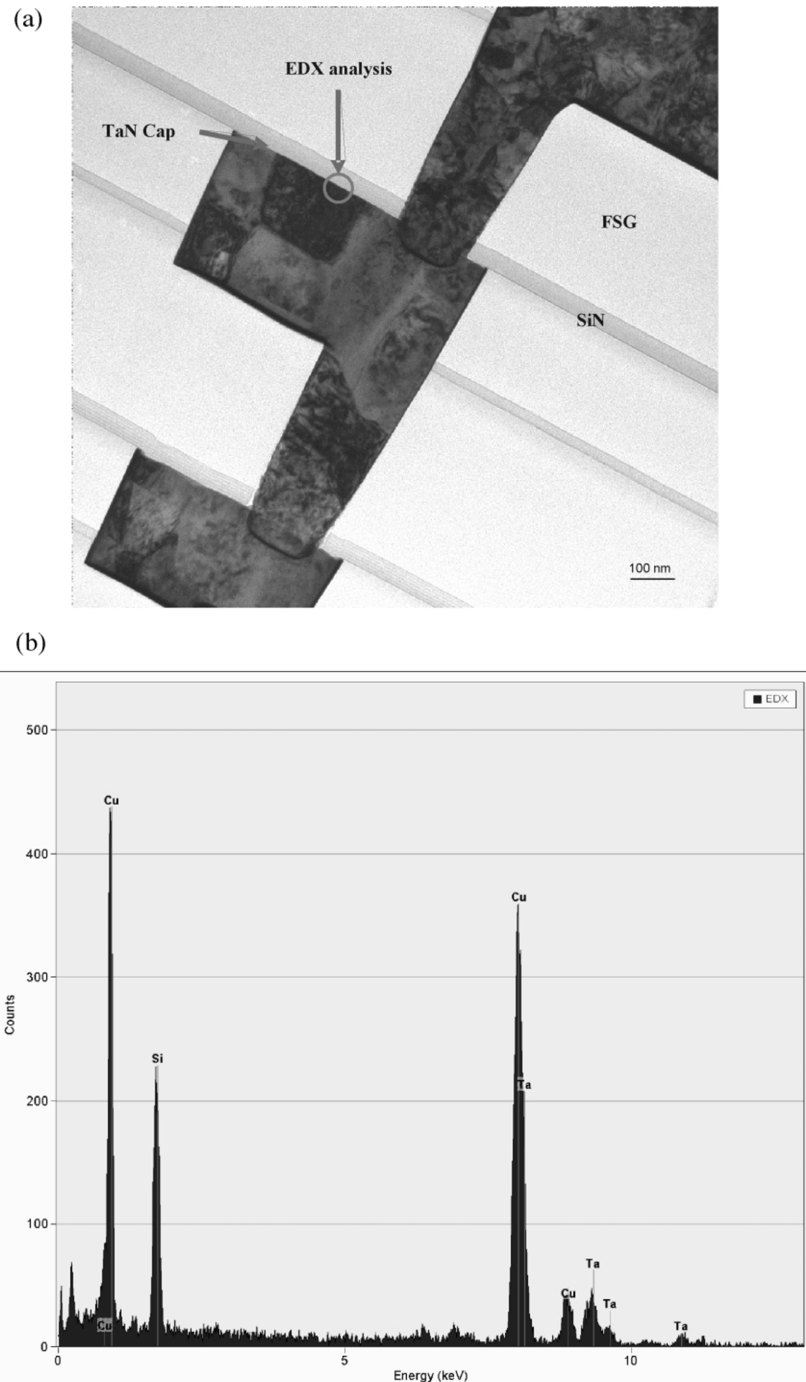

Fig. 4. (a) The cross-sectional view of the Cu surface capped with a very thin layer of TaN. (b) The EDX analysis of the circled area of (a).

oxygen. The oxidation is a continuous reaction due to porous nature of Cu oxide and raises the resistivity of the Cu. The more Cu oxidation occurred, the less speed gain from the material changing from Al to Cu. In addition, the process reliability as well as the lifetime of products will shorten. The corrosion defect characterizations shown in Figs. 6 and 7a,b reveal that the corrosion defects dramatically increase in the specimens without TaN capping. As to the specimens capped with TaN, the defect level remained the same up to 128-h heating treatment at 180 °C. This observation evidenced that the TaN capping could effectively isolate the Cu to prevent corrosion in ambient environment.

Thermal stability is another important issue for the utilization of Cu interconnection. Thermal stability of Cu was evaluated by the via resistance shift and the

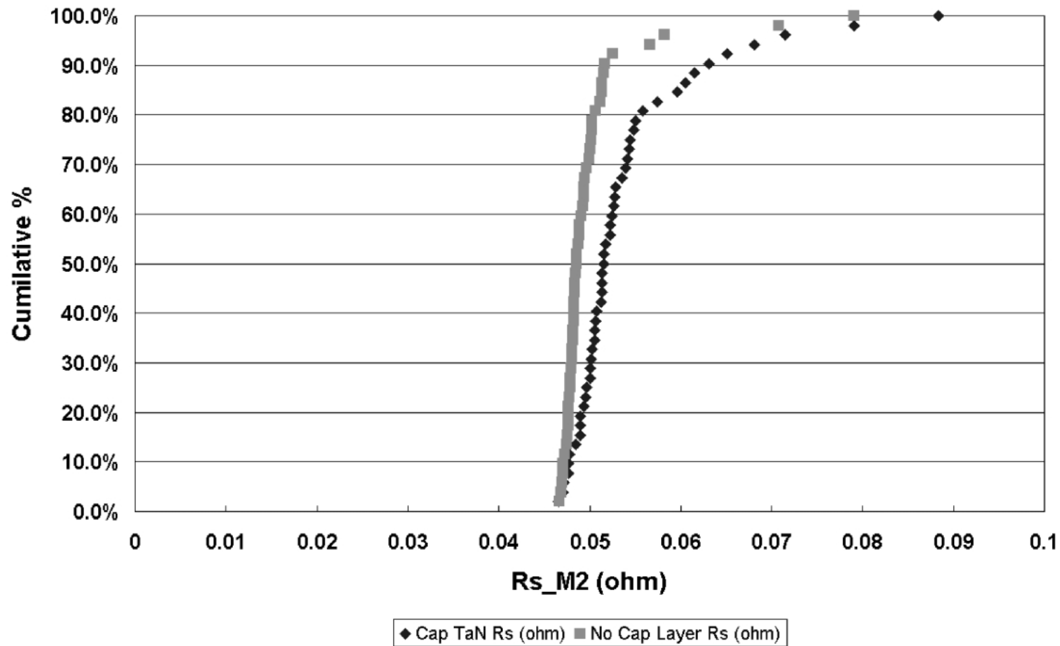

Fig. 5. The R_s of specimens with TaN and without TaN capping at 0.19 μm in width and 1400 μm in length. The R_s of specimens with TaN exhibited 7.9% increment compared with the specimen without TaN capping.

result is shown in Fig. 8. After baking for 170 h in furnace, the specimens capped with TaN exhibited a better thermal stability as indicated by the R_c shift percentage characterization. During the following thermal process, grain growth of Cu occurred and the voids appeared. The interface of via connecting to pre-layer metal is the preferential site of void formation. Poor adhesion between oxide and metal interface was observed at the bottom of via sidewall (i.e. the shrank), as shown in Fig. 9. These voids deteriorated the thermal stability after high-temperature baking. The TaN capping is able to enhance the thermal stability because it restricts the Cu surface from reacting with the oxidative ambient and provides a good adhesion on the next Cu

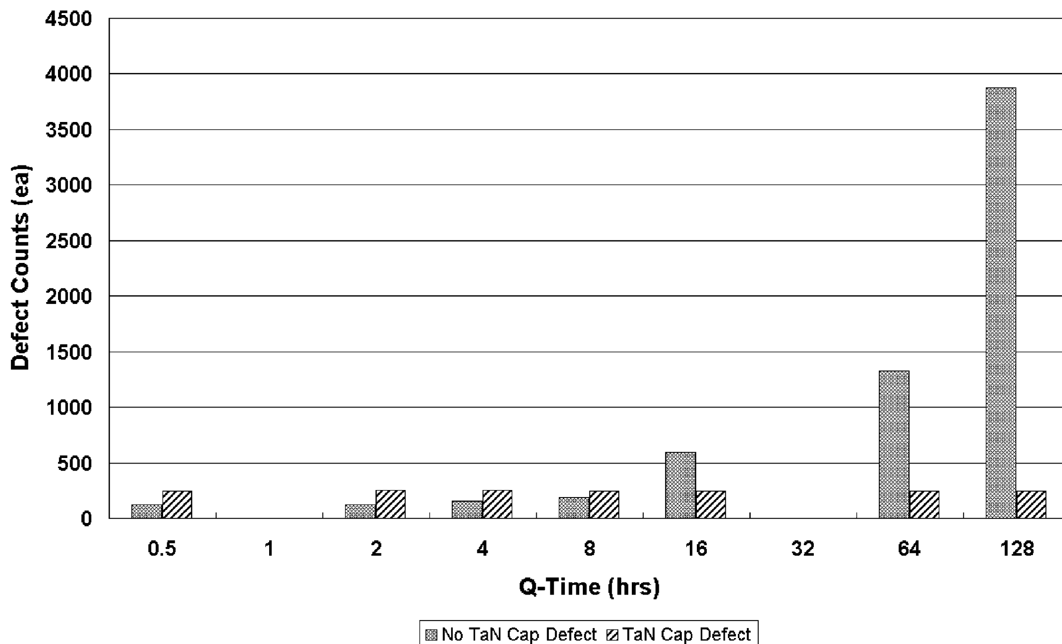

Fig. 6. The relationship between waiting time and defect counts scanned by KLA-AIT-II. The defect counts increase with the waiting time.

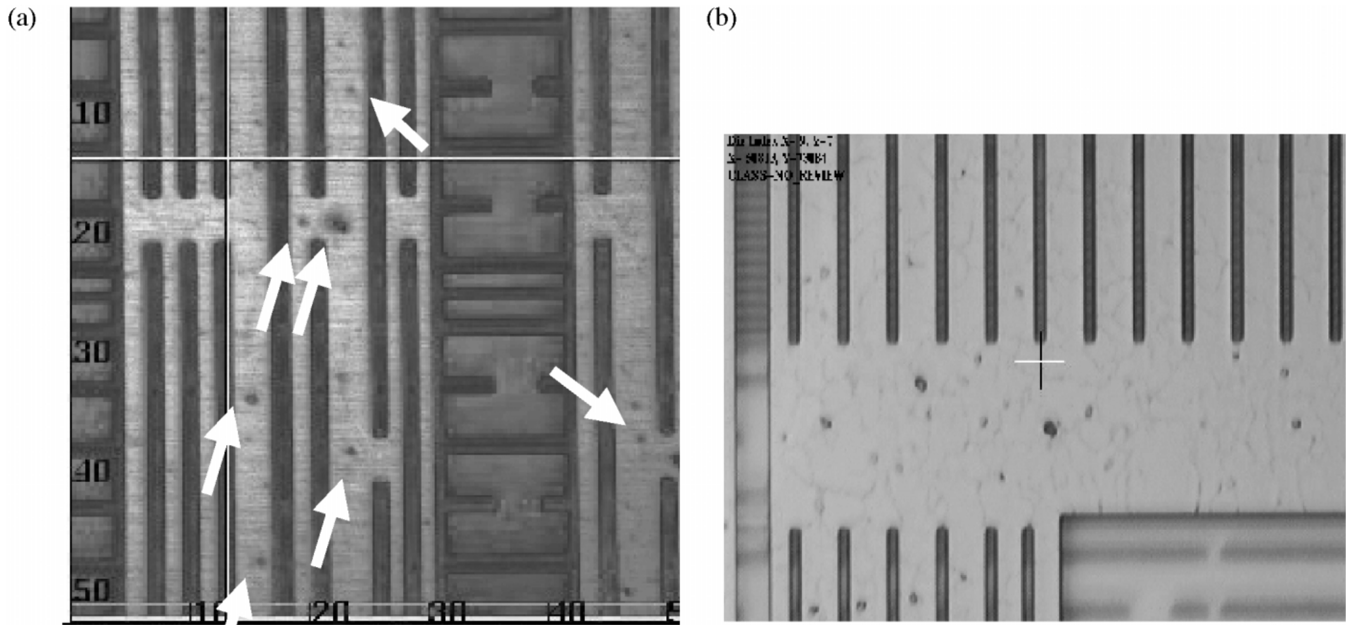

Fig. 7. (a) The corrosion defects observed after annealing for 8 h at 180 °C. (b) The corrosion defects observed after annealing for 128 h at 180 °C.

barrier layer which is also of TaN. In addition, the TaN cap restricts the Cu line and inhibits its expansion during subsequent dielectric deposition. The restriction provides a stable volume of Cu during further thermal processes and hence leads to a higher thermal stability of Cu.

4. Conclusions

In this work, a planarization tendency upon different Cu pad size and density is presented. The amount of Cu dishing and erosion after Cu CMP was found to increase with the increases of Cu pad size and over polish time. By capping a thin TaN layer on Cu, the Cu surface was effectively isolated from the oxidative ambient and the corrosion is presented. Furthermore, there is no increase of defect density in the specimens incorporating with TaN capping process. The TaN capping process also provided a better thermal stability of Cu during subsequent thermal treatment. The only flaw of TaN capping is the increase of R_s, which will deteriorate the operation

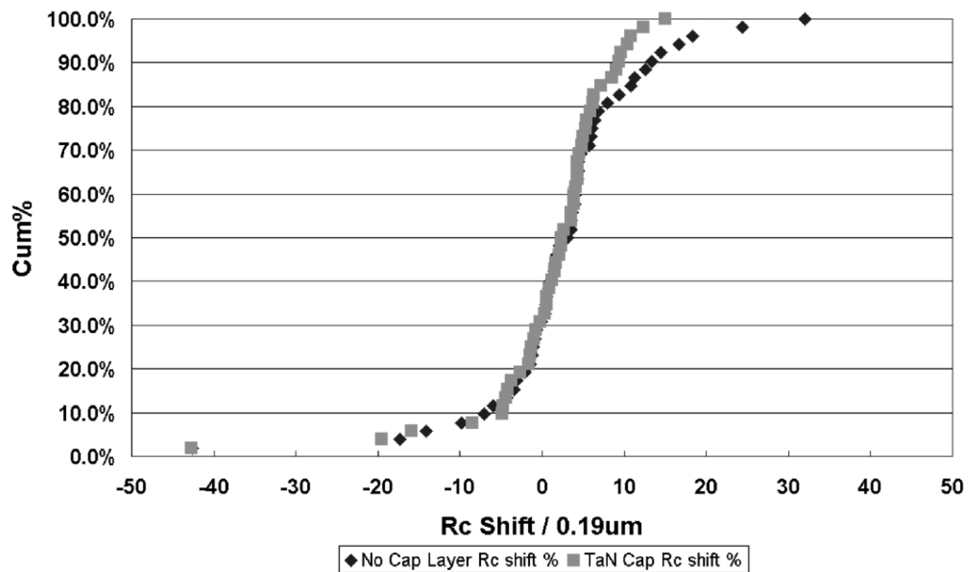

Fig. 8. The shift of R_c after 180 °C baking for 170 h.

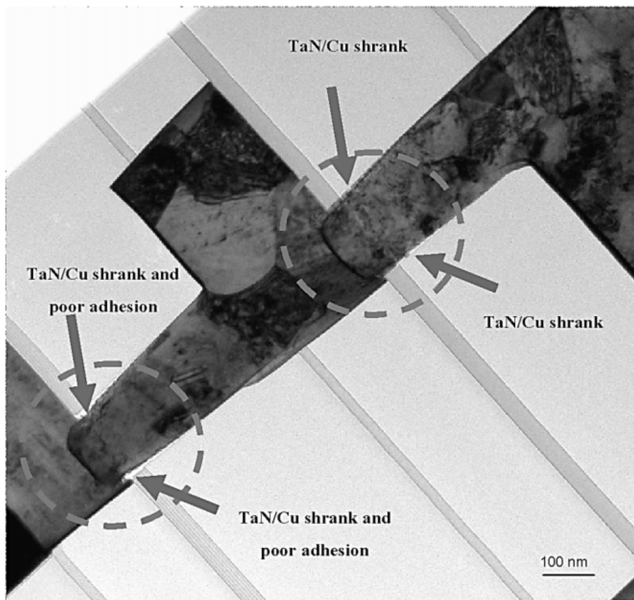

Fig. 9. The via bottom (i.e. the shrank) exhibited a poor adhesion after heat treatment.

speed of devices. However, it could be overcome by design optimization of the circuits.

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