

# Monitor and eliminate the circular defects in HDP–STI deposition through oxynitride/oxide composite liner

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## Abstract

This paper investigates the monitor and elimination methods for the circular defects in high-density-plasma shallow trench isolation (HDP–STI) deposition process. The optical measurement method can monitor the circular defects in early stage. When the thickness of silane-burst film exceeds 7.8 nm, the fit-error can alert the circular defects. The oxynitride/oxide composite liner can eliminate the circular defects. Besides this, the oxynitride/oxide composite liner can also improve the breakdown strength of the STI oxide. The breakdown strength of the STI oxide increases, respectively, 375 and 30% in the wafer center and edge. The uniformity of the STI breakdown strength was reduced from greater than 200% to less than 10% using the composite liner. The traditional N<sub>2</sub>O plasma treatment for stabilizing the oxynitride film is harmful in the HDP–STI process. The N<sub>2</sub>O plasma treatment shows the worst circular defect performance.

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## 1. Introduction

The local oxidation of silicon isolation technique has been used for many years for integrated circuits. The lateral encroachment, also known as bird's beak, is the key disadvantage of this technique, which makes this technique unsuitable for deep submicrometer devices [1–4]. In ultra-large-scale integration, there will be more request to reduce the size of isolation region; thus, shallow trench isolation (STI) process has been developed [5–10].

Recently, high density plasma (HDP) based chemical vapor deposition (CVD) oxide has been extensively used as a trench filling material because of its good characteristics such as good gap-fill, low thermal budget, low HF-etching rate and high throughput [11–14]. However, there are still many issues in the STI process,

such as planarization improvement [15,16], corner shape's effects [17] and process-related defects elimination [18,19].

Investigations on the improvement of STI planarization after CMP have been addressed [15,16,20–22]. A common solution is the implementation of dummy active area regions. These dummy areas are designed in a way such that the local density of active areas over the chip and over the wafer is rather uniform. In that way, the CMP process can be optimized so that dishing is minimized while keeping the nitride erosion to a minimum.

The STI's corner shape improvement have also been extensively studied [17,23–25]. A sharp active corner at the STI edge can lead to a high fringing electric field, which can establish a parasitic transistor with a lower threshold voltage ( $V_t$ ) along the trench edge in parallel to the normal transistor [17]. An edge transistor with a lower  $V_t$  provides a leakage path even before the normal transistor is turned 'on'. One of the easily manufactur-

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able ways is the undercutting of the pad oxide beneath the masking nitride by an isotropic wet etching before the trench liner oxide is grown. Another corner shape's issue is the oxide recess at the upper corner of the trench edge that is believed to cause the subthreshold 'kink'. Many novel STI processes can solve the issue [23–25].

Most STI defects studied were stress-related. The effects of the stress, induced by the STI process, on the device performance such as data retention time and junction leakage have been explored [14,26–34]. The stress-induced defects ever examined were dislocations and circular defects [19,26,27,29,33]. When STI dislocations are located within the depletion region of p–n junction, anomalous junction leakage current could flow. The crystal defects and the mechanical stress are reduced by optimizing the implantation condition and the densification temperature of trench-filled HDP oxide, respectively [26]. Many researchers have proposed models and methods to measure and reduce the stress [35–37].

However, the monitor and reduction of the circular defects in the STI process have seldom been addressed. This investigation considers the monitor methodology for circular defects and provides a solution to eliminate the circular defects.

## 2. Experiment

All wafers used in this study were 200-mm p-type (1 0 0) Si wafers with resistivity 8–12 ohm cm. Wafers were cleaned with standard clean-1 and standard clean-2 before STI process. For pattern wafers, thermal 5-nm oxide layers (pad oxide) were grown atop pre-cleaned Si substrates followed by 160-nm silicon nitride (pad nitride) deposition in a low-pressure CVD diffusion furnace. These stacks were then patterned using deep ultraviolet lithography system with 0.18- $\mu\text{m}$  feature size for trench formation. After trench etching, different liner schemes were processed: (1) Oxide liner: thermal 20-nm dry oxide were grown. (2) Composite oxynitride/oxide liner: thermal 20-nm dry oxide were grown followed by a 20-nm plasma enhanced chemical vapor deposition (PECVD) oxynitride (SION). Then, HDP oxide deposits to fill the trenches. Fig. 1 presented the schemes of SION/oxide composite liner and oxide liner. The  $\text{N}_2\text{O}$  treatment was done after SION deposition. The commercially available Applied Material Centura<sup>®</sup> and Ultima Plus<sup>®</sup> chambers were used for the SION and HDP oxide, respectively. The process parameters for SION were 400 °C, 5.5 Torr, 110-W RF, 54-sccm silane, 82-sccm  $\text{N}_2\text{O}$  and 1600-sccm helium. The process parameters for  $\text{N}_2\text{O}$  plasma treatment were 400 °C, 4.8 Torr, 20 s, 200-W RF and 1400-sccm  $\text{N}_2\text{O}$ . The process parameters for HDP oxide were 1300-W top-RF, 3100-W side-RF, 3000-W bias-RF, 125-sccm argon (Ar), 270-

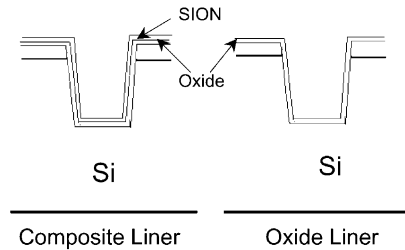


Fig. 1. Schemes of SION/oxide composite liner and oxide liner.

sccm oxygen ( $\text{O}_2$ ) and 140-sccm silane. For blanket wafers, the pad oxide, pad nitride, trench photo and etch steps were skipped. The silane burst film was simulated with films deposited at 110-sccm Ar, 35-sccm silane, 1000-W top-RF and 2500-W side-RF.

The film stress was measured using TENCOR FLX-5400. The contact angle was measured using KYOWA FACE CA-W200 with 10- $\mu\text{l}$  de-ionized water droplet for test. The breakdown voltage was measured using mercury probe by SSM 5100CV system. The criterion for film breakdown was leakage current larger than 10E-4 A. The FTIR was measured using ACCENT QS2000.

## 3. Results and discussion

### 3.1. Circular defects in patterned wafers

Fig. 2a displayed the optical microscopy of the circular defects in pattern wafers. Fig. 2b presented the focus-ion-beam (FIB) photography of the circular defects. Fig. 2d–f showed the film composition analysis: (d) was for the area above the defect, (e) for the defect itself and (f) for the area beneath the defect. The energy dispersive analysis for X-ray (EDX) data yielded that circular defects had higher silicon content than that of the other area around it. This confirmed that circular defects were generated by the existence of a silicon-rich oxide layer between STI oxide and liner oxide. The mechanism for circular defects formation had been explored in the previous research [19].

### 3.2. Circular defects monitor and reduction

Fig. 3 presented the fit-error in the thickness measurement of the STI oxide. The fit-error was highly sensitive to the silane-burst flow. Silane-burst flow was the important factor for the circular defects [19]. When the silane burst-flow time exceeded 3 s, the fit-error was larger than 0. The thickness of the deposited film within 3 s of silane burst-flow was less than 7.8 nm [19]. The circular defects can be monitored in early stage using the fit-error method.

Fig. 4 presents the wafer morphologies with different liners. Fig. 4a yielded some circular defects using the

oxide liner. Fig. 4b showed the worst circular defects using oxynitride with N<sub>2</sub>O treatment (SION-T)/oxide composite liner. Fig. 4c showed no circular defects using the oxynitride without N<sub>2</sub>O treatment (SION-NT)/oxide composite liner. The N<sub>2</sub>O treatment was done in-situ after SION deposition. This step was the default process for SION deposition to improve the SION stability. The benefits of plasma treatment in the dielectric films had been explored in our previous research [38] and by many other researchers [39–41]. However, the N<sub>2</sub>O plasma treatment presented poorest circular defects in this study. The real mechanism for this deterioration needed further study. Using the FTIR, contact angle and stress data gave us some insights into this phenomenon. Fig. 5 plotted the FTIR absorbance intensity for oxide liner, SION-NT/oxide liner and SION-T/oxide liner. Fig. 5 showed that the extra-bonding such as Si–N

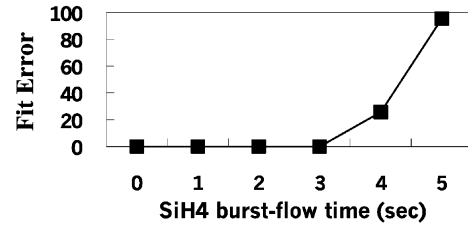


Fig. 3. Fit-error in the thickness measurement of the STI oxide.

caused by the N<sub>2</sub>O plasma treatment was negligible. Table 1 presented the contact angle and stress data for various films. The stress variation between SION-NT and SION-T films were 19%. Our previous study [19] on the circular defects showed that the circular defects were thermal stress related. The SION film became less

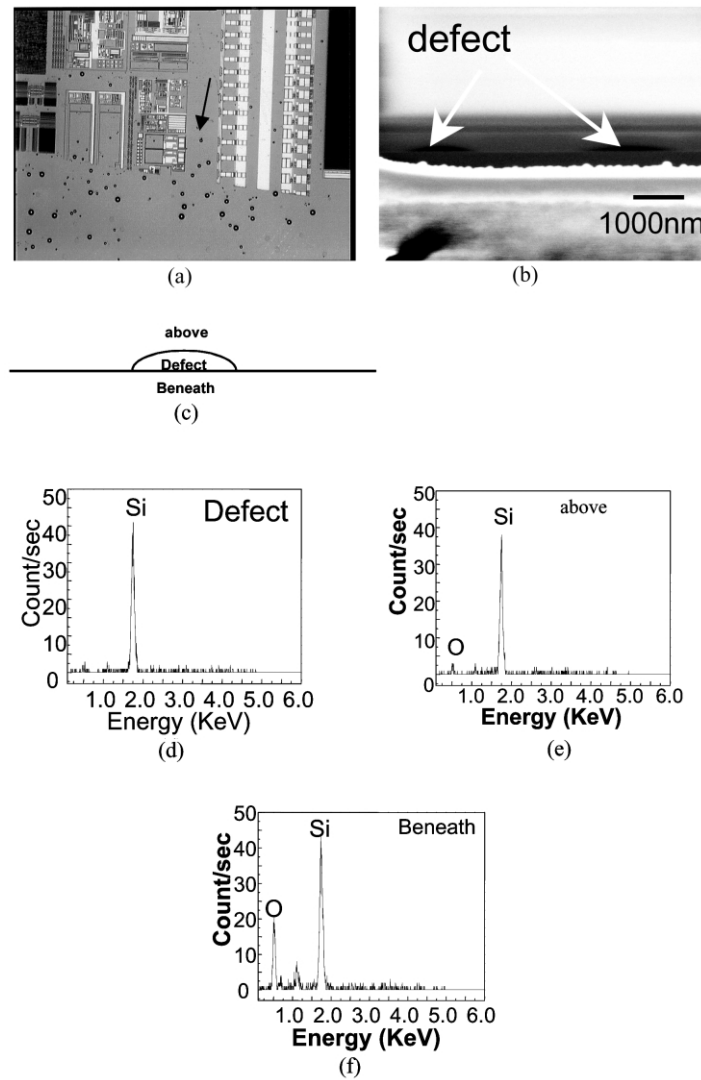


Fig. 2. EDX analysis for circular defects: (a) optical microscopy of the circular defects; (b) FIB photography of the defects; (c) points of EDX analysis; (d) EDX data for area above the defect; (e) EDX data for the defect; (f) EDX data for area beneath the defect.

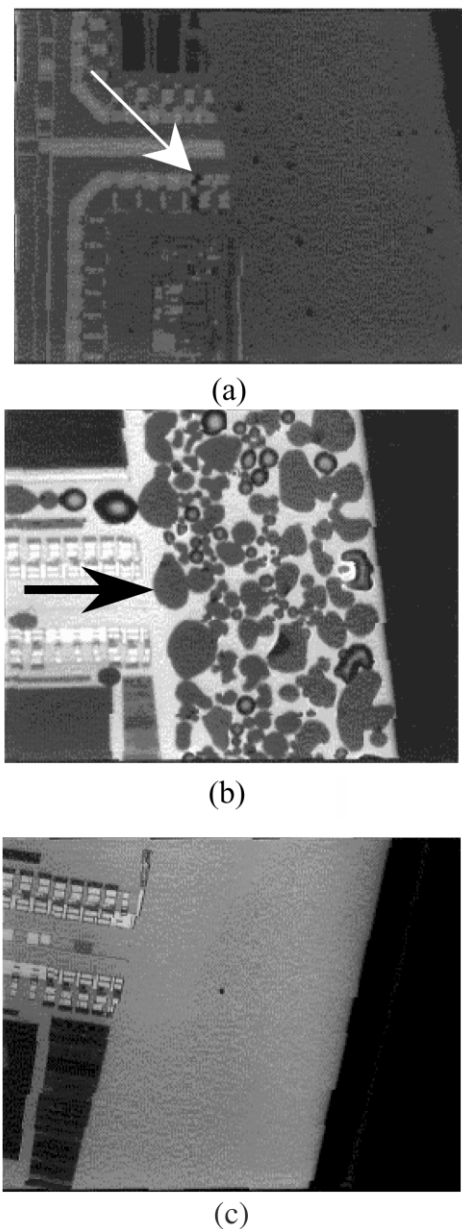


Fig. 4. Wafer morphologies with different liners: (a) oxide liner; (b) oxynitride with  $N_2O$  treatment (SION-T)/oxide composite liner; (c) oxynitride without  $N_2O$  treatment (SION-NT)/oxide composite liner.

compressive after doing  $N_2O$  plasma treatment. The SION-T film with lower compressive stress worsens the circular defect condition. The contact angle variation

Table 1  
Stress data and contact angle for various films

Film	Thickness (nm)	Stress ( $10E9$ , dyne/cm <sup>2</sup> ) <sup>a</sup>	Contact angle (°)
Furnace oxide liner	20	-3.93	33
SION-T	20	-1.35	17
SION-NT	20	-1.66	72

<sup>a</sup> Negative values presented compressive stress.

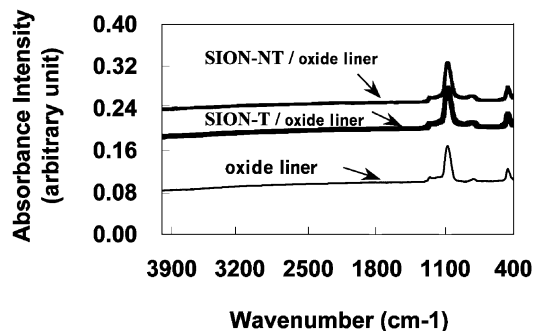


Fig. 5. FTIR absorbance intensity for oxide liner, SION-NT/oxide liner and SION-T/oxide liner.

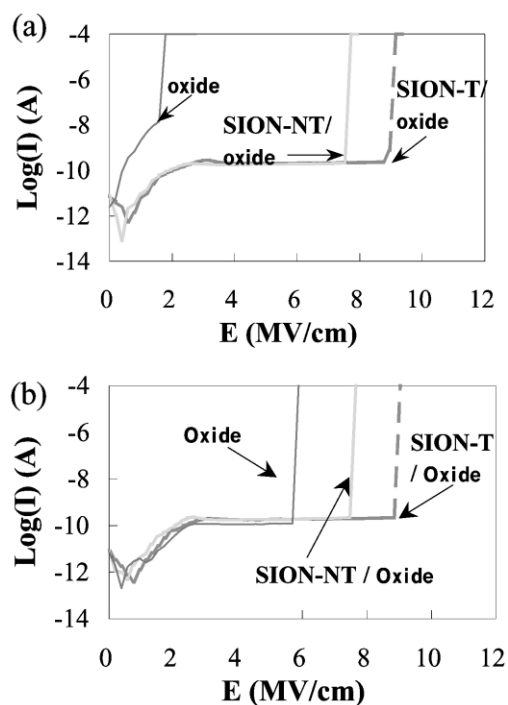


Fig. 6. Breakdown strength for STI oxide with various liners: (a) wafer center; (b) wafer edge.

between SION-NT and SION-T films were 76%. The SION film became more hydrophilic after doing  $N_2O$  plasma treatment. The contact angle analysis yielded that the hydrophobic surface in the SION film was beneficial for eliminating the circular defects.

Table 2  
Breakdown strength for STI oxide using various liners

Film <sup>a</sup>	$E_{B,C}$ (MV/cm) <sup>b</sup>	$E_{B,E}$ (MV/cm) <sup>c</sup>
STI/oxide liner	−1.79	−5.88
STI/SION-T/oxide liner	−9.15	−9.04
STI/SION-NT/oxide liner	−7.72	−7.66

<sup>a</sup> The thickness of STI oxide was 200 nm and liner thickness was kept at 40 nm.

<sup>b</sup>  $E_{B,C}$ : breakdown electric field strength in wafer center.

<sup>c</sup>  $E_{B,E}$ : breakdown electric field strength in wafer edge.

### 3.3. The $I$ – $E$ performance of SION/oxide composite liner

Fig. 6 presented the breakdown strength for STI oxide with various liners. Fig. 6a showed the breakdown strength measured in the wafer center and Fig. 6b in the wafer edge. The oxide liner yielded the poorest breakdown strength. The SION-NT/oxide composite liner had, respectively, 375 and 30% improvement for the breakdown strength in wafer center and edge. The SION-T/oxide composite liner showed 411 and 54% enhancement in wafer center and edge. Although  $N_2O$  plasma treatment showed the best breakdown strength, it led to serious circular defects. Table 2 summarized the breakdown strength of STI oxide with different liner oxides. Besides increasing the breakdown strength, SION/oxide composite liner greatly reduced the within wafer uniformity of breakdown strength from greater than 200% to less than 10%. The major improvement of breakdown strength was in the wafer center. The weak performance of oxide liner in wafer center was possible specific to its growth mechanism. The liner oxide grew in the furnace with the reactants flowing radially toward the wafer center. The SION films deposited in PECVD chamber with downstream reactants toward the wafer surface.

## 4. Conclusions

The mechanism of circular defects in HDP-STI deposition had been explored in the last research [19]. Using the optical measuring method, the circular defects can be monitored. This paper also presented that SION/oxide composite liner can eliminate the circular defects. The original default step of  $N_2O$  plasma treatment in the SION deposition process was used to stabilize the SION film. However, the  $N_2O$  plasma treatment showed the worst circular defects condition in this HDP-STI process. Therefore, the SION film used for the composite liner was no  $N_2O$  plasma treatment. The SION film without  $N_2O$  plasma treatment was represented as SION-NT. The corresponding SION film with  $N_2O$  plasma treatment was represented as SION-T.

Besides solving the circular defects, the composite liner SION-NT/oxide can also improve the breakdown

strength of the STI oxide. The breakdown strength of the STI oxide increased 375 and 30% in the wafer center and edge. The uniformity of the breakdown strength was reduced from greater than 200% to less than 10% using the composite liner.

## References

- [1] J.A. Appels, E. Kooi, M.M. Paffen, J.J.H. Schatorje, W.H.C.G. Verkuylen, Philips Res. Rep. 25 (1970) 118.
- [2] J.W. Lutze, J.P. Krusius, IEEE Trans. Electron Devices Ed-38 (1991) 242.
- [3] S.S. Roth, W.J. Ray, C. Mazure, K. Cooper, H.C. Hirsch, C.D. Gunderson, J. Ko, IEEE Trans. Electron Devices Ed-39 (1992) 1085.
- [4] K. Blumenstock, J. Theisen, P. Pan, J. Dulak, A. Ticknor, T. Sandwick, J. Vac. Sci. Technol. B 12 (1) (1994) 54.
- [5] K. Shiozawa, T. Oishi, H. Maeda, T. Murakami, K. Yasumura, Y. Abe, Y. Tokuda, J. Electrochem. Soc. 145 (1998) 1684.
- [6] K. Shiozawa, T. Oishi, K. Sugihara, A. Furukawa, Y. Abe, Y. Tokuda, Jap. J. Appl. Phys. 38 (1999) 234.
- [7] Bohr, S.U. Ahmed, L. Brigham, R. Chau, R. Gasser, R. Green, W. Hargrove, E. Lee, R. Natter, S. Thompson, K. Weldon, S. Yang, Tech. Dig. Int. Electron Devices Meet. (1994) 273.
- [8] Y. Tamaki, S. Isomae, K. Sagara, T. Kure, J. Electrochem. Soc. 135 (1988) 726.
- [9] L.Q. Xia, S. Nemani, M. Galiano, S. Pichai, S. Chandran, E. Yieh, D. Cote, R. Conti, D. Restaino, D. Tobben, J. Electrochem. Soc. 146 (3) (1999) 1181.
- [10] C.P. Chang, S.F. Shive, S.C. Kuehne, Y. Ma, H. Vuong, F.H. Baumann, M. Bude, E.J. Lloyd, C.S. Pai, M.A. Abdelgadi, R. Dail, C.T. Llu, K.P. Cheung, J.I. Colonell, W.Y.C. Lai, J.F. Miner, H. Vaidya, R.C. Liu, J.T. Clemens, Symposium on VLSI Technology, Digest of Technical Papers, 1999, 161.
- [11] D. Nag, IEDM Tech. Dig. (1996) 841.
- [12] M. Nandakumar, IEDM Tech. Dig. (1997) 657.
- [13] S. Lee, SSDM Dig. (1997) 524.
- [14] K. Saino, K. Okonogi, S. Horiba, M. Sakao, M. Komuro, Y. Takaishi, T. Sakoh, K. Yoshida, K. Koyama, IEDM (1998) 149.
- [15] G. Badenes, R. Rooyackers, E. Augendre, E. Vandamme, C. Perello, N. Heylen, J. Grillaert, L. Deferm, J. Electrochem. Soc. 147 (10) (2000) 3827.
- [16] Y.B. Park, J.Y. Kim, D.W. Seo, W.G. Lee, J. Electrochem. Soc. 148 (10) (2001) 572.
- [17] N. Balasubramanian, E. Johnson, J. Vac. Sci. Technol. B 18 (2) (2002) 700.
- [18] H. Park, K.B. Kim, C.K. Hong, U.I. Chung, M.Y. Lee, Jap. J. Appl. Phys. 37 (1998) 5849.
- [19] J.K. Lan, C.G. Chao, Y.L. Cheng, Y.L. Wang, C.W. Liu, K.-Y. Lo, J. Vac. Sci. Technol. B 21 (5) (2003) 2098.
- [20] S.D. Kim, I.S. Hwang, H.M. Park, J.K. Rhee, J. Vac. Sci. Technol. B 20 (3) (2002) 918.
- [21] A. Itoh, M. Imai, Y. Arimoto, Jpn. J. Appl. Phys. 37 (1998) 1697.
- [22] J.Y. Cheng, T.F. Lei, T.S. Chao, Jpn. J. Appl. Phys. 36 (1997) 1319.
- [23] K. Shiozawa, T. Oishi, Y. Abe, Y. Tokuda, Jap. J. Appl. Phys. 40 (2001) 462.
- [24] W.K. Yeh, T. Lin, C. Chen, J.W. Chou, S.W. Sun, Jap. J. Appl. Phys. 38 (1999) 2300.
- [25] C. Chen, C.Y. Chang, J.W. Chou, W. Lur, S.W. Sun, Jap. J. Appl. Phys. 39 (2000) 1080.

- [26] D. Ha, C. Cho, D. Shin, G.H. Koh, T.Y. Chung, K. Kim, IEEE Trans. Electron Devices 46 (5) (1999) 940.
- [27] H. Lee, J.M. Hwang, Y.J. Park, H.S. Min, IEEE Electron Devices Lett. 20 (5) (1999) 251.
- [28] M.H. Park, S.H. Hong, S.J. Hong, T. Park, S. Song, J.H. Park, H.S. Kim, Y.G. Shin, H.K. Kang, M.Y. Lee, IEDM (1997) 669.
- [29] J.W. Sleight, C. Lin, G.J. Gula, IEEE Electron Devices Lett. 20 (5) (1999) 248.
- [30] P. Smeys, P.B. Griffin, Z.U. Rek, I.D. Wolf, K.C. Saraswat, IEEE Trans. Electron Devices 46 (6) (1999) 1245.
- [31] W.G. En, D.H. Ju, D.C. Chan, S. Chan, O. Karlsson, IEEE International SOI Conference, 2001, 85.
- [32] H. Watanabe, K. Shimizu, Y. Takeuchi, S. Aritome, IEDM (1996) 833.
- [33] P. Smeys, P.B. Griffin, Z.U. Rek, I.D. Wolf, K.C. Saraswat, IEDM (1996) 709.
- [34] V.P. Gopinath, H. Puchner, M. Mirabedini, IEEE Electron Devices Lett. 23 (6) (2002) 312.
- [35] C. Stuer, J.V. Landuyt, H. Bender, I.D. Wolf, R. Rooyackers, G. Badenes, J. Electrochem. Soc. 148 (11) (2001) 597.
- [36] T.K. Kim, D.H. Kim, J.K. Park, T.S. Park, Y.K. Park, H.J. Lee, K.Y. Lee, J.T. Kong, J.W. Park, IEDM (1998) 145.
- [37] K.F. Dombrowski, A. Fischer, B. Dietrich, I.D. Wolf, H. Bender, S. Pochet, V. Simons, R. Rooyackers, G. Badenes, C. Stuer, J.V. Landuyt, IEDM (1999) 357.
- [38] H.J. Lee, E.K. Lin, W.L. Wu, B.M. Fanconi, J.K. Lan, Y.L. Cheng, H.C. Liou, Y.L. Wang, M.S. Feng, C.G. Chao, J. Electrochem. Soc. 148 (10) (2001) F195.
- [39] A.S. Bloot, W. Peters, J.M. Luchies, Fifth International Symposium on Plasma Process-Induced Damage, 2000, 34–37.
- [40] B. Cheon Lim, Y. Jin Choi, J. Hyun Choi, J. Jang, IEEE Trans. Electron Devices 47 (2) (2000) 367–371.
- [41] J. Noguchi, N. Ohashi, T. Jimbo, H. Yamaguchi, K.I. Takeda, K. Hinode, IEEE Trans. Electron Devices 48 (8) (2001) 1340–1345.