

Integration of a stack of two fluorine doped silicon oxide film with ULSI interconnect metallization

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Abstract

Recently, fluorosilicate glass (FSG) has received much attention for application in microelectronics manufacturing due to its low dielectric constant and stable gap-filling ability. Although FSG films have been demonstrated as potential inter metal dielectrics (IMD) for sub-micron devices, integrating a stack of two fluorine doped silicon oxide film deposited on a high-density plasma chemical vapor deposition (HDP-CVD) system for gap filling and a plasma-enhanced chemical vapor deposition (PECVD) system for throughput has not been fully investigated. In this research, an excellent and exceptionally stable process was demonstrated for a stack of HDP-CVD FSG and PECVD FSG layers. Cracks that result from multi-level metal technology were eliminated when higher compressive stress PECVD FSG film was implemented as a capping layer. An 11% capacitance reduction was achieved when comparing a stack of FSG films to undoped silicon oxide. No problem occurred for photo, via etching and chemical mechanical polishing of FSG film. The FSG layer stack's via resistance (R_{c_Via}) as well as a full HDP-FSG scheme is comparable. These results are very promising for the integration of FSG films as inter metal dielectric for devices.

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1. Introduction

As the minimum geometry in the integrated circuits (ICs) continues to shrink, Fluorine doped silicon oxide (FSG) film becomes an attractive solution for reducing the wiring capacitance in ultra large-scale circuits [1–4]. The FSG film has three main advantages: first, it can be deposited both in an high-density-plasma chemical vapor deposition (HDP-CVD) or conventional plasma-enhanced CVD (PECVD) system that become high quality and thermally stable films [5,6]. Second, FSG film can be integrated in a standard inter-metal dielectric (IMD) architecture, due to the HDP-CVD FSG's gap-filling capability superiority over PEOX [7,8]. The combination of the two processes

for different FSG depositing systems, an HDP-CVD FSG film deposition to fill the inter-metal spacing followed by a capping layer deposited by PECVD FSG film is a feasible scheme, for both reliability and throughput. Third, the dielectric constant can be reduced from 4.2 of PECVD oxide film to 3.6 of FSG film, with a decreased capacitance between the lines [9,10].

In this study, we have integrated fluorine doped silicon oxide film with a dielectric constant of 3.6 deposited using HDP-CVD and PECVD into sub-0.18 μm processes. We have optimized the HDP-CVD and PECVD processes for stable FSG film. The low dielectric constant inter-metal dielectric (IMD) was composed with the HDP-CVD FSG film for gap-filling and in the PECVD FSG layer for capping before the chemical mechanical polishing planarization. The HDP-CVD FSG layer's performance and PECVD FSG films were examined in terms of

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film properties and capability to be integrated in sub-micro devices.

2. Experimental

The HDP-CVD FSG films were prepared using an inductively coupled plasma CVD system with gas sources of SiF_4 , SiH_4 , O_2 , and Ar. The substrate temperature was set at 420°C . In the case of the PECVD FSG layers, the substrate temperature was 400°C , deposited in a dual frequency (13.56 MHz and 350 kHz) PECVD system using $\text{SiF}_4/\text{SiH}_4/\text{N}_2\text{O}$ chemistry. Undoped silicon oxide (USG) films were also prepared by the PECVD technique using SiH_4 and N_2O gas mixtures. The different refractive index (RI) of oxide films was deposited by adjusting the different gas ratio. The film's thickness and the FSG film's refractive index were measured using an ellipsometer on 600 nm thick films deposited on Si wafer. The Si–F peak and F percentage were monitored by Fourier transformation infrared spectroscopy (FTIR) (peak Si–F was about 930 cm^{-1}) and was calibrated with Rutherford back scattering (RBS). Film stress was measured with a Flexus stress gauge. The dielectric constant was measured using a mercury probe at 1 MHz. For the adhesion study, the FSG films were deposited on $0.2\text{ }\mu\text{m}$ USG/ $0.7\text{ }\mu\text{m}$ Al stack structure. In addition, the ability of fluorine diffusion was evaluated by a secondary ion mass spectrometry (SIMs) analysis using an oxide/FSG/oxide film sandwich structure. The capacitance reduction and via resistance ($R_{\text{c-Via}}$) at different metal widths and gaps were measured by using a two-layered Al metal structure deposited with 30 nm of Si-rich oxide liner, $0.6\text{ }\mu\text{m}$ of HDP-CVD FSG layer, and a PECVD FSG $1.1\text{ }\mu\text{m}$ cap layer followed by CMP polish.

3. Results and discussions

3.1. Adhesion testing

It is well known that fluorine is an active atom, which reacts easily with other elements. Therefore, a risk of corrosion caused by fluorine exists when applying FSG film in integration on IC production. In order to verify this, the corrosion properties were investigated by depositing a FSG film stack on a TiN/AlCu/TiN/oxide layer/silicon substrate. No abnormal image was observed by the optical microscopy (OM) and SEM after depositing the FSG film. However, bubble-like defects were found following a 410°C thermal test and can be seen in Fig. 1. This seems to indicate some bonding was destroyed or weakened by the thermal-induced reaction. A cross-sectional analysis revealed observed peeling at the metal-FSG interface. Further evidence came from the secondary ion mass spectrometry (SIMs) analysis (as shown in Fig. 2), which indicates fluorine diffused into the TiN layer after the thermal treatment; indicating that a reaction between the fluorine and TiN took place forming a TiFx compound and the TiFx was desorbed [10–12]. This desorbed species became trapped beneath the FSG film and decreased its adhesion ability, leading to blistering. SIMs analysis (not shown) also indicates the thermal cycle was the dominant factor on fluorine stability. The fluorine retains stability and will not diffuse out after deposition. By thermal treatment (the temperature is 410°C in this experiment), fluorine will diffuse into the metal layer and react with Ti and form TiFx. As noted in Fig. 3, the stress changes after the 410°C thermal test also demonstrates this evocation. It exhibited that no stress change occurred for the FSG/TiN/AlCu/TiN/oxide layer even after 1 month in an air environment. Further, after thermal cycling at 410°C , stress

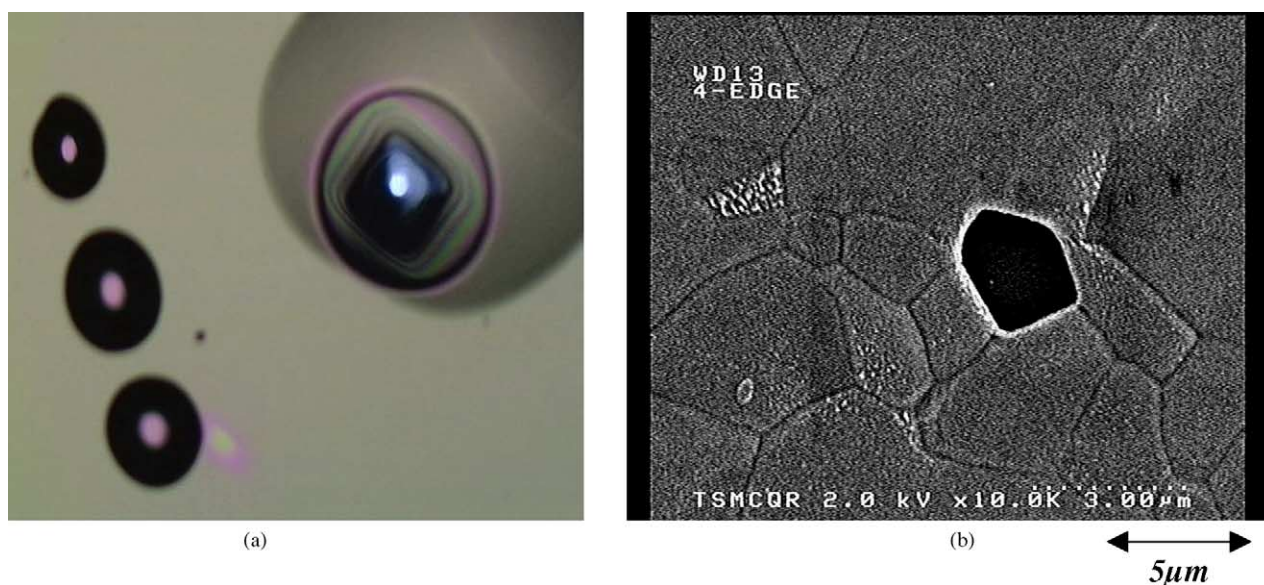


Fig. 1. Corrosion images of FSG/TiN/AlCu/TiN/oxide: (a) OM image and (b) SEM image.

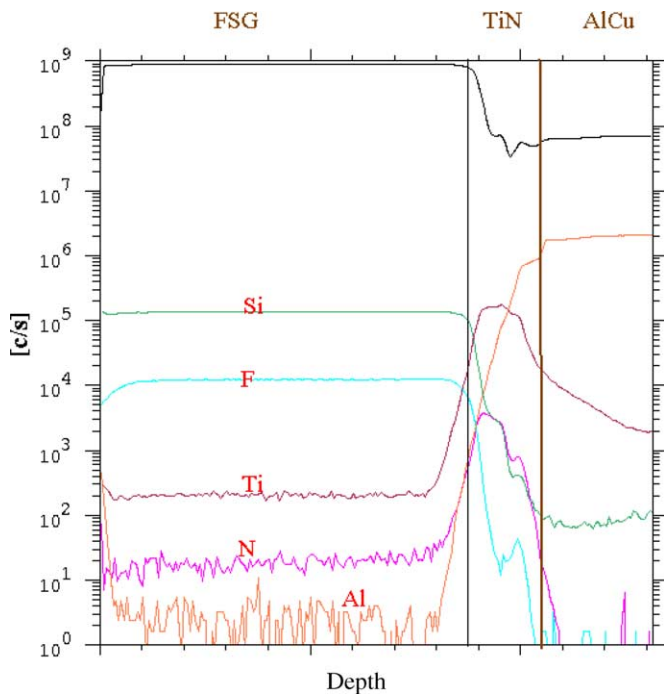


Fig. 2. The SIMS profile for FSG/TiN/AlCu/TiN structure.

would change, which suggests that at elevated temperatures, a reaction may occur.

As the IC process possesses many thermal budgets, the implication is that a good barrier layer is required to prevent the fluorine from diffusing into the metal layer. As a result, the varying oxide films were deposited in plasma-enhanced CVD by changing the SiH₄/N₂O ratio to evaluate the efficiency of the fluorine barrier effect. Fig. 4 shows the differ-

ent oxide layer and HDP-CVD FSG layer's SIMS profile. The results showed that the higher the Si concentration is in oxide films, the better its ability is to block F diffuse out. As a result, silane-based silicon rich oxide film (SRO, refractive index was 1.5, O:Si ratio < 2:1) was recognized as good fluorine barrier against diffusing out. The diffusing depth was about 20 nm SRO film containing a substantial number of unterminated silicon bonds, which quickly got free fluorine to form Si–F bonds. A 30 nm silicon-rich oxide film prior to HDP-CVD FSG film deposition was shown to be an effective solution to solve metal corrosion issue. No corrosion was demonstrated before and/or after the alloy process tests for the TiN/ALCu/TiN/30 nm Si-rich oxide/FSG scheme.

3.2. The physical priorities of FSG film

In ultra large-scale single damascene technology, the HDP-CVD FSG has two functions; providing low-dielectric constant films and achieving gap-filling capability. Using full HDP-CVD FSG film as IMD layer was an expensive and time-consuming HDP process because of the simultaneous sputter and deposition. From the manufacturing viewpoint, the full HDP-CVD FSG scheme was assessed as a low-throughput. As a result, the stack film makes of 0.6 μm thick HDP-CVD FSG film and followed deposited with 1.1 μm thick PECVD FSG films seems to be an acceptable solution for the global interconnect scheme. The fundamental HDP-CVD FSG and PECVD FSG film's properties are detailed listed in Table 1. The fluorine concentration was chosen as 4.5 at.% for HDP-CVD FSG films and 6.0 at.% for PECVD FSG films.

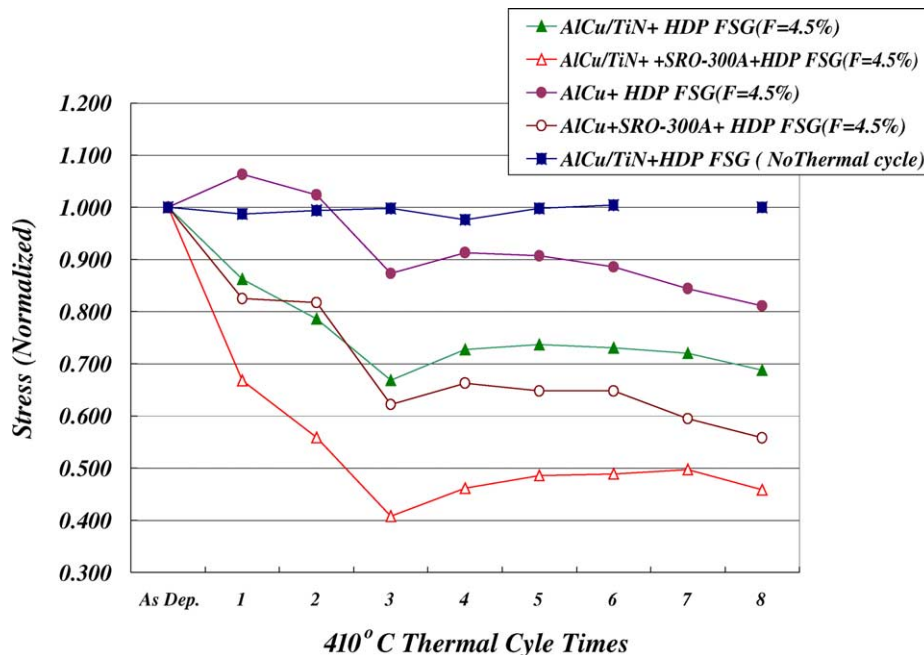


Fig. 3. The stress change for TiN/AlCu/TiN/FSG structure after 410°C alloy test.

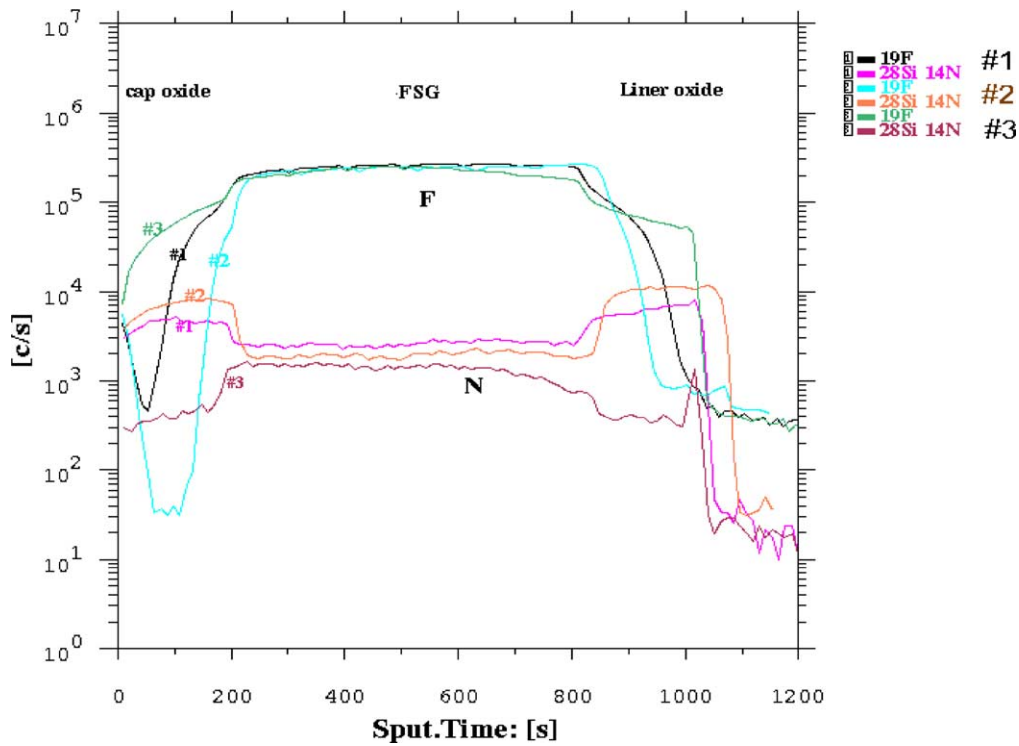


Fig. 4. The *F* profile of FSG film with different oxide for oxide/FSG/oxide structure: (1) RI = 1.480 oxide, (2) RI = 1.460 oxide, and (3) RI = 1.500 oxide.

As shown in Table 1, the PECVD FSG film’s stress was more compressive, which is suitable for multi-layered metalization. Since the stress of the deposition film is essential for implementing the film as an IMD layer. Too low or large stress of the IMD film would induce integration problems. Fig. 5 shows the crack SEM image for implementing full HDP-CVD FSG film as an IMD layer. Depending on the IMD crack location, the HDP-CVD FSG film’s low compressive stress was suspected to be the root cause that induced the IMD crack in multi-layer metalization. Two main factors were used to improve the HDP-CVD FSG layer’s film compressive stress. There were limited improvements. One was reducing deposition temperature. This had an unstable fluorine side effect. The other was decreasing the concentration in the FSG film, which downgraded the effect of lower dielectric constant material. The stress hysteresis curve for full HDP-CVD FSG and stack films are showed

in Fig. 6. The stress deviations were $1.2E8 \text{ dynes cm}^{-2}$ and $3.0E8 \text{ dynes cm}^{-2}$ for HDP-CVD FSG films and stack FSG layers, respectively, after the first 500°C thermal cycle. Higher stress hysteresis for stack layers implies that the film does change due to the combination of two types of FSG films. The stress hysteresis was almost zero after the second 500°C thermal cycle. It also indicated that the stress ($-1.2E9 \text{ dynes cm}^{-2}$, compressive) will be higher for HDP-CVD FSG and PECVD FSG film’s stack layers after a 500°C thermal cycle. That is, the stack films compensate the multi-layers metalization tensile stress, which reduces

Table 1
The film properties of HDP-CVD FSG and PECVD FSG layer

	HDP-CVD FSG	PECVD FSG
Dep. rate (nm min^{-1})	321.5	687.4
Uniformity (49P, 3 mm exclusion)	1.943	1.421
RI (633 nm)	1.4413	1.4416
Stress	$-6.00E + 08$	$-1.70E + 09$
<i>F</i> (% SiF/Si–O)	4.5	6
Dielectric constant	3.624	3.702

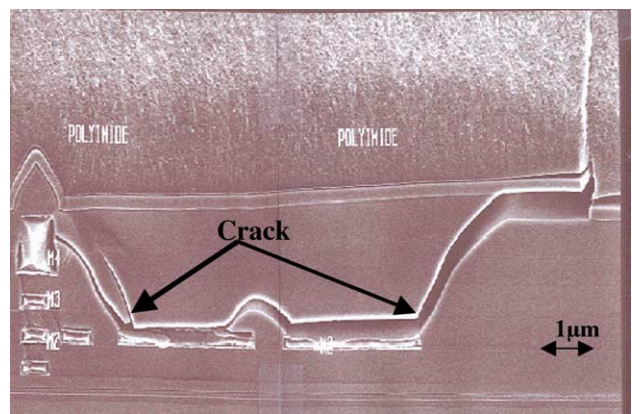


Fig. 5. The SEM image of full HDP-CVD FSG IMD Film crack on four-layer metal design.

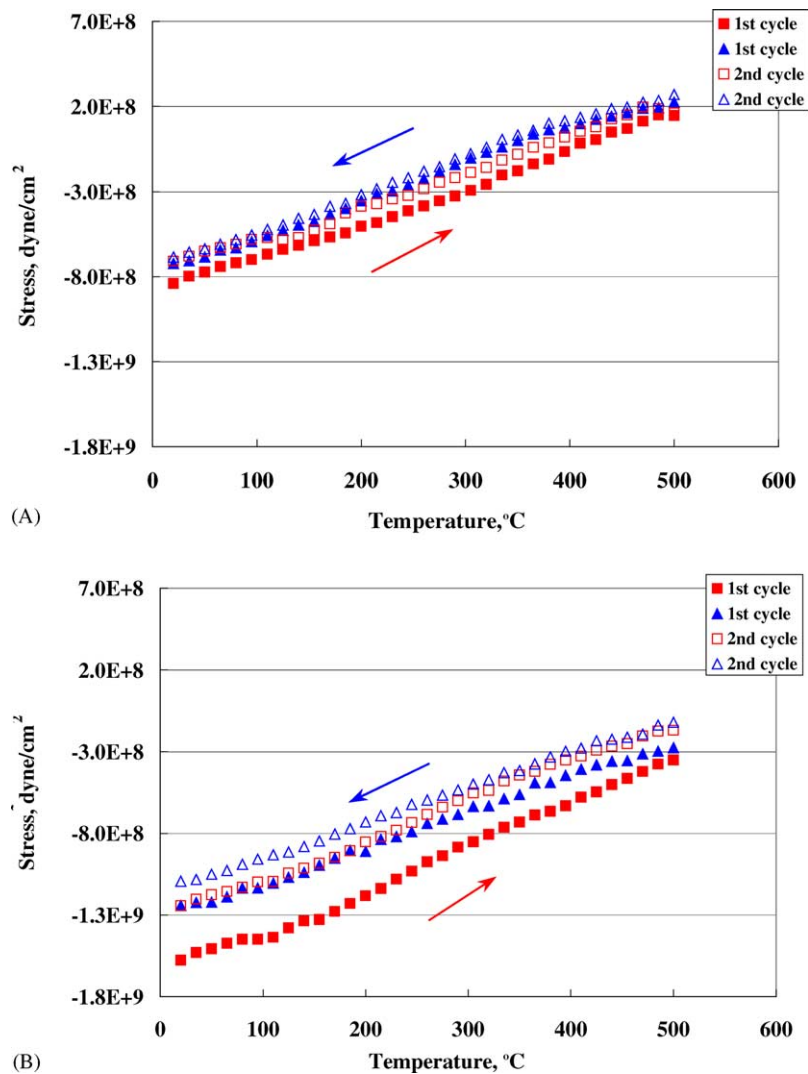


Fig. 6. The stress hysteresis of FSG film: (A) full HDP-CVD FSG layer and (B) A stack of HDP-CVD and PECVD FSG layer.

film crack in integration. By a long-time trace after adapting a stack of two FSG films, no crack was found for the stack film scheme.

3.3. Integration features

A partial integrated structure with the via holes is reported in Fig. 7. The via hole's critical dimension (CD), dry etch

rate and chemical mechanical polishing rate has been listed in Table 2. The CD showed no significant differences for the two different schemes. The via etch had been performed using the applied materials HDP etcher system. The etching rate was measured at $143.2 \text{ nm min}^{-1}$. HDP-CVD FSG film, and $158.3 \text{ nm min}^{-1}$, for the PECVD FSG layers. In comparison, the undoped PEOX and PETEOS film etch rate was measured at $140.5 \text{ nm min}^{-1}$. This is lower than the FSG

Table 2
The integration properties of HDP-CVD FSG and PECVD FSG layer

		HDP-CVD FSG	PECVD FSG	PECVD oxide
Control wafer	Etch rate (nm min^{-1})	262.1	270.3	243.1
	CMP polish rate (nm min^{-1})	241.6	289.6	222.6
	Etch rate (nm min^{-1})	143.2	158.3	140.5
Pattern wafer	(CMP) polish selective	1.026	1.045	1
	CD of via	0.2562	0.2564	–

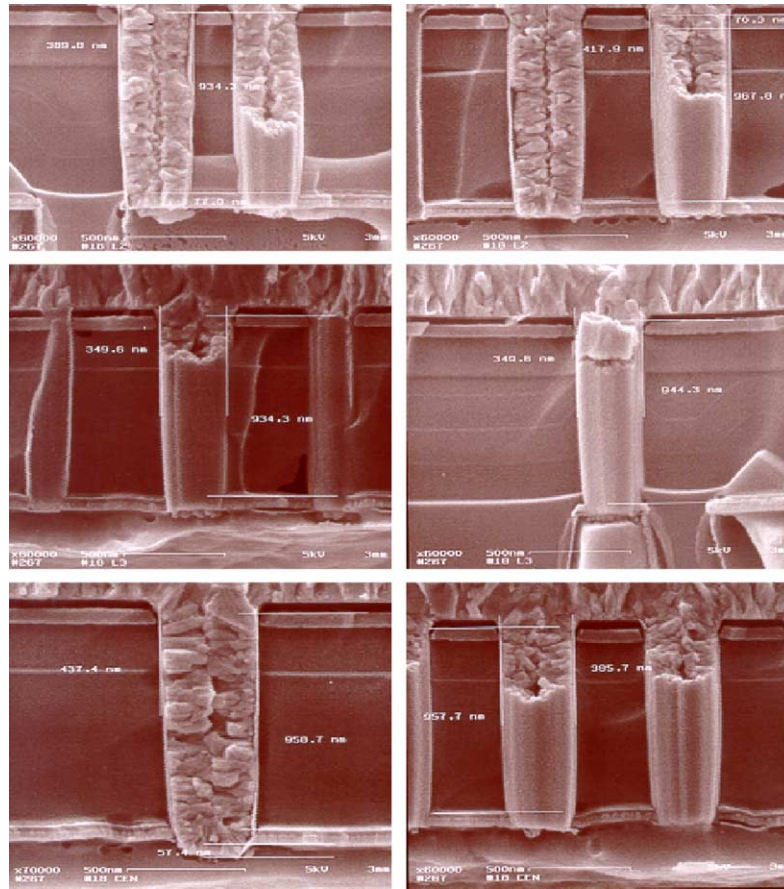


Fig. 7. Partial integration of a stack of HDP-CVD FSG and PECVD FSG layer.

layer's. In a FSG film's stack, the mechanical polishing process was performed on PECVD FSG film. The PECVD FSG film's polishing rate ($289.6 \text{ nm min}^{-1}$) was 40 and 60 nm higher than those of the HDP-CVD FSG layer and undoped PECVD oxide film on a blanket wafer. The same trend was found on pattern wafers. That is, it is as beneficial for improving throughput as taking two stack FSG films as the IMD scheme. Considering the global planarization's effect, the HDP-CVD FSG layer's profile on control wafer would collapse at 85 mm from the wafer edge. This is because the smaller chamber spacing for the HDP-CVD hardware design was limited. However, no such phenomenon was found with PECVD FSG film, as shown in Fig. 8. The fifth interlayer FSG film's edge profile was in a pattern wafer after CMP process, the collapse location on wafer's edge was extended from 85 to 95 mm (as shown in Fig. 9), which provides an improvement in total wafer edge yield.

3.4. The capacitance reduction and via resistance

Because the purpose of using low- k materials is to reduce the capacitance for smaller geometry, the capacitance reduction will directly influence the device's performance. The line-to-line capacitance of patterns with different FSG IMD

structures was measured at different metal widths and gaps. The line-to-line capacitance reduction for the stack FSG films varies with the metal spacing is shown in Fig. 10. It indicates that wider metal spacing has a smaller impact than the thinner metal spacing on the line-to-line capacitance. The larger capacitance observed at wider metal spacing is the result of a larger fringe capacitance between the wider metal spacing. Comparing with different inter-metal schemes with different metal spacing/widths, it shows that Si-rich oxide with 30 nm thickness was induced to decrease average line-to-line capacitance reduction from 12 to 10–11%. In addition, in comparing the full HDP-CVD FSG layer and stack layers, the line-to-line capacitance reduction was found comparable, which achieves a 10–11% reduction when compared to undoped silicon oxide film. A stack of FSG film's via resistance needs to be investigated to ensure that a stack of FSG scheme can be processed without affecting the via yield. The different IMD layer's via resistance at a different via hole is also checked. If compared with the full HDP-CVD FSG case, R_{c_Via} for IMD consisted of a stack of HDP-CVD and PECVD FSG that was comparable with a full HDP-FSG scheme. Nonetheless, the R_{c_Via} 's variation is considered insignificant. The conclusion shows that a stack of HDP-CVD FSG and PECVD FSG film as IMD is suitable

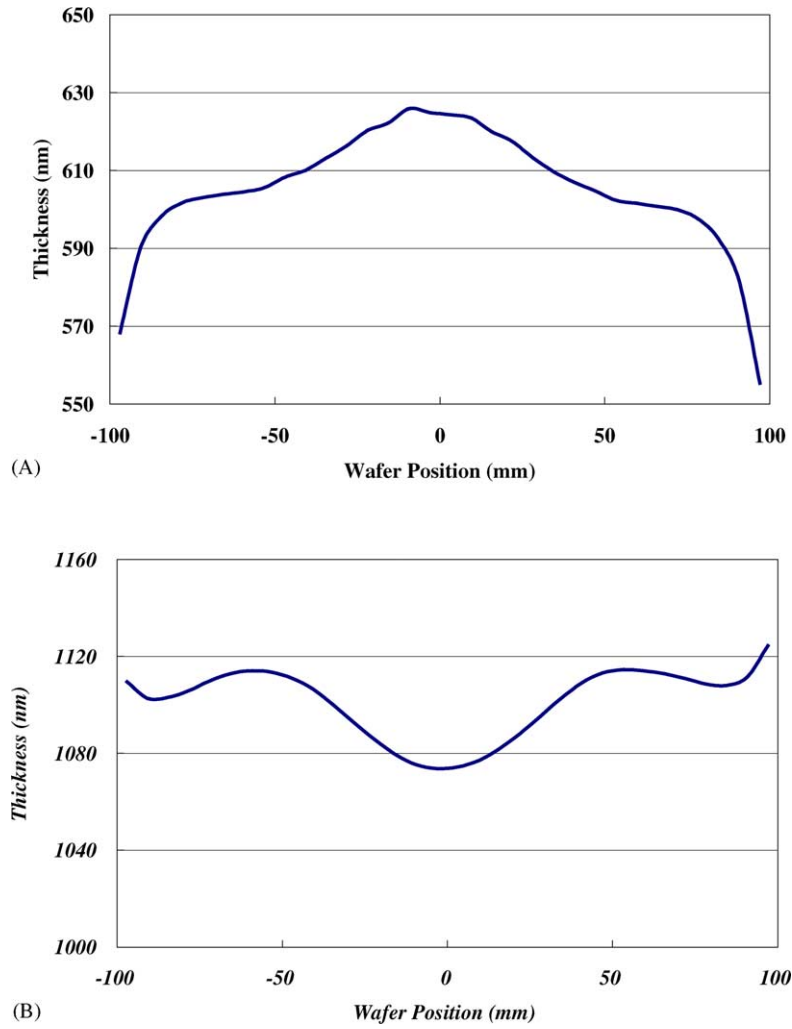


Fig. 8. The profile of FSG film on 200 mm control wafer: (left) HDP-CVD FSG and (right) PECVD FSG.

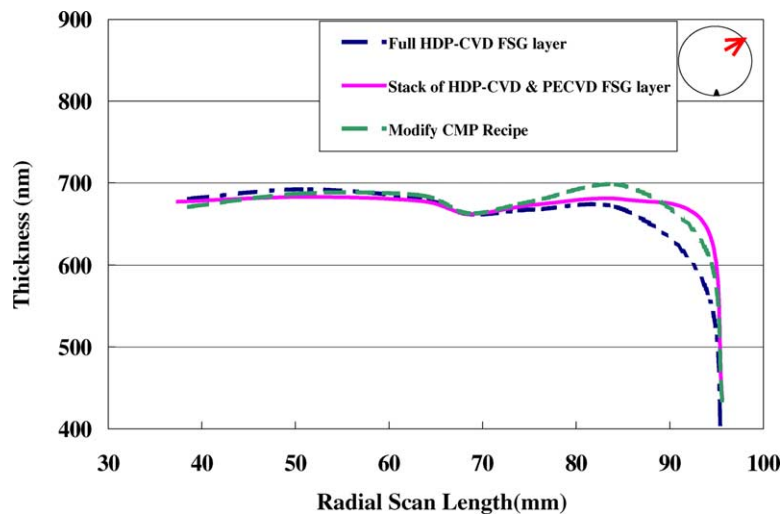


Fig. 9. Edge profile of the fifth IMD-layers dielectric films in product with different FSG film after CMP.

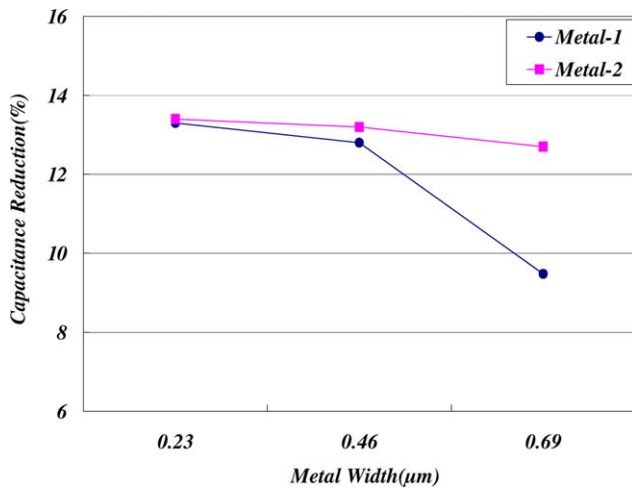


Fig. 10. Line-to-line capacitance of FSG layer for different metal structure with 0.23 μm gap.

and reliable for low- k applications on the sub-micron processes.

4. Conclusion

The stack made of 0.6 μm thick HDP-CVD FSG film for gap-filling and followed by capping with 1.1 μm PECVD FSG films is a good compromise to fill narrow gaps between metal lines, to reduce the capacitance in the plane and between metal levels, and to optimize the throughput on a global isolation structure. Additionally, to prevent poor adhesion due to fluorine diffuse into metal layer, 30 nm thick SRO film was deposited prior to HDP-CVD FSG film. It has successfully demonstrated promising film properties as well as easy drop-in device and process integration feasibility for IMD applications in sub-0.18 μm generations. No signifi-

cant issue has been shown to realize the partial integration of FSG films. On the other hand, implementing a stack of FSG layers as the IMD for the interconnect of the 0.18 μm generation exhibited 10–11% gain in the ring-oscillator's RC delay. Based on the electrical and reliability test results, it is believed that this stack deposited of HDP-CVD FSG film capped with a PECVD FSG layer is a good candidate for advanced sub-micro inter-metal dielectric.

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