New Current-Mode Wave-Pipelined Architectures for High-Speed Analog-to-Digital Converters

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***Abstract*—In this paper, two new architectures for high-speed CMOS wave-pipelined current-mode A/D converters (WP-IADCs) are proposed and analyzed. In the new WP-IADC architectures, the wave-pipelined theory is applied to both pipeline structures, called full WP-IADC (FWP-IADC) and indirect transfer WP-IADC (ITWP-IADC). In the FWP-IADC, each stage uses the full current-mode wave-pipelined structure without switched-current cell circuits. In the ITWP-IADC, the switched-current cells are incorporated into the wave-pipelined stages which are divided into several sections with controlled clocks. Therefore, the proposed ITWP-IADC performs optimally in terms of speed and accuracy in the WP-IADCs. Generally, the proposed WP-IADCs have the advantages of high speed, high input frequency, high efficiency of timing usage, high clock-period flexibility in switched-current cells for precision enhancement, and reduced number of switched-current cells in the overall data path for linearity improvement. According to the theoretical analysis on the proposed WP-IADC structures, the minimum sampling clock period is proportional to the intrinsic delay of the current mirror and the increased rise/fall time in each wave-pipelined stage. The HSPICE simulation results reveal that, under Nyquist rate sampling in 8-b resolution, a sampling rate of 20 and 54 MHz can be achieved for FWP-IADC and two-section ITWP-IADC, respectively. If four wave-pipelined sections are used, the ITWP-IADC can be operated at 166 MHz at an input frequency of 8 MHz. To experimentally verify the correct function of the proposed WP-IADC structures, the proposed new architecture of the FWP-IADC is implemented by using 0.35-μm CMOS technology. The measurement results successfully demonstrate the feasibility of wave-pipelined IADC architectures in applications of high-speed ADCs.**

***Index Terms*—CMOS technology, current-mode A/D converter, switched-current cell, wave pipelined.**

I. Introduction

CURRENT-MODE signal processing techniques have been extensively adopted in several applications that involve low-power, high-speed, or complex arithmetic computation in integrated circuits. Such applications include data converters, filters, and cellular neural networks [1]–[3]. Current-mode ICs have several important features. First, current-mode circuits can easily implement the basic functions of inversion, scaling, and summation, without using op amps [4]. Second, the voltage swing required in current-mode circuits is smaller than that required in voltage-mode circuits, due to the square I–V law of MOS transistors operated in the saturation region. Third, the current switch can achieve high-speed operation in many applications. These three features make the high-performance current-mode design feasible.

So far, many high-speed digital-to-analog converters (DACs) have been successfully implemented using the current steering technique [5], [6]. Several current-mode analog-to-digital converters (IADCs) have been also developed [7]–[15]. Among them, the pipelined IADC structure [12]–[15] has exhibited high-speed performance. Especially in the work of [15], 32 parallel pipeline IADCs were used and each IADC was run at 125 MSample/s. The overall IADC can achieve 4 Gsample/s at 6-b resolution under calibration and at an input frequency of 1 GHz.

In a pipelined IADC, the current sample and hold (S/H) circuit is the most critical component. It limits both the accuracy and the conversion rate of the IADC. The current S/H circuit is normally based on the switch-current (SI) technique. However, the switch clock feedthrough problem in SI circuits is more serious than that in switch-capacitor circuits because any error voltage produced on the gate of the current-holding transistor causes a large current error, according to the square current law. Although many circuit techniques have been proposed to improve the SI structure, a long period is still required to cancel the clock feedthrough effect [14]. Consequently, the accuracy and high-speed are traded off in the current S/H circuits (switched-current circuits).

Wave-pipelined theory has been successfully adopted in regular digital systems, such as DRAM, SRAM, and digital multipliers, among others [16]–[20], to achieve high-speed performance. In this work, wave-pipelined theory is applied to ADC design [21] as the first application of the theory to analog IC design. Two novel wave-pipelined architectures called full WP-IADC (FWP-IADC) and indirect transfer WP-IADC (ITWP-IADC) are proposed and analyzed. The full current-mode wave-pipelined structure is used in each stage of the FWP-IADC, without switched-current cell circuits. In the ITWP-IADC, the switched-current cells are incorporated into the wave-pipelined stages to obtain better speed performance. Both wave-pipelined architectures are analyzed and simulated by HSPICE. The proposed ITWP-IADC is shown to achieve 166 MS/s with 8-b resolution at an input signal of 8 MHz. Moreover, measurement results of the experimental chip have successfully verified the function of FWP-IADC. Applying the wave-pipelined structures in an ADC can prevent or reduce the use of switched-current circuits in the pipelined path. Thus, the

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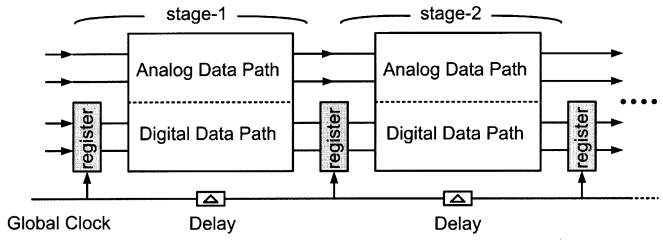


Fig. 1. Wave-pipelined ADC system.

optimal performance in terms of speed and accuracy can be obtained.

The rest of this paper is organized as follows. Section II describes the architectures and the design considerations of the wave-pipelined IADC (WP-IADC). Section III explicates the circuit design and simulation results. Section IV presents the experimental results. Finally, Section V draws conclusions and suggests directions for future research.

II. Wave-Pipelined ADCs

A. Full Wave-Pipelined Current-Mode ADC (FWP-IADC)

This work proposes wave-pipelined architectures to improve the speed of the current-mode analog-to-digital converter (IADC). The proposed full wave-pipelined current-mode analog-to-digital converter (FWP-IADC) is designed without switched-current circuits. Fig. 1 presents the underlying concept of the wave-pipelined ADC system. In Fig. 1, the S/H circuits have been removed from the ADC system. A delayed clock, instead of a global clock, controls the digital registers, except in the first stage. Fig. 2 displays a conceptual block diagram of the proposed FWP-IADC. An 8-b structure is considered as an example. The 8-b IADC consists of one voltage sample and hold (S/H) circuit, one V/I conversion circuit, one pre-stage, seven identical 1-b pipelined stages, and one final current comparator. The voltage S/H circuit is used to generate the sample-data waveforms of the input voltage $V_{\rm in}$, whereas the V/I converter is used to convert the voltage waveforms into current waveforms as $I_{\rm in}$. Accordingly, sample-data waveforms of the input high-frequency current signals can be generated.

In the FWP-IADC architecture, the pre-stage is used to generate the difference current between the reference current $I_r/2$ and the current signal I_0. The difference current is sent to the current comparator of $\rm stage_1$. Meanwhile, the current mirror stage $\rm CM_0$ is used to reproduce the input current $I_{\rm in}$ as I_0 and I_0'. Each 1-b pipelined stage includes one current mirror stage $(\rm CM_{\it i})$, one current comparator (CCMP), one D-type flip-flop (DFF), and one current-mode digital-to-analog subconverter (sub-$\rm DAC_{\it i}$), as shown in Fig. 2. The current mirror stages $\rm CM_{\it i}$ are used to reproduce and propagate the input current I_{i-1}' to I_i and I_i', with an appropriate delay to match that in the path of CCMP, DFF and sub-$\rm DAC_{\it i}$. The input current of the current comparator is the resultant current I_{i-1}-$\rm Iref_{\it i-1}$ of the last stage. If current I_{i-1} is greater (smaller) than $\rm Iref_{\it i-1}$, then the corresponding bit B_i is set to logic ONE (ZERO). The output bit B_i is stored in the DFF. After B_i is determined, the digital output B_i is sent to the following stage and serves as the input signal of the sub-$\rm DAC_{\it i}$. The digital input signals of sub-$\rm DAC_{\it i}$ are the output digital signals of all CCMPs in the preceding pipelined stages, as well as B_i. These signals are converted into the output current signal $\rm Iref_{\it i}$. The sub-$\rm DAC_{\it i}$ output current $\rm Iref_{\it i}$ is determined by the following rule used to implement the ADC process, in a manner similar to the successive approximation algorithm [22]:

$$\rm Iref_{\it i} = \frac{I_r}{2^{i+1}} + \sum_{k=1}^{i} B_k \cdot \frac{I_r}{2^k}, \quad i = 1\text{–}7 \tag{1}$$

where I_r represents the current reference and $0 \le I_{\rm in} \le I_r$. $\rm Iref_{\it i}$ is subtracted from I_i by directly connecting the corresponding nodes. Then the resultant current I_i-$\rm Iref_{\it i}$ is sent to the current comparator of the next pipelined stage. After $\rm Iref_{\it i}$ is generated, the output current I_i' and the resultant current I_i-$Iref_i$ are sent to the following stage. The above description establishes that the A/D conversion process can be implemented by the architecture presented in Fig. 2. After complete conversion, $I_{\rm in}$ can be expressed by the output digital bits as

$$\begin{aligned} I_{\rm in} &= B_1\frac{I_r}{2} + B_2\frac{I_r}{4} + \cdots + B_8\frac{I_r}{2^8} \\ &= I_r(B_1 \cdot 2^{-1} + B_2 \cdot 2^{-2} + \cdots + B_8 \cdot 2^{-8}). \end{aligned} \tag{2}$$

Notably, the $\rm CM_{\it i}$ path allows the input current to propagate throughout the pipelined stages without sampling or holding operations during the implementation of the wave-pipelined structure.

Fig. 3 details the structure of the proposed FWP-IADC. Three separate signal paths, paths A, B, and C, are identified to explain the control of the timing of the wave-pipelined structure. Path A is the analog propagation path. It includes a $\rm CM_{\it i}$ stage. The $\rm CM_0$ stage has two current mirror circuits since the $\rm CM_0$ stage is used only to reproduce the input current $I_{\rm in}$ as I_0 and I_0', as shown in Fig. 4. In Fig. 4, the other $\rm CM_{\it i}$ stages are composed of an analog delay element and a current mirror. The analog delay elements are inserted into path A to provide a suitable delay for the analog signals, since the analog signals must be synchronized with the signal of path B to perform a correct subtraction.

Path B includes current-mode sub-DACs, CCMPs, and DFFs. In path B, the DFF latches the output of the current comparator, which is then sent to the subsequent sub-DAC. The DFF is needed to equalize the delay of path B in each stage because the comparison time of the current comparator depends on the amplitude of the input signal. The equally delayed clock signal from path C controls the DFF. Thus, the DFF can latch the data during the identical period.

Path C is the path along which the digital signals propagate through the digital delayed elements (DD). The input signals $B_1, \ldots,$ and B_{i-1} are sent into the ith DAC through the digital delay elements in path C. After the final stage, all the digital bits can be sent out in parallel.

In general, the analog data paths A and B in Fig. 3 dominate the propagation delay in each stage. The characteristics of the signals in paths A and B must be detailed to determine the maximum speed of the proposed FWP-IADC. In particular, two practical considerations related to path A must be addressed in

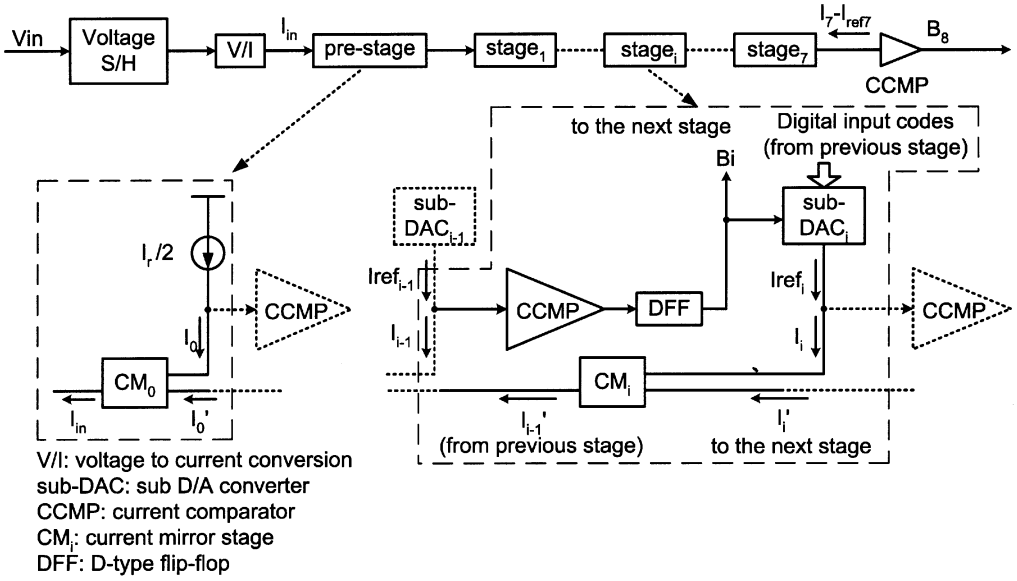


Fig. 2. Conceptual block diagram of the proposed 8-b wave-pipelined IADC.

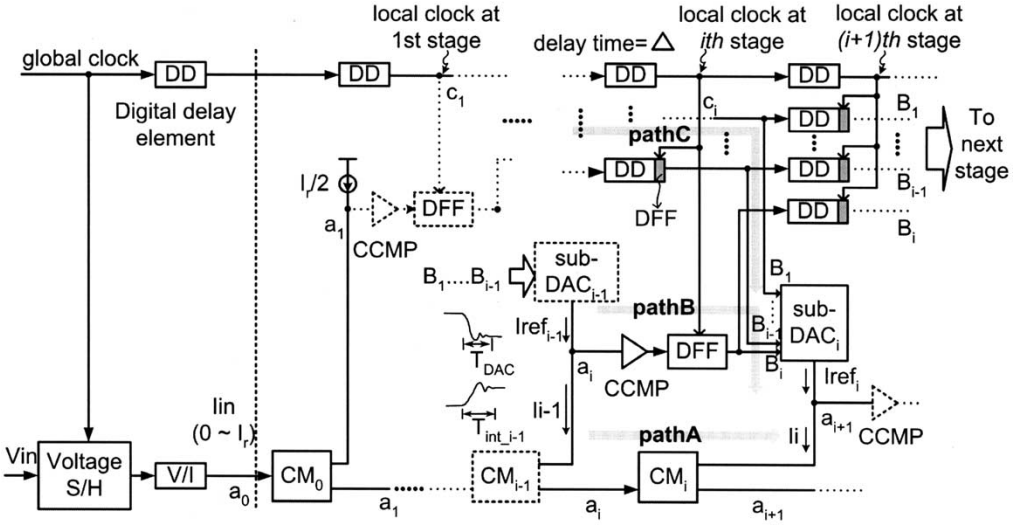


Fig. 3. Detailed structure of the wave-pipelined IADC.

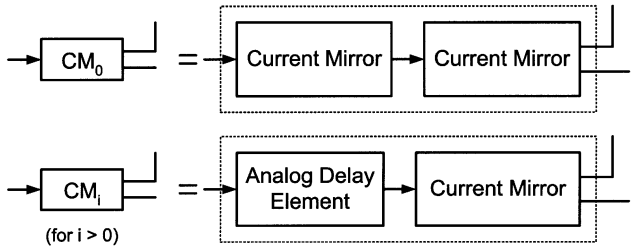


Fig. 4. Function block of the CM block.

a real design. One is the rise/fall time of current signals in every CM_i stage. The other is the intrinsic delay of a current mirror.

Fig. 5(a) shows the structure of path A in the FWP-IADC with CM_0 and three identical CM_i stages. The current signal I_i is the output current signal of the CM_i stages, where i is between 0 and 3. Fig. 5(b) and (c) shows the output current waveforms of the CM_i stage when the swings of the input current signals are full scale and LSB scale, respectively. In Fig. 5(b) and (c), Td_a is the delay between when I_i and I_{i+1} start to rise from the initial zero value. Td_{bf} and Td_{bl} are the delays between when I_i and I_{i+1} settle to their final values in full scale and LSB scale swing, respectively. As the figures indicate, the rise times of the current signals that propagate through each CM_i stage are increased. Therefore, the delay times Td_{bf} and Td_{bl} do not equal Td_a. However, neither Td_{bf} nor Td_{bl} vary among stages because the increased rise/fall time is the same in every stage. Moreover, if the swing of the input current is smaller, then Td_b is closer to Td_a. According to Fig. 5(b) and (c), Td_{bf} and Td_{bl} represent the two extreme cases. Td_{bf} is the maximum delay, whereas Td_{bl} is the minimum.

The intrinsic delay of the current mirror is one of the factors that limits the speed. In the CM_i stage, when the input current signal of the final current mirror changes from the present value to the next value, the output current I_i follows the change of the input current. The output current signals I_i take the rise/fall

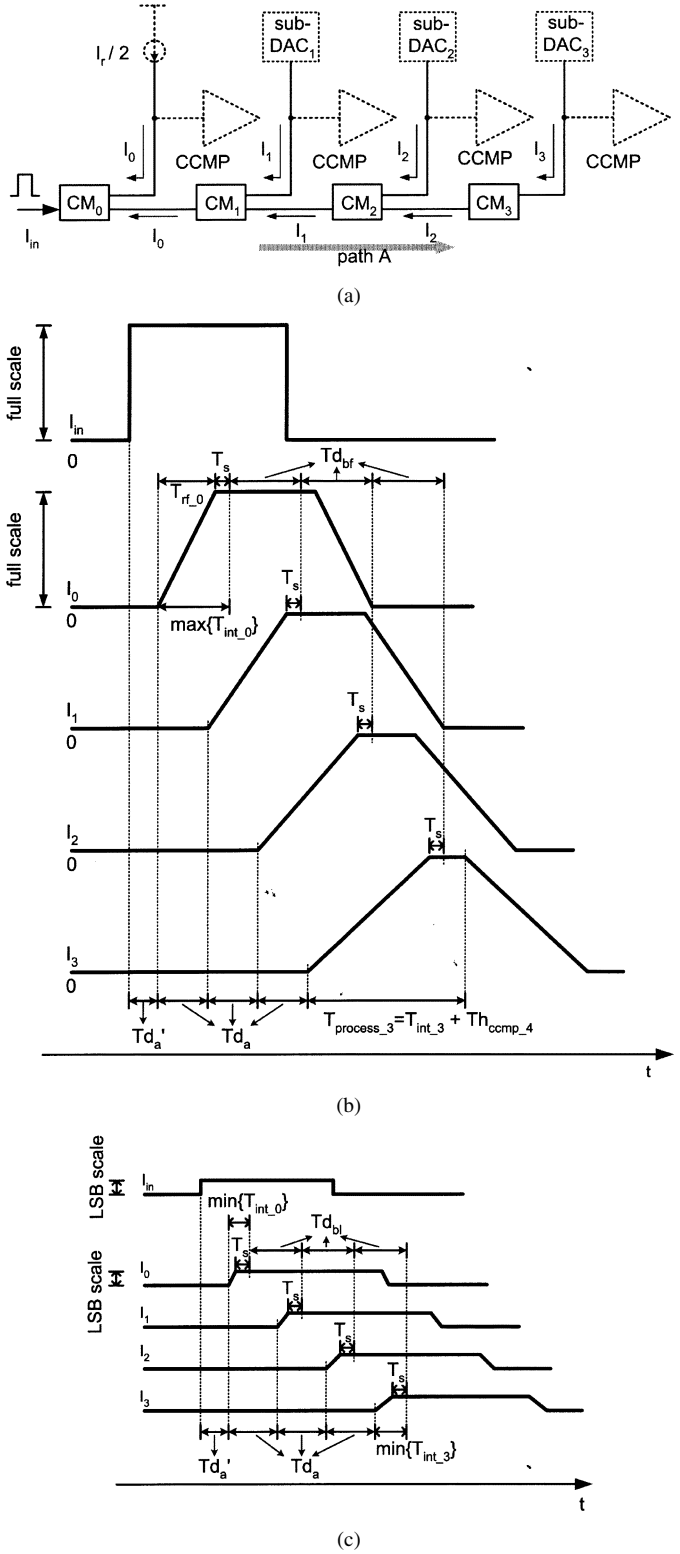


Fig. 5. (a) Four-stage example of the wave-pipelined structure. (b) Output current waveforms of the CM_i stage for full-scale input swing. (c) Output current waveforms of the CM_i stage for LSB scale input swing.

time (T_{rf_i}) plus the settling time (T_s) to reach their final stable value. During this period, the input current signal of the current mirror cannot be changed. Consequently, the time for which the input current signal must be held constant can be defined as the intrinsic delay T_{int} of the current mirror. Hence, the intrinsic delay T_{int_i} of the current mirror in the CM_i stage can be written as follows:

$$T_{\mathrm{int}\_i} = T_{\mathrm{rf}\_i} + T_s, \qquad i = 0 \sim 3. \tag{3}$$

Notably, T_{rf_i} increases with i and T_s is constant in each stage. Moreover, the intrinsic delay T_{int_i} is maximum and minimum when the input swing is full and LSB scale, respectively. The intrinsic delay of a current mirror exceeds that of a simple logic gate since the circuit of a current mirror is more complicated than that of a logic gate and the required accuracy of the output signal in the current mirror is higher. From Fig. 5(b), the relationships among the maximum T_{int_i} in each CM_i stage can be explained as follows:

$$Td'_a + \max\{T_{\mathrm{int}\_0}\} + Td_{bf} = Td'_a + Td_a + \max\{T_{\mathrm{int}\_1}\}. \tag{4}$$

This equation can be extended to general form as

$$\begin{aligned} Td_a + \max\{T_{\mathrm{int}\_i}\} + Td_{bf} &= Td_a + Td_a + \max\{T_{\mathrm{int}\_i+1}\} \\ \max\{T_{\mathrm{int}\_i}\} &= \max\{T_{\mathrm{int}\_i+1}\} \\ &\quad - (Td_{bf} - Td_a), \quad i = 0 \sim 3. \end{aligned} \tag{5}$$

From Fig. 5(c), the following equation is valid for minimum T_{int_i}:

$$\min\{T_{\mathrm{int}\_0}\} + 3Td_{bl} - \min\{T_{\mathrm{int}\_3}\} = 3Td_a. \tag{6}$$

As shown in Fig. 3, the output currents I_i of the CM_i stages are subtracted from the output current $I\mathrm{ref}_i$ of the sub-DAC in the ith stage and the residue current is sent into the current comparator of the next stage. Thus, the output current signal of the CM_i stage after the settling down must be held constant for the process of comparator. The total processing time T_{process_i} of the last current mirror in each CM_i stage can be defined as follows:

$$T_{\mathrm{process}\_i} = T_{\mathrm{int}\_i} + Th_{\mathrm{ccmp}\_i+1}, \qquad i = 0 \sim 3. \tag{7}$$

In (7), Th_{ccmp_i+1} is the input signal hold time of the current comparator in the $(i+1)$th stage.

In Fig. 5(b), only the total processing time T_{process_3} of the final current mirror in the CM_3 stage is shown. T_{int_i} increases with i since T_{rf_i} increases with i. At the final stage, Th_{ccmp} is the maximum because the input signal of the current comparator is less than 1 LSB. Thus, T_{process_3} has the largest value because both T_{int_i} and Th_{ccmp} have the maximum value in the example of four wave-pipelined stages.

According to the above discussion, the space-timing diagram of the analog data path A can be drawn and shown in Fig. 6(a). The vertical axis represents the data depth in path A and the labels a_i and c_i indicate the corresponding nodes in Fig. 3. The boundaries of the shaded regions in Fig. 6(a) depict the flow of data through the data path A under the minimum delay case and worst delay case. Thus, the shaded regions of each data processed at nT_{clk} for $n = 0, 1, \ldots$ must not overlap one another and the minimum required time spacing is Th_{ccmp_4} and $\min\{T_{\mathrm{int}\_3}\}$ so that the previous datum remains unchanged during the period Th_{ccmp_4} to protect the correct functioning

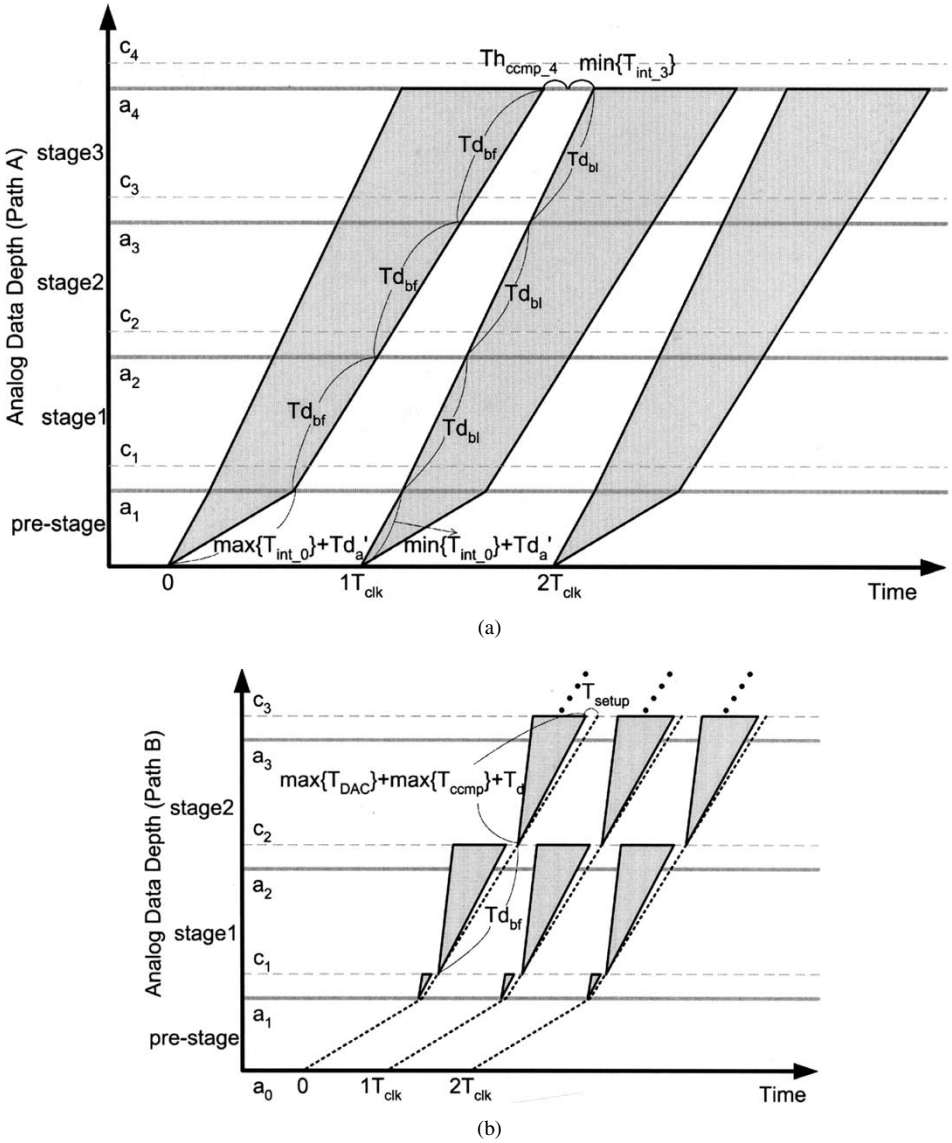


Fig. 6. (a) Space-timing diagram of the analog data path A. (b) Space-timing diagram of the analog data path B.

of the comparator, whereas the next LSB-swing datum requires $\min\{T_{\text{int\_3}}\}$ time to set up. This constraint is expressed as

$$T_{\text{clk}} + \min\{T_{\text{int\_0}}\} + Td'_a + 3Td_{bl} - \min\{T_{\text{int\_3}}\} \geq \max\{T_{\text{int\_0}}\} + Td'_a + 3Td_{bf} + Th_{\text{ccmp\_4}} \quad (8)$$

where T_{clk} is the global sampling clock period. Substituting (6) into (8) yields T_{clk} as

$$T_{\text{clk}} \geq \max\{T_{\text{int\_0}}\} + Th_{\text{ccmp\_4}} + 3(Td_{bf} - Td_a). \quad (9)$$

In (9), the first term on the right-hand side is contributed by the maximum intrinsic delay time of the final current mirror in CM_0 stage. The second term is associated with the hold time of the input signal of the current comparator after stage 3. The third term is related to the different rise/fall times of the output currents among the CM_i stages. If the rise/fall times of the output current are same for every CM_i stage, the third term can be set to zero. Therefore, the minimum value of T_{clk} is limited by the maximum value of intrinsic delay of the current mirror and the hold time of the current comparator. Furthermore, substituting (5) and (7) into (9) yields T_{clk} in the following form:

$$T_{\text{clk}} \geq \max\{T_{\text{process\_3}}\}. \quad (10)$$

Therefore, the maximum speed of the global clock of path A in the proposed FWP-IADC is limited by the maximum total processing time of the last current mirror in the final CM_i stage because the rise/fall time of the output current of the CM_i stage gradually increases from stage to stage.

As may be seen from Fig. 5(b), Td_{bf} is the maximum delay between stages CM_i and CM_{i+1} in path A. In path B of Fig. 3, the current comparator CCMP, DFF and the ith sub-DAC must generate the output current $I\text{ref}_i$ during Td_{bf}. In the final stage, the delay time T_{DAC} of the sub-DAC is maximum since the changing swing of the output current $I\text{ref}_i$ in the ith sub-DAC

is closer to the swing of the input current of the ADC than the one of sub-DAC in previous stage. The current comparator also has the maximum comparison time $T_{\rm ccmp}$. Thus, in path B, the global sampling clock period $T_{\rm clk}$ and the maximum delay Td_{bf} must be satisfied by the following relation:

$$T_{\rm clk} \geq Td_{bf} \geq \max\{T_{\rm DAC}\} + \max\{T_{\rm ccmp}\} + T_d + T_{\rm setup} \tag{11}$$

where T_d and $T_{\rm setup}$ are the delay time and the setup time of the DFF, respectively. Fig. 6(b) shows the space-timing diagrams of path B. Fig. 6(b) shows a data depth of only three stages. The dashed lines indicate the clock delay through the clock delay unit. Clearly, the process of the sub-DAC, the comparison of the current comparator, and the delay of the DFF must be accomplished during time Td_{bf}.

The clock and digital data delay time Δ of the digital path C in Fig. 3 must equal Td_{bf}, because the digital data are aligned by the DFF that is controlled by the local clock. In general, the digital delay elements can be implemented easily. Therefore, path C is not critical to the design of the FWP-IADC.

The maximum global sampling rate of FWP-IADC is decided according to (9) and (11). If path B, as given by (11), dominates $T_{\rm clk}$, then a suitable number of current mirrors must be inserted into the analog delay elements in each $\rm CM_{\it i}$ stage to increase the delay time Td_{bf} and satisfy (11). If the overall delay in path B is smaller than that in path A in (9), then (9) determines $T_{\rm clk}$ and the number of current mirrors in analog delay elements can be decreased. In the extreme case, only two current mirrors in each $\rm CM_{\it i}$ stage are required. In this case, the term (Td_{bf}-Td_a) can be reduced and the maximum sampling rate is increased.

The proposed FWP-IADC can also be designed in multibits per stage to decrease the total number of $\rm CM_{\it i}$ stages. According to (10), the sampling rate can be further increased by reducing the total number of $\rm CM_{\it i}$ stages. Furthermore, the redundant digital bits can be used to implement the digital error correction function in the structure of multibits per stage.

The results of the above analysis reveal that the proposed FWP-IADC architecture has several advantages. First, the efficiency of timing usage is improved. In the conventional switched-current pipelined structure [12]–[15], the half of the period $T_{\rm clk}$ is required to track signals, whereas the other half of this period is used to hold the signal. If the tracking time does not equal the holding time, then the efficiency of timing usage is poor. However, in the proposed FWP-IADC structure, the entire clock period is used for signal processing. Timing is used efficiently. Second, the signal path includes no switched-current circuits. The proposed FWP-IADC eliminates the nonlinearity factor that is contributed by the switched-current circuits from the signal path. Third, the number of controlled clocks in the FWP-IADC is reduced. Finally, the proposed FWP-IADC can accept a high-frequency input signal since the voltage S/H circuits are used ahead of the V/I conversion circuit.

B. Indirect Transfer WP-IADC (ITWP-IADC)

As may be seen from (10), if path A is the critical path in the FWP-IADC, then the total processing time of the last current mirror in the final stage limits the sampling rate of the FWP-IADC. The wave-pipelined stages of FWP-IADC can be divided into several wave-pipelined sections to increase the sampling rate. The input data of each section is controlled by the delay clock. Such an architecture is called the indirect transfer WP-IADC (ITWP-IADC). Fig. 7(a) shows the structures of current-mirror wave-pipelined sections in the ITWP-IADC. Four CM stages are divided into two current-mirror wave-pipelined sections. In Fig. 7(a), one section consists of $\rm CM_0$ and $\rm CM_1$, whereas the other section consists of $\rm CM_2$ and $\rm CM_3$. The function block of the $\rm CM_2$ stage is the same as that of the $\rm CM_0$ stage presented in Fig. 4. The input current of the $\rm CM_2$ is not taken directly from $\rm CM_1$, but from the switched-current cells. Fig. 7(b) shows the space-timing diagram of the ITWP-IADC in Fig. 7(a). As shown in Fig. 7(a), the first datum is sent into the first wave-pipelined section and switched-current cell 1 during the period when $\phi_1 = 1$. The first datum is continually propagated through the wave-pipelined path for data conversion and it is also stored in switched-current cell 1. During ϕ_2, the second datum is sent into the first wave-pipelined section for processing and it is stored in switched-current cell 2. A similar operation is performed for each datum from 1 to n. When $\phi_n = 1$, the nth datum is sent into the first wave-pipelined section and stored in switched-current cell n. At this time, the slowest data is about to reach the final current-mirror stage and the stored first datum in switched-current cell 1 must be sent into stage $\rm CM_2$ of the second wave-pipelined section to continue the wave-pipelined operation during ϕ_1', where ϕ_1' is the delay clock of ϕ_1. Therefore, the first datum is aligned at time $t_{\rm align}$ by switched current cell 1 and sent into the second wave-pipelined section, as shown in Fig. 7(a) and (b).

In the case of the maximum sampling rate, the ITWP-IADC needs enough switched-current cells to store the input data. Thus, the following constraint must be satisfied, as shown in Fig. 7(a):

$$nT_{\rm clk} \geq t_{\rm align} + \frac{1}{2}T_{\rm clk} \tag{12}$$

where $T_{\rm clk}$ is the minimum clock period. Meanwhile, $t_{\rm align}$ must satisfy the following constraint to guarantee the successful operation, as shown in Fig. 7(b):

$$\max\{T_{\rm int\_0}\} + Td_a' + 2Td_{bf} \leq t_{\rm align} + \max\{T_{\rm int\_0}\} + Td_a'.$$

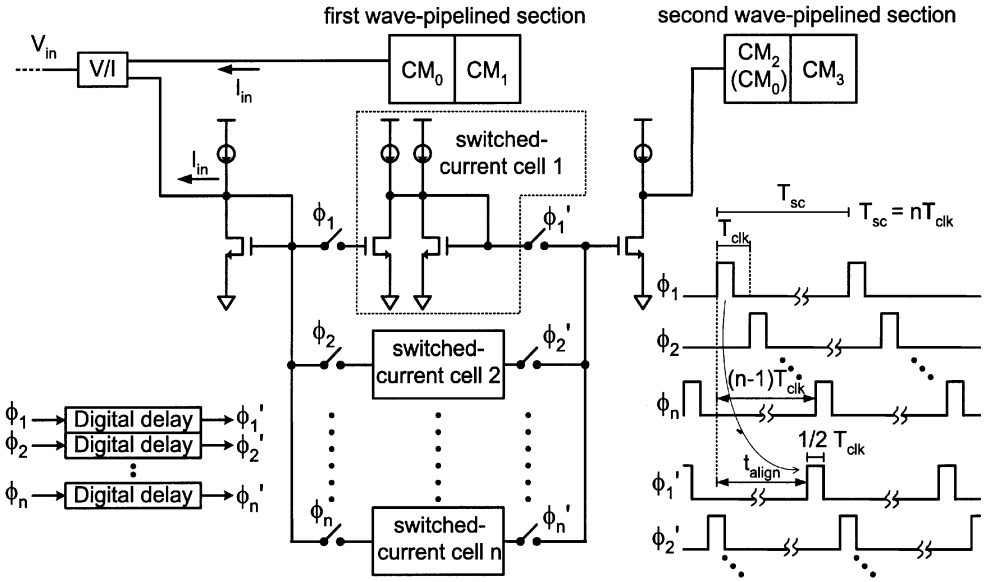
Thus,

$$t_{\rm align} \geq 2Td_{bf}. \tag{13}$$

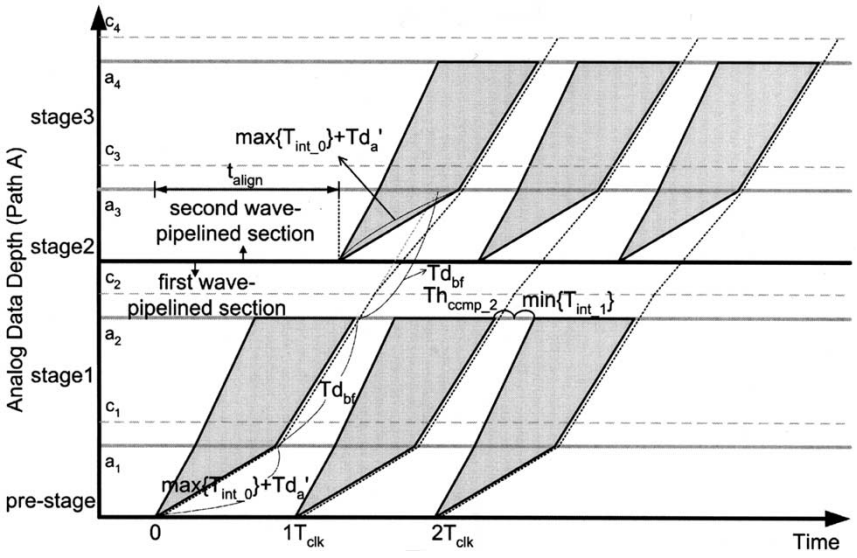
According to (12) and (13), the range of aligned time $t_{\rm align}$ and the number n of the switched-current cells can be obtained as

$$\left(n - \frac{1}{2}\right) T_{\rm clk} \geq t_{\rm align} \geq 2Td_{bf},$$
$$n \geq \frac{2Td_{bf}}{T_{\rm clk}} + \frac{1}{2} \quad n \text{ is integer} \tag{14}$$

where $T_{\rm clk}$ represents the minimum clock period. After the number n of switched-current cells and $t_{\rm align}$ are determined, the required delay elements with a delay of $t_{\rm align} - 2\,Td_{bf}$ can be inserted in path C to control the sub-$\rm DAC_2$.



(a)



(b)

Fig. 7. (a) The simplified block diagram of the two-section ITWP-IADC for 4 CM stages. (b) The space-timing diagram of the two-section ITWP-IADC for 4 CM stages.

Accordingly, the longest data path A reduces to two CM stages in the 4-b example. $T_{\rm clk}$ is decreased from $T_{\rm process\_3}$ to $T_{\rm process\_1}$ in a two-section ITWP-IADC. Therefore, speed can be increased using the two-section ITWP-IADC in four CM stages.

Applying the same principle, the four CM stages in a two-section ITWP-IADC can be extended to eight CM stages, as shown in Fig. 8. Each section includes four CM stages. The current input to the $\rm CM_4$ stage does not directly come from the previous $\rm CM_3$ stage, but from the switched-current cells. Meanwhile, the function block of $\rm CM_4$ is the same as the one of $\rm CM_0$ shown in Fig. 4. Thus, the sampling clock $T_{\rm clk}$ can be reduced to $T_{\rm process\_3}$ in the two-section ITWP-IADC for the 8-b example; $T_{\rm process\_3}$ is smaller than $T_{\rm process\_7}$ in FWP-IADC. Furthermore, the wave-pipelined stage can be further divided into four sections. Each section has two CM stages, just like the section in Fig. 7(a). Thus, the sampling clock $T_{\rm clk}$ can further reduce to $T_{\rm process\_1}$ in the four-section ITWP-IADC; $T_{\rm process\_1}$ is smaller than $T_{\rm process\_3}$ in the two-section ITWP-IADC for the 8-b example.

According to the timing diagram of ITWP-IADC in Figs. 7(a) and 8, the period $T_{\rm sc}$ of the switched-current cell equals $nT_{\rm clk}$. Thus, the switched-current cells have enough time to satisfy the demand for accuracy and speed. Moreover, only a few switched-current cells are present in the overall data path of ITWP-IADC to degrade the linearity. Consequently, the linearity is expected to be better than that in the conventional pipelined IADC. Besides, the error generated by the current mirror does not accumulate through the total CM stages in ITWP-IADC. Therefore, less accuracy can be required of the current mirror in ITWP-IADC than of that in FWP-IADC.

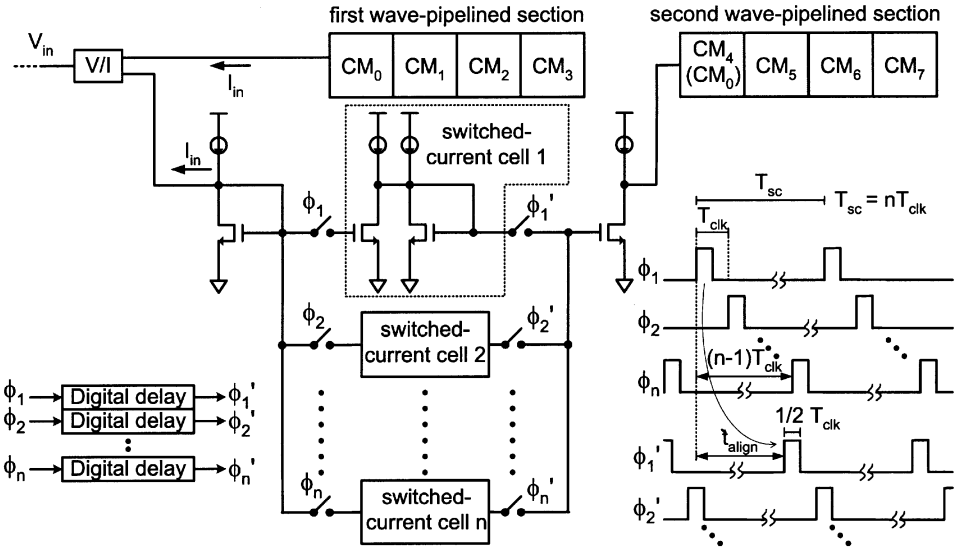


Fig. 8. Simplified block diagram of the two-section ITWP-IADC for eight CM stages.

III. Circuit Implementation and Simulation Results

To further verify the proposed new architectures of full wave-pipelined IADC (FWP-IADC), CMOS circuits are used to implement the ADC as a demonstrative example. The current mirror is a basic component in the proposed new architectures for the FWP-IADC. It acts as a current conveyer, an inverter, and an analog delay element. Accordingly, the design of the current mirror is crucial. Generally, high output impedance is required in the current mirror to reduce the gain error. Fig. 9(a) shows the adopted current mirror circuit with the enhanced output impedance, as proposed by Säckinger *et al.* [23]. As shown in Fig. 9(a), the capacitances C1 and C2 are added to reduce the ripple phenomenon of the input current. The MOSFETs M9, M10, M11 and M12, with their associated current sources I_{B1}, I_{B2}, I_{B3}, and I_{B4} are common-source amplifiers that provide negative feedback to the cascoded devices M1, M3, M6, and M8, respectively, and increase the output resistance of the current mirror. Assuming that the output resistances of current sources I_{B2} and I_{B4} are approximately r_{ds10} and r_{ds12}, respectively, the final output resistance can be written as

$$r_{\text{out}} = \frac{g_{m3}g_{m10}r_{ds3}r_{ds4}r_{ds10}}{2} \parallel \frac{g_{m8}g_{m12}r_{ds8}r_{ds7}r_{ds12}}{2}. \tag{15}$$

Moreover, if the current mirror circuits are perfectly symmetrical, the frequency response of current mirror can be derived as

$$H(s)=\frac{I_{\text{out}}}{I_{\text{in}}}(s)=\frac{1}{\left(1+s\frac{C_g}{g_{m1}g_{m2}g_{m9}r_{ds9}r_{ds2}}+\frac{1}{2}s^2\frac{C_{x1}C_g}{g_{m1}g_{m2}}\right)} \tag{16}$$

where $C_{x1} = C_{gs1} + C_{gd9}$ and C_g is the total capacitance including parasitic capacitance from node A to ground in Fig. 9(a). As may be seen from (16), the current gain is unity at low frequency with $s \cong 0$. The step response $h(t)$ of the current mirror can be obtained by the inverse Laplace transformation of $1/sH(s)$ as

$$h(t) = \left[1 - e^{-t/a}\left(\cos ct + \frac{\sqrt{C_g}}{b}\sin ct\right)\right]u(t) \tag{17}$$

where

$$\begin{aligned} a &= g_{m9}r_{ds9}r_{ds2}C_{\times 1} \\ b &= \sqrt{-C_g + 2{g_{m9}}^2 g_{m1}g_{m2}{r_{ds9}}^2{r_{ds2}}^2 C_{x1}} \\ c &= (b/a\sqrt{C_g}). \end{aligned}$$

From (17), it can be seen that the constant a is the most critical factor on time response. If a is decreased, the time response of current mirror can be improved. To decrease the value of a, C_{gs1} and C_{gs3} in M_1 and M_3, respectively, should be kept small.

In the FWP-IADC, the current signal through the eight CM stages should have 8-b accuracy given a suitably designed device size. From HSPICE simulation results, the output resistance of current mirror is about 3 kΩ. The HSPICE-simulated intrinsic delay of the final current mirror in a CM stage with eight current mirrors is about 48 ns when the input signal is of full scale. Since the current signal only propagates through four (two) CM stages in a two (four)-section ITWP-IADC, the accuracy demand of ITWP-IADC can be relaxed as compared with that in FWP-IADC. After the current mirror circuits are resized, the intrinsic delay of the final current mirror is about 17 ns in the two-section ITWP-IADC when the input signal is of full scale from 0 to 128 μA, as may be seen from the simulated waveforms in Fig. 9(b). Fig. 9(c) shows the output waveforms of stage CM_i when the swing of the current input signal varies from 54 to 74 μA. It is the maximum swing of the input signal when the sampling rate is 166 MS/s and input frequency is 8 MHz. In Fig. 9(c), the four-section ITWP-IADC is adopted and each CM_i stage consists of two current mirrors. The intrinsic delay of the last current mirror can be decreased to 5 ns, as shown in Fig. 9(c).

Fig. 10(a) and (b) presents the circuit diagrams of current-mode sub-DACs. All sub-DACs are implemented using the current steering structure. From Fig. 10(a), the sub-DAC_1 is a 1-b DAC, which is composed of three identical current sources with magnitudes of $I_r/4$. Two current sources are switched by the control signal B_1, which is the result of conversion of the first stage. If $B_1 = 1(= 0)$, then the two current sources

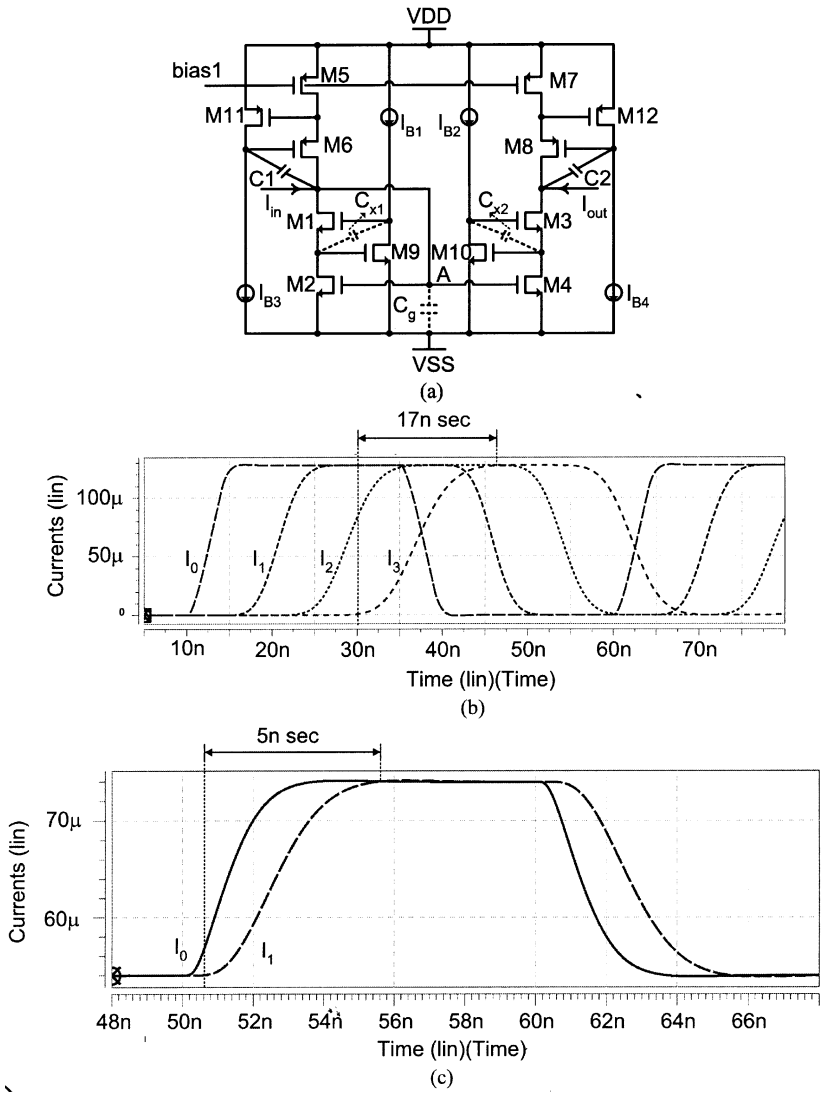


Fig. 9. (a) Enhanced output-impedance current mirror. (b) The simulated output current waveforms of the CM_i stage in a two-section ITWP-IADC structure with full-scale step input current from 0 to 128 μA. (c) The output current waveforms of the CM_i stage in a four-section ITWP-IADC structure with nonfull-scale step input current of 20 μA.

are switched to $I\mathrm{ref}_1$ (GND) to make $I\mathrm{ref}_1 = 3/4I_r(1/4\ I_r)$. The sub-$\mathrm{DAC}_2$ is a 2-b DAC and the two bits are linearly decoded to become the thermometer code. The ith sub-DAC has a $2 + (i - 2)$ segmented architecture for $i \geq 3$, as shown in Fig. 10(b). In this DAC, the two most significant bits (MSBs) are linearly decoded whereas the rest of the bits are binary weighted. Using $2 + (i - 2)$ segmented architecture greatly reduces the transition time and the glitch problem of the DAC. Furthermore, the threshold-voltage compensation technique [24] and the cascode structure are used to implement the reference current source I_{ref} to ensure accuracy. Fig. 10(c) shows the output transition curve of the seventh DAC from 0.5 to 127.5 μA in the worst case. It takes 6 ns to settle down to the final stable value with 8-b accuracy.

Fig. 11(a) shows the low-input-impedance current comparator circuits [3], [14]. Node B must be connected to dummy MOS transistors, as indicated in Fig. 11(a), since the proposed WP-IADCs have single-ended structures. The input impedance can be reduced greatly since transistors M5 and M1 provide negative feedback. Moreover, the input current can be amplified by the current mirror M1/M3 and PMOS latch. The regeneration characteristics of the PMOS latch improve the speed performance.

Because the input impedance of current comparator is the loading of current mirror and DAC circuits, the low-input-impedance of current comparator circuit can reduce the RC time delay. In Fig. 11(a), the input impedance can be derived by the small-signal model

$$Z_{\mathrm{in}}(s) = \frac{\frac{1}{r_{ds5}} + \frac{1}{r_{ds7}} + sC_{g13}}{g_{m1}g_{m5} + sC_{g13}\left(\frac{1}{r_{ds1}} + \frac{1}{r_{ds5}} + g_{m5}\right)} \tag{18}$$

where C_{g13} is the total capacitance including parasitic capacitance from node C to ground in Fig. 11(a). To obtain a low input resistance at low frequency, large g_{m1}, g_{m5}, r_{ds5}, and r_{ds7} are required. From the HSPICE simulation results, the input resistance of the current comparator is about 150 Ω at low frequency.

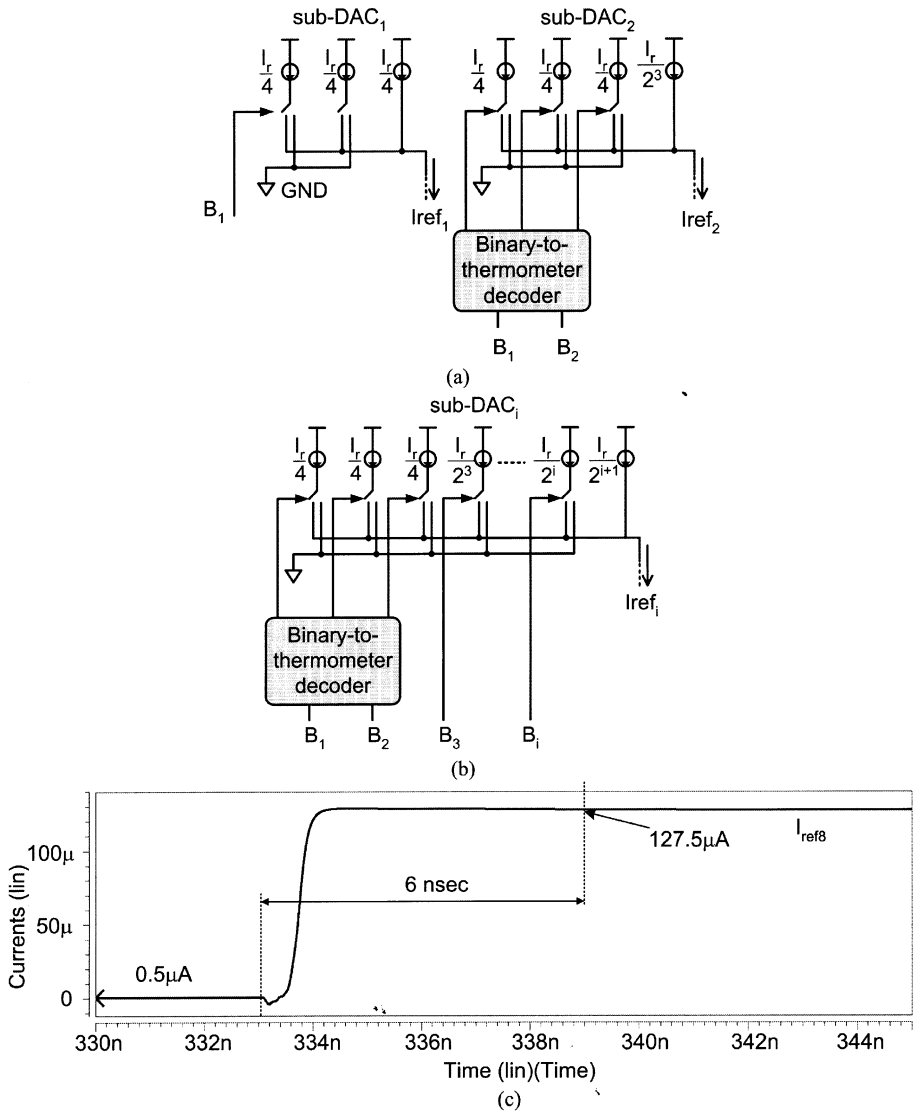


Fig. 10. (a) Second and third current-mode sub-DACs. (b) The ith sub-DAC. (c) The output transition curve of the 7th DAC.

Generally, the time response of current comparator is related to Z_{in}, the time response of the preamplifier circuits M1–M8 in Fig. 11(a), and the time response of the PMOS latch. The step response of the preamplifier can be derived as

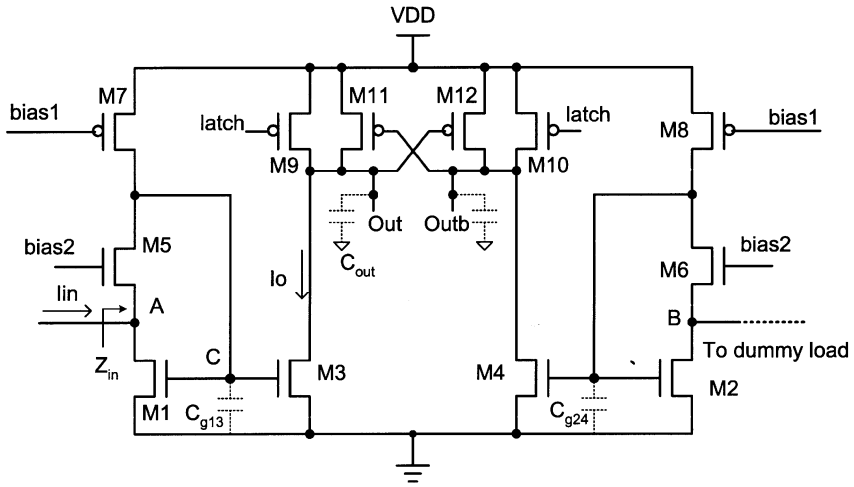
$$h(t) \equiv \frac{Io}{I_{\text{in}}}(t) = \left(\frac{g_{m3}}{g_{m1}} - \frac{g_{m3}}{g_{m1}} e^{(-t/C_{g13}/g_{m1})}\right) u(t). \quad (19)$$

From (19), the time response of the preamplifier can be improved by reducing the capacitance C_{g13}. The time response of the PMOS latch can be characterize by the output voltage change versus time with the major factor as $e^{(g_{m11}t/C_{\text{out}})}$. Thus, reducing the output capacitance C_{out} and increasing g_{m11} can improve the speed performance. According to the HSPICE simulation results, the current comparator takes 1.6 ns to amplify an input current of 2 nA.

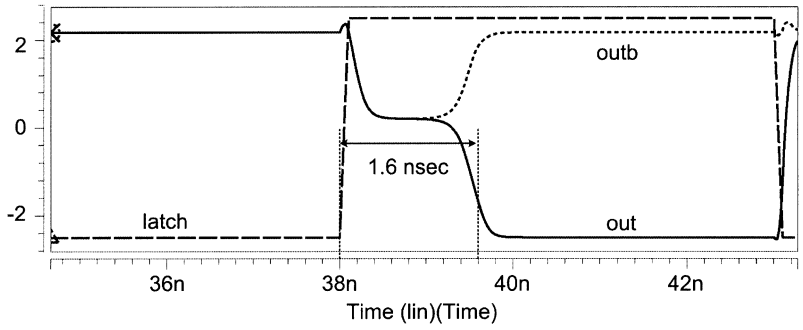
In the ITWP-IADC, the switched-current cells with the clock feedthrough errors cancellation technique as proposed by Sugimoto [25] are used. For switches, the complementary (NMOS and PMOS) and dummy switches are adopted. Since the switched-current cells in the ITWP-IADC have relaxed timing requirement, other cell circuits could also be used to satisfy both accuracy and speed requirements.

The speed performance of the FWP-IADC and ITWP-IADC can be obtained from the HSPICE simulation. In the 8-b example, the sampling rate of FWP-IADC and the two-section ITWP-IADC can achieve to 20 and 54 MHz, respectively, under Nyquist rate sampling. If the two-section ITWP-IADC does not use Nyquist rate sampling, a sampling rate of 80 MHz can be achieved when the frequency of the input signal is 4 MHz. In the four-section ITWP-IADC case, a sampling rate of 133 MHz can be achieved at an input frequency of 6.25 MHz. The increased sampling rate is due to the nonfull-scale input currents that reduce the intrinsic delay of the last current mirror.

If the delay time of path B can be reduced such that the path can become noncritical, then the total number of current mirrors in stage CM_i can be reduced to two. Meanwhile, if the intrinsic delay of the last current mirror and the comparator hold time can be reduced to 5 and 1 ns, respectively, then the four-section ITWP-IADC can achieve a sampling rate of 166 MS/s at an input frequency of 8 MHz.



(a)



(b)

Fig. 11. (a) The circuit structure of the low-input-impedance current comparator. (b) The transition characteristic of the current comparator.

TABLE I
COMPARISON OF CMOS CURRENT-MODE PIPELINED ADCs

	Res. (bits)	Architecture	Sample Rate	Technology
[10]	6	8 parallel pipeline ADCs	32 MS/s (4 MS/s per pipeline ADC)	0.8 μm
[11]	8	4 parallel pipeline ADCs	70 MS/s (17.5 MS/s per pipeline ADC)	0.8 μm
[12]	7.43	Pipeline ADC	3 MS/s	0.8 μm
[13]	6.35	Pipeline ADC	15 MS/s	0.8 μm
[15]	6.1	32 parallel pipeline ADCs	4 GS/s (125 MS/s per pipeline ADC)	0.35 μm
This work	8	4 - section ITWP - IADC	133 MS/s - 166 MS/s	0.35 μm

In Table I, the performance of the ITWP-IADC is compared with that of other known CMOS current-mode pipelined ADCs. It can be seen from that the ITWP-IADC has the superior speed performance.

IV. EXPERIMENTAL RESULTS

To demonstrate the feasibility and verify the function, the experimental chip of a full wave-pipelined IADC (FWP-IADC) was designed and fabricated in a double-poly quadruple-metal 0.35-μm CMOS process. Fig. 12 shows the photograph of the fabricated experimental chip. For testing, the voltage S/H circuit was not included in the whole chip, so the performance limits of the developed architecture could be recognized. Therefore, the arbitrary-waveform-generator must be used to generate the 12-b S/H voltage. The chip was laid out to contain eight wave-pipelined stages. For simplicity, this demonstrative design included neither digital error correction nor calibration circuits. In the experimental chip of the FWP-IADC, the simple current comparator [21] is used.

The sine-wave-based histogram algorithm was used to measure the linearity of the fabricated FWP-IADC. Based on 4-b resolution and operated at a 20-MS/s conversion rate, the DNL and INL for all codes were within $\pm$0.45 LSB and $\pm$1.1 LSB, respectively. The signal-to-noise- and-distortion ratio (SNDR) was measured by taking the fast Fourier transform (FFT)

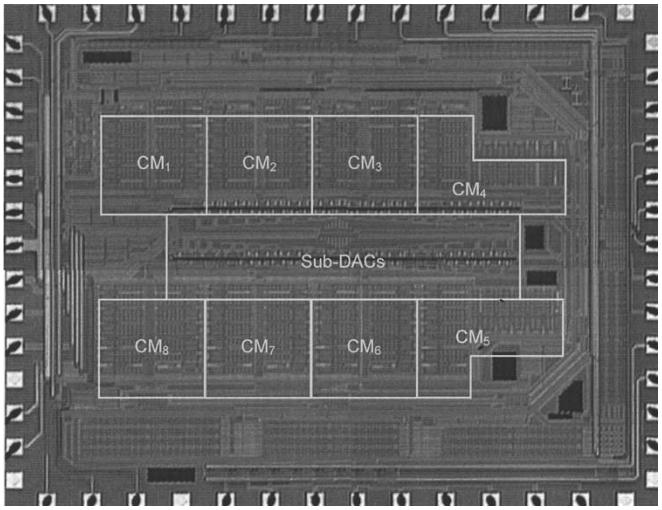
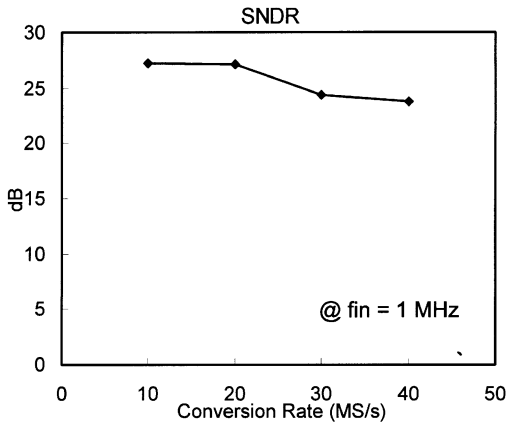
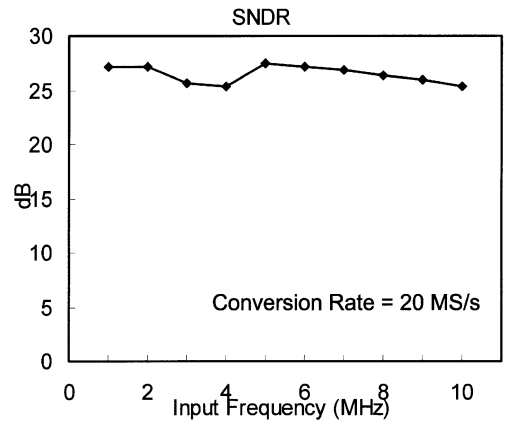


Fig. 12. Photograph of the fabricated chip.



(a)



(b)

Fig. 13. (a) The measured SNDR versus conversion rate of the wave-pipelined IADC for 1-MHz analog input. (b) The measured SNDR versus analog input frequency of the wave-pipelined IADC at a 20-MS/s conversion rate.

on 8192 samples from the output codes of the FWP-IADC. Fig. 13(a) plots the measured SNDR versus the conversion rate for the signal input frequency of 1 MHz. It can be seen that the measured SNDR remains at approximately 27 dB (effective 4.2 b) when the conversion frequency is below 20 MS/s. Furthermore, the measured SNDR decreases to 23.7 dB when the conversion frequency is increased to 40 MS/s. Fig. 13(b) plots the measured SNDR versus the analog input frequency for a full-scale sinusoidal input at 20 MS/s. The SNDR is seen to exceed 25.4 dB when the input frequency is between 1 and 10 MHz. The measured results verify the advantages of high input frequency and Nyquist-rate operation in the proposed architecture of WP-IADCs.

TABLE II
MEASURED WAVE-PIPELINED IADC CHARACTERISTICS

Technology	0.35 μm 2P4M CMOS
SNDR (f_s = 20 MS/s)	27 dB (f_{in} = 1 MHz) 25.4 dB (f_{in} = 10 MHz)
DNL	< ± 0.45 LSB (4-b, f_s = 20 MHz)
INL	< ± 1.1 LSB (4-b, f_s = 20 MHz)
Full Scale Current	0 ~ 128 μA
Unit LSB Current	0.5 μA
Power Dissipation	390 mW
Power Supply	5 V
Chip Area	3.7 × 2.9 mm^2

Table II summarizes the measured characteristics of the example FWP-IADC. The area of the chip (including the I/O pads) is 3.7×2.9 mm^2 and the power consumption is 390 mW, with a 5-V single power supply.

Based on the above experimental and simulation results, the ITWP-IADC with digital error correction circuits, calibration circuits, and precise current comparator will be designed and fabricated to verify the full performance with 133–166 MHz and 8/10-b accuracy in the future.

V. CONCLUSION

In this paper, new architectures of the FWP-IADC and ITWP-IADC are proposed and analyzed for the design of a current-mode analog-to-digital converter (IADC). The novelty lies in the application of wave-pipelined theory to form the wave-pipelined IADCs (WP-IADCs) and improve the speed performance of the IADCs. WP-IADCs offer several advantages, including high-speed performance, high input frequency, more efficient use of timing, relaxation of the clock period of the switched-current cells, and increased linearity by reducing the total number of switched-current cells. The operation timing of WP-IADCs are derived and given in this work. HSPICE simulation results reveal that FWP-IADCs and two-section ITWP-IADCs can achieve sampling rates of 20 and 54 MHz, respectively, under Nyquist rate sampling with 8-b resolution. Moreover, the ITWP-IADC with two wave-pipelined sections can achieve a sampling rate of 80 MHz with 8-b resolution when the frequency of the input signal is 4 MHz. In an 8-b example, the sampling rate of the four-section ITWP-IADC can reach 166 MS/s at an input frequency of 8 MHz.

The proposed FWP-IADC was experimentally verified by a test chip fabricated using 0.35-μm CMOS technology. The measurement results have successfully demonstrated that the proposed design concept and architectures can be applied to the design of future high-speed IADCs. In future work, ITWP-IADC

architectures and digital error correction circuits will be used to implement 8–10-b high-speed WP-IADCs.

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