Performance and Reliability of Low-Temperature Polysilicon TFT With a Novel Stack Gate Dielectric and Stack Optimization Using PECVD Nitrous Oxide Plasma

Kow-Ming Chang, *Member, IEEE*, Wen-Chih Yang, and Chiu-Pao Tsai

***Abstract*—This paper proposes a novel tetraethylorthosilicate (TEOS)/oxynitride stack gate dielectric for low-temperature poly-Si thin-film transistors, composed of a plasma-enhanced chemical vapor deposition (PECVD) thick TEOS oxide/ultrathin oxynitride grown by PECVD N_2O plasma. The novel stack gate dielectric exhibits a very high electrical breakdown field of 8.5 MV/cm, which is approximately 3 MV/cm higher than traditional PECVD TEOS oxide. The novel stack oxide also has better interface quality, lower bulk-trap density, and higher long-term reliability than PECVD TEOS dielectrics. These improvements are attributed to the formation of strong Si $\equiv$ N bonds of high quality ultra-thin oxynitride grown by PECVD N_2O plasma, and the reduction in the trap density at the oxynitride/poly-Si interface.**

***Index Terms*—Dielectric films, gate oxide, nitrous oxide plasma, polycrystalline-silicon thin-film transistor (polysilicon TFT), reliability.**

I. Introduction

LOW-TEMPERATURE poly-Si (LTPS) thin-film transistors (TFTs) have high mobility and driving current, making them highly suited for realizing peripheral circuits on active matrix liquid crystal displays (AMLCDs) glass substrate [1]. However, the traditional LTPS TFTs, which use PECVD SiO_2 or Si_3N_4 as the gate insulator, suffer from high interface trap states, low electrical breakdown field ($<$6 MV/cm) and high gate leakage current [2]. In contrast, PECVD N_2O plasma oxide has been reported to achieve strong Si $\equiv$ N bonds, smooth interface, and excellent charge trapping properties at the oxynitride/poly-Si interface [3]–[5]. However, although N_2O plasma oxide is a good candidate for forming high quality ultra-thin oxide, it is unsuitable for high-voltage LTPS TFTs peripheral driver IC applications. Specifically, the plasma radical oxidation process has difficulty in obtaining a thick and high-quality dielectric film at low oxidation temperature ($\leq$300 °C), because of the self-limiting effect of thermal oxidation [6] and plasma-induced damage [7]. Because of the small breakdown voltage of such thin ($\leq$120 Å) plasma-grown oxide, they cannot be applied as a gate dielectric for making high-voltage TFTs peripheral driving integrated circuits [8], [9]. Therefore, a high-quality low-temperature gate dielectric, capable of sustaining high-voltage operations, needs to be developed for LTPS TFTs peripheral circuit applications embedded in AM-LCDs plates. This work proposes a simple stack gate dielectric structure, based on the continuous stacking of a PECVD N_2O plasma-grown ultra-thin oxynitride film (about 3 nm) together with a thick-TEOS oxide film (37 nm), without breaking the process chamber vacuum. The bottom high-quality ultra-thin oxynitride formed strong Si $\equiv$ N bonds and low charge trapping density at the oxynitride/poly-Si interface. The upper 37-nm TEOS oxide layer solves the high-voltage operation problem in the application of LTPS TFTs peripheral circuits. The experimental results reveal that the electrical breakdown field of the stack oxide is up to 8.5 MV/cm, which is 3 MV/cm larger than that of the traditional single layer TEOS oxide.

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II. Device Fabrication

Amorphous silicon (a-Si) films with thickness of 100 nm were formed on 4-inch thermally oxidized p-type Si wafers by dissociating SiH_4 gas at 550 °C using low pressure chemical vapor deposition (LPCVD). The a-Si films were then prepatterned into active islands, and subsequently crystallized at 600 °C furnace annealing in the N_2 ambient for 24 h. Following surface oxide removal, the 40-nm-thick stack gate dielectric (37 nm TEOS/3 nm oxynitride) film was formed by two-step oxidation processes. First, PECVD N_2O plasma oxidation was performed at substrate temperature 300 °C, chamber pressure 100 mTorr, RF power 200 W and 1 min of processing time to grow the 3-nm thickness of oxynitride, then a 37-nm thickness of PECVD TEOS oxide was continuously deposited *in-situ* on the thin-oxynitride film without vacuum breakup. The process illustration of stack gate dielectric was shown in Fig. 1. To optimize the quality of thin-oxynitride and investigate plasma induced damage, the radio frequency (RF) power 600 W and various N_2O plasma oxidation times were also examined, as summarized in Table I. For comparison, the control sample was comprised a 40–nm thickness of PECVD TEOS oxide without N_2O plasma treatment. Next,

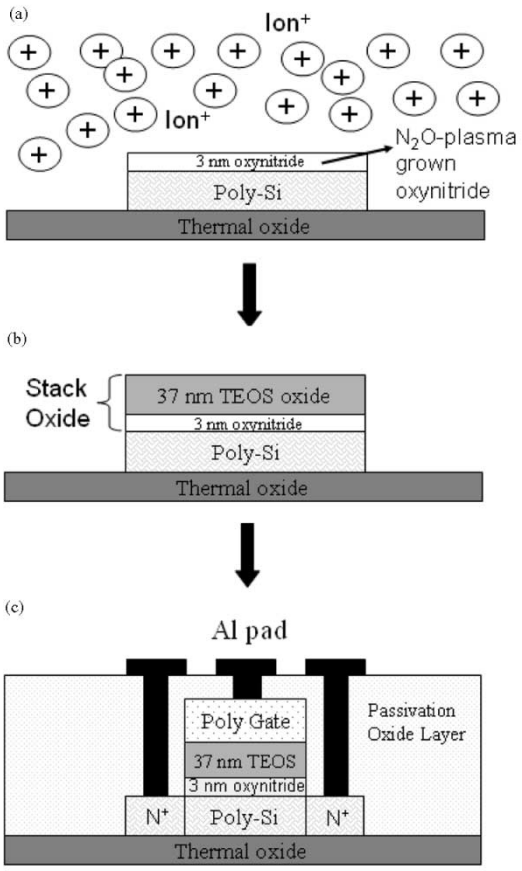

Fig. 1. Schematic process steps for fabrication of poly-Si TFTs with stack gate dielectric. (a) N_2O plasma-grown ultrathin oxynitride film. (b) Deposit thick TEOS oxide film. (c) Low-temperature poly-Si TFT with stack oxide.

TABLE I
DEPOSITION CONDITIONS OF TEOS/N_2O-PLASMA GROWN OXYNITRIDE STACK GATE DIELECTRICS IN THIS PAPER

Stack Oxide Samples	RF Power (Watt)	N_2O-plasma Processing Times (min)	N_2O-plasma Oxynitride Thickness (Å)	TEOS Oxide Thickness (Å)	Total Thickness (Å)
SOTFT-1	200	1	30	370	400
SOTFT-2	200	5	70	330	400
SOTFT-3	600	1	50	350	400
SOTFT-4	600	5	100	300	400

a 200 nm-thick poly-Si was deposited and patterned for the gate electrode. Also, a self-aligned phosphorous implantation was performed at a $5 \times 10^{15}/\text{cm}^2$ dosage and 40 keV energy. Moreover, dopant activation was performed at 600 °C furnace annealing at N_2 ambient for 12 h following the deposition of a 400-nm TEOS oxide passivation layer and contact hole definition. Subsequently, 500-nm Al was deposited and patterned to provide an electrode pad. Al sintering was then carried out at 400 °C for 30 min. These LTPS TFTs devices were fabricated without using hydrogenation plasma passivation treatment to passivate the poly-Si grain boundary or oxide/poly-Si interface. To measure the capacitance-voltage (*C–V*) curve, the stack gate dielectric films were also deposited on p-type Si (100) wafer in the same run, and the *C–V* measurement was performed on this metal-oxide-semiconductor (MOS) capacitor. The thickness of

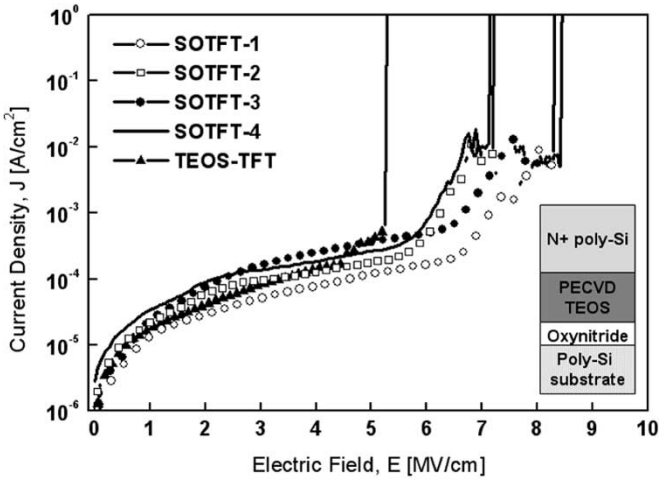

Fig. 2. Current density versus electric field *J–E* characteristics of the gate oxide for the conventional TEOS oxide and proposed stack oxide poly-Si TFTs.

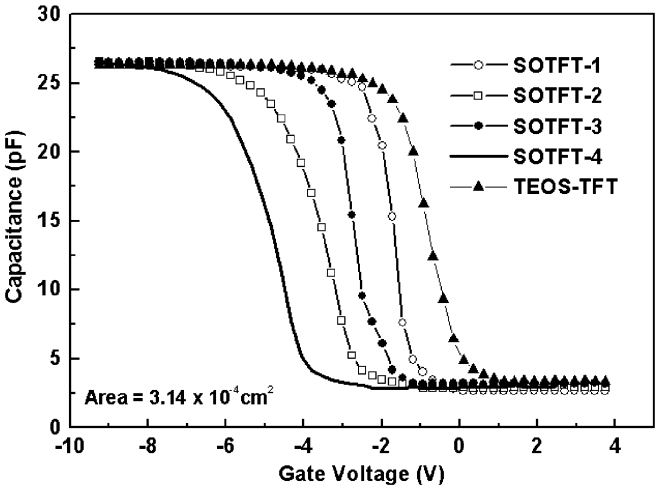

Fig. 3. High-frequency C–V curves of MOS capacitor with TEOS and stack oxide dielectric films. The measurement frequency was 1 MHz.

the stack gate dielectric was measured using an Ellipsometer. The thickness variation of N_2O plasma-grown oxynitride film is below $\pm 5\%$. Finally, the electrical characteristics of LTPS TFTs were analyzed by HP 4156 A semiconductor parameter analyzer.

III. RESULTS AND DISCUSSION

Fig. 2 illustrates the current density versus electric filed characteristics of LTPS TFTs with both TEOS and TEOS/N_2O plasma oxynitride stack oxides under various oxynitride growth conditions. The *J–E* characteristics were measured by applying a voltage to the gate electrode and grounding the source and drain electrodes. The ramp speed of the applied gate voltage was 0.25 V/step. Obviously, the electrical breakdown field of stack oxide is up to 8.5 MV/cm. Evidently, stack oxide breakdown field decreased and leakage current increased when the thin oxynitride films were grown with a higher RF power as in 600 W or with longer oxidation time. The plasma-induced damage effect may explain this degradation of ultra-thin oxynitride films [10]. Fig. 3 shows the *C–V* curve of the stack gate dielectrics. Samples SOTFT-1 and SOTFT-3 have sharper curves than those of the conventional TEOS oxide.

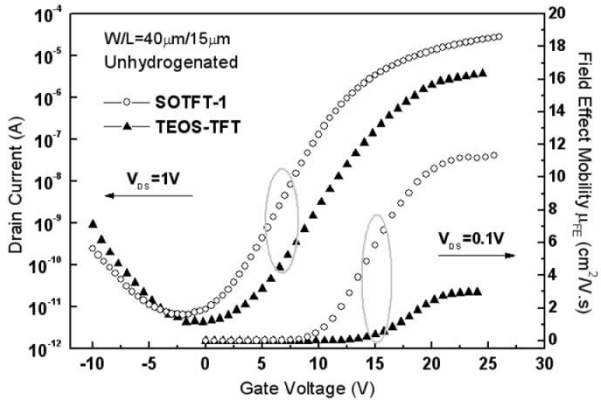

Fig. 4. Transfer characteristic for a 40 μm wide and 15 μm long stack oxide structure n-channel polysilicon TFT with $V_{DS} = 1$ V for drain current ID and $V_{DS} = 0.1$ V for field-effect mobility $\mu_{\rm FE}$.

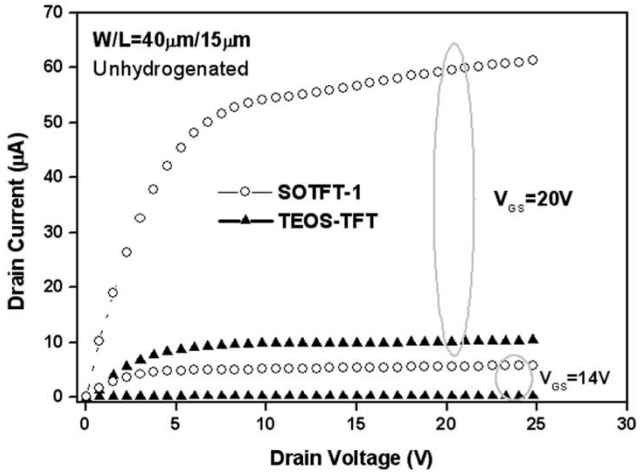

Fig. 5. Output characteristics of the fabricated poly-Si TFT with TEOS and stack oxide gate dielectrics.

This indicates that the interface traps of N_2O plasma oxynitride is less than that of conventional TEOS oxide [10]. Although the TEOS/N_2O plasma oxynitride stack gate dielectric induced more trapped charge than TEOS oxide and caused a slightly flat-band voltage (V_{FB}) shift, the TEOS/oxynitride stack gate dielectric still demonstrates good interface properties and lower leakage current than TEOS oxide. These results indicate that the ultra-thin oxynitride film of stack oxide was grown with the condition of RF power 200 W and oxidation time 1 min appeared to be the optimum process condition. Fig. 4 displays the I_D–V_G characteristics of the stack oxide and the conventional TEOS oxide LTPS TFTs. The ON current of the stack oxide TFTs (SOTFT) was approximately one order of magnitude higher than that of TEOS oxide TFTs (TEOS-TFT). The leakage current of SOTFT was 50% lower than that of TEOS oxide TFTs at $V_{gs} = -10$ V and $V_{DS} = 1$ V. Notably, the field effective mobility of stack oxide TFTs is 4 times that of TEOS oxide TFTs at $V_{DS} = 0.1$ V, $V_{GS} = 23$ V. Moreover, the subthreshold swing (SS) of the SOTFT was 2 V/dec, compared to 2.67 V/dec for the TEOS oxide TFTs. The subthreshold swing of TFTs is well known to be determined by the interface trap states, while the small SS value implies low interface states [11]. Fig. 5 shows the output characteristics of the stack oxide and conventional TEOS oxide LTPS TFTs. Importantly, the

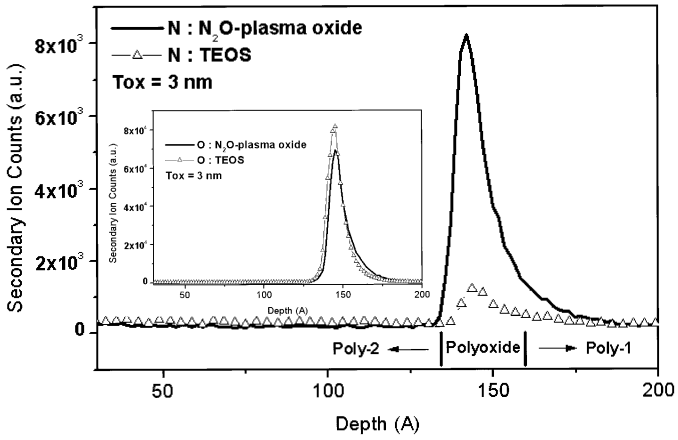

Fig. 6. SIMS nitrogen profiles of the thin N_2O plasma oxynitride and TEOS oxide films. The insert is the SIMS oxygen profiles of the thin N_2O plasma oxynitride and TEOS oxide films.

driving current of the stack oxide TFTs is significantly higher than that of TEOS oxide TFTs. Such a high driving current implies that SOTFT can be applied to integrated peripheral drive circuit on AMLCD panel.

This paper also evaluated the grain boundary trap density using a modified Levinson's model to investigate the improvement of device characteristics in TEOS/oxynitride stack oxide LTPS TFTs [12]. The density of the grain boundary traps in SOTFTs and TEOS TFTs was found to be 1.45 $\times 10^{13}/\mathrm{cm}^2\mathrm{ev}$ and 1.78 $\times 10^{13}/\mathrm{cm}^2\mathrm{eV}$, respectively, indicating that the N_2O plasma reduces both the interface and grain boundary trap states [10]. Fig. 6 shows the secondary ion mass spectrometry (SIMS) depth profiles of N and O atoms in the N_2O plasma-grown oxynitride and TEOS dielectric films. Structurally, the SIMS samples comprise poly-Si/oxide/poly-Si, and were prepared as the same process as the LTPS TFTs. The N concentration of the oxynitride film is clearly higher than that of the TEOS oxide film. And the SIMS nitrogen profile of others SOTFT samples was almost the same as that of the SOTFT-1. (data not shown.) This results proves that a large amount of nitrogen is present in the oxynitride film and forms the strong Si $\equiv$ N bonds at the oxynitride/poly-Si interface. The roughness of the oxide/poly-Si interface has also been reported to affect the field effect mobility of TFT devices [13]. The electrical characteristics and reliability of polyoxide are also correlated with the surface morphology of a poly-Si film [14]. Atomic force microscopy (AFM) was performed on samples of bare poly-Si film, poly-Si film with PECVD N_2O plasma oxidation, and poly-Si film on which TEOS oxide had been deposited, as shown in Fig. 7(a)–(c) respectively, to elucidate the surface morphology of the interface between oxide film and poly-Si. Notably, before AFM measurements were made, all of the samples were dipped into 100:1 HF solution to remove completely oxide grown on the poly-Si surface. The average RMS values of poly-Si roughness were 8.46, 5.8, and 7.18 Å, respectively. Clearly, the N_2O plasma oxidation process does not degrade the surface roughness of the poly-Si film. Furthermore, this process renders an interface even smoother than the original surface due to the uniformity of the oxidation rate, irrespective of the crystalline orientation and the suppression of enhanced

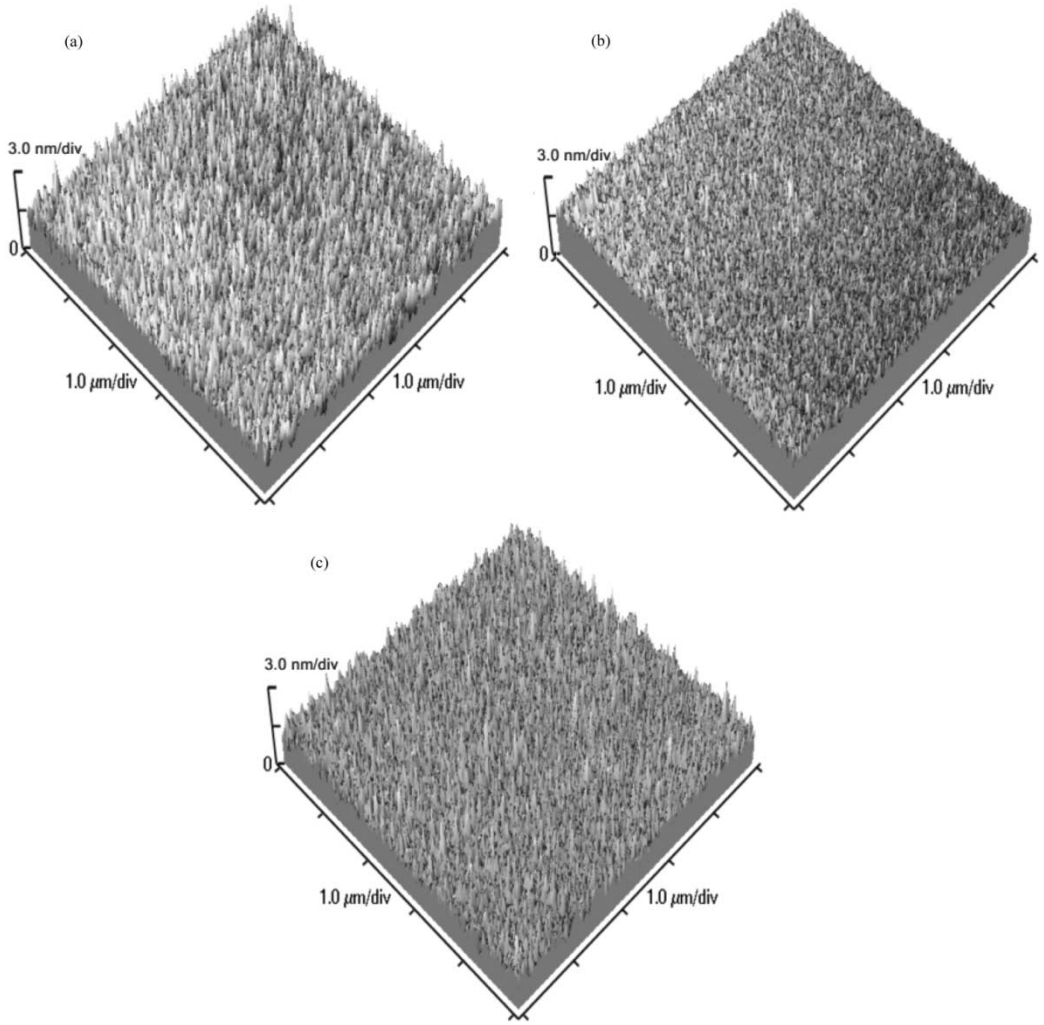

Fig. 7. AFM images of poly-Si. Before AFM observation, the oxide film on the poly-Si was removed completely. (a) Nontreated poly-Si sample. (b) Poly-Si sample with N_2O plasma oxidation. (c) poly-Si sample with TEOS oxide deposition. The corresponding RMS values of poly-Si surface roughness are 8.46 Å, 5.8 Å, and 7.18 Å, respectively.

oxidant diffusion through grain boundaries [6]. Based on these results, the improvement of the electrical characteristics of the stack oxide LTPS TFTs was attributed to the formation of strong Si $\equiv$ N bonds, the smoothness of the surface, and the reduction in the trap density at the oxide/poly-Si films interface associated with N_2O plasma-grown oxynitride.

As is well known, the hot carrier effect often degrades the performance and reliability of TFT devices [14]. The n-channel LTPS TFTs fabricated with novel TEOS/N_2O plasma oxynitride stack oxide and TEOS oxide were stressed at room temperature by a high electric field to study N_2O plasma oxynitride in relation to the reliability of TFT devices. Fig. 8 shows transfer characteristics of as-fabricated LTPS TFTs before and after hot carrier stress was applied ($V_{GS} = 20$ V, $V_{DS} = 25$ V) for 30 000 s. The typical operation voltage of high-voltage driver-integrated LTPS TFT-LCD application is $V_{dd} = 12$ V. The SOTFT exhibits a smaller shift in the threshold voltage, a smaller decrease in the peak transconductance and a smaller increase in the subthreshold slope than TEOS oxide TFTs after the stress. The slight shift of the transfer curves of SOTFT is believed to be related to the strong Si $\equiv$ N bonds formed by

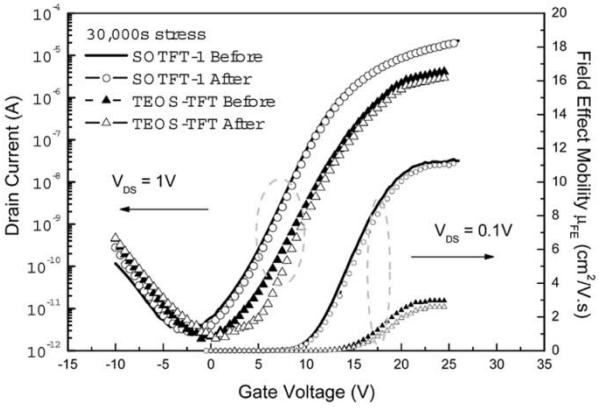

Fig. 8. Transfer characteristics of poly-Si TFTs with stack oxide and TEOS oxide before and after 30 000 s hot carrier stress with $V_{GS} = 20$ V, $V_{DS} = 25$ V.

the N_2O plasma, and the excellent trapping charge properties at the oxide/poly-Si interface, which reduce the generation of fixed charges by breaking weak Si-O bonds or Si-ON bonds under high-field stress [15]. This results shows that the N_2O

plasma-grown oxynitride positively affects on the reliability of the fabricated SOTFTs and improves the hardness of gate dielectric against stress-induced damage.

IV. Conclusion

The LTPS TFTs fabricated with TEOS/N_2O plasma-grown oxynitride stack gate dielectric exhibit excellent characteristics, including electrical breakdown field up to 8.5 MV/cm, low leakage current, low interface trap density, and high long-term reliability, resulting from the formation of strong Si $\equiv$ N bonds at the oxynitride/poly-Si interface, while the N_2O plasma passivation effect reduces the interface and grain boundary trap densities. The PECVD TEOS/N_2O plasma-grown ultra-thin oxynitride stack oxide can be adapted for utilization in the AMLCD panel manufacturing industry due to simple process and improving the performance of low-temperature fabricated poly-Si TFTs.

References

[1] G. K. Guist and T. W. Sigmon, "High-performance thin-film transistors fabricated using excimer laser processing and grain engineering," *IEEE Trans. Electron Devices*, vol. 45, pp. 925–932, Apr. 1998.

[2] J. K. Lee, J. B. Choi, S. M. Seo, C. W. Han, and H. S. Soh, "The application of tetraethooxysilane(TEOS) oxide to a-Si: H TFTs as the gate insulator," in *SID Tech. Dig.*, vol. 29, 1998.

[3] E. Ibok, K. Ahmed, M.-Y. Hao, B. Ogle, J. J. Wortman, and J. R. Hauser, "Gate quality ultrathin (2.5 nm) PECVD deposited oxynitride and nitrided oxide dielectrics," *IEEE Electron Device Lett.*, vol. 20, pp. 442–444, Sept. 1999.

[4] S. Han and H. Shin, "Ultrathin oxide grown on polysilicon by ECR (electron cyclotron resonance) N_2O plasma," in *Proc. Int. Symp. on Plasma-Induced Damage*, pp. 133–136.

[5] J.-W. Lee, N.-I. Lee, S.-H. Hur, and C.-H. Han, "Suppressed short-channel effects and improved stability in polysilicon thin film transistors with very thin ECR N_2O plasma gate oxide," in *IEDM Tech. Dig.*, 1997, pp. 519–522.

[6] J. W. Lee, N. I. Lee, S. H. Hur, and C. H. Han, "Oxidation of silicon using electron cyclotron resonance nitrous oxide plasma and its application to polycrystalline silicon thin film transistors," *J. Electrochem. Soc.*, vol. 144, p. 3283, 1997.

[7] K. P. Cheung and C.-S. Pai, "Charging damage from plasma enhanced TEOS deposition," *IEEE Electron Device Lett.*, vol. 16, pp. 220–222, June 1995.

[8] Y. Z. Xu, F. J. Clough, E. M. S. Narayanana, Y. Chen, and W. I. Milne, "A conductivity modulated high voltage polycrystalline silicon thin film transistor with improved on state and transient performance," in *IEDM Tech. Dig.*, 1998, pp. 273–276.

[9] F. J. Clough, Y. Chen, E. M. S. Narayanan, W. Eccleston, and W. I. Milne, "A novel thin film transistor for high voltage circuitry on glass," *Power Semicond. Devices ICs*, pp. 321–324, 1997.

[10] J.-W. Lee, N.-I. Lee, J.-I. Han, and C.-H. Han, "Characteristics of polysilicon thin-film transistor with thin-gate dielectric grown by electron cyclotron resonance nitrous oxide plasma," *IEEE Electron Device Lett.*, vol. 20, pp. 172–174, May 1997.

[11] C. A. Dimitriadis, P. Coxon, L. Dozsa, L. Papaddimitrious, and N. Economou, "Performance of thin film transistors on polysilicon films grown by LPCVD at various conditions," *IEEE Trans. Electron Devices*, vol. 39, p. 598, Mar. 1992.

[12] J. Levinson, F. R. Shepherd, P. Scanlon, W. D. Westwood, G. Este, and M. Rider, "Conductivity behavior in polycrystalline semiconductor thin film transistors," *J. Appl. Phys.*, vol. 53, p. 1193, Feb. 1982.

[13] K. Takechi, H. Uchida, and S. Kaneko, "Mobility improvement mechanism in a-Si:H/SiNx interface," in *Proc. Mat. Res. Soc. Symp.*, vol. 258, 1992, p. 955.

[14] J. Y. Lee, C. H. Han, and C. K. Kim, "ECR plasma oxidation effects on performance and stability of polysilicon thin-film transistors," in *IEDM Tech. Dig.*, 1994, p. 523.

[15] M. Hack *et al.*, "Physical models for degradation effects in polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 40, pp. 890–898, May 1993.

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