A 2-V 2.3/4.6-GHz Dual-Band Frequency Synthesizer in 0.35-μm Digital CMOS Process

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***Abstract*—This brief describes the design of a frequency synthesizer for 2.3/4.6-GHz wireless applications in a 0.35-μm digital CMOS process. This synthesizer provides dual-band output signals by means of frequency doubling techniques. Output frequency of the proposed synthesizer ranges from 1.87–2.3 GHz, and 3.74–4.6 GHz. This chip consumes a total power of 80 mW from a single 2-V supply, including 45 mW for dual-band output buffers. Core size is 2200 μm $\times$ 1600 μm.**

***Index Terms*—Dual band, frequency doubler, frequency synthesizer.**

I. Introduction

PHASE-LOCKED loop (PLL)-based frequency synthesizers are often utilized for RF local oscillator design for their capacity to operate at high speed. Synthesizers of this type can vary their output frequency by changing the divide ratio of the frequency divider in the feedback path. Along with the increasing demands of data bandwidth, the radio frequency of wireless local-area network (LAN) transceivers have been pushed beyond 5 GHz [1]–[4]. Meanwhile, the operating speed of voltage-controlled oscillators and frequency dividers in the PLL-based frequency synthesizer should be increased as well, which in general results in high power consumption of the radio transceiver.

This brief presents a PLL-based frequency synthesizer fabricated in a 0.35-μm digital CMOS process. In this architecture, a high-frequency carrier is indirectly synthesized by a novel frequency doubler [4], [5]. Thus, the operating frequency of the VCO and prescaler can be relaxed to save power. This architecture also inherently provides dual-band carriers.

II. Architecture

Fig. 1 shows the frequency synthesizer architecture, which consists of a voltage-controlled oscillator (VCO) that employs an on-chip tuning scheme, a programmable frequency divider ($1/N$), a phase-frequency detector (PFD), a second-order charge pump loop filter (CP), and a frequency doubler ($\times 2$). The VCO provides quadrature output phases for the frequency doubler, and can be utilized in conjunction with image rejection mixers. The frequency divider consists of a divide-by-64/65 prescaler followed by a 10-bit programmable counter and a 6-bit swallow counter. Thus, the divide ratio ranges from 128 to 65 535.

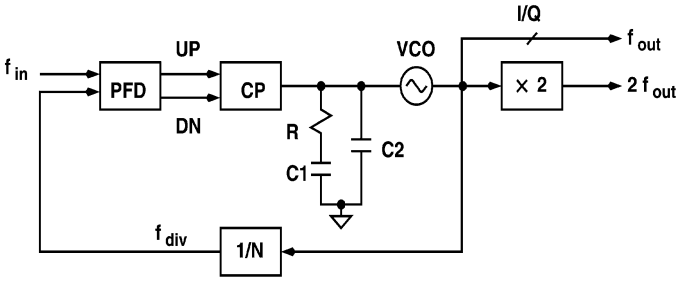

Fig. 1. Frequency synthesizer architecture.

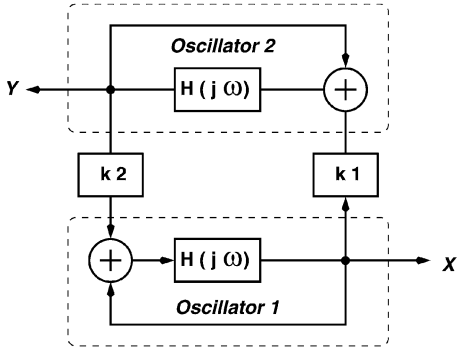

Fig. 2. Quadrature VCO architecture.

A. Varactorless LC VCO

For RF transceiver applications, the *LC*-type oscillator is a superior choice due to the inherent bandpass filtering of the *LC* resonator which can suppress side-band noise. Conventionally, the VCO's output frequency is tuned by on-chip varactor diodes. For a multigigahertz-range application, varactor diodes should exhibit low parasitic capacitance and wide tuning range to cope with process variations. However, a wide tuning range is difficult to achieve under a low supply voltage. In this design, a quadrature phase varactorless-type VCO is utilized.

The architecture of the quadrature VCO, as shown in Fig. 2, consists of two mutually coupled *LC* oscillators, $OSC1$ and $OSC2$ [6]. These two oscillators are identical, and each oscillator is modeled by a positive feedback system with open—loop gain $H(j\,\omega)$. Let their outputs be coupled to the inputs of each other with coupling coefficients of $k1$ and $k2$, where $k_1 = -k2 = k$. Assuming that these two oscillators are synchronized to the same oscillation frequency of ω_1 at the steady state,

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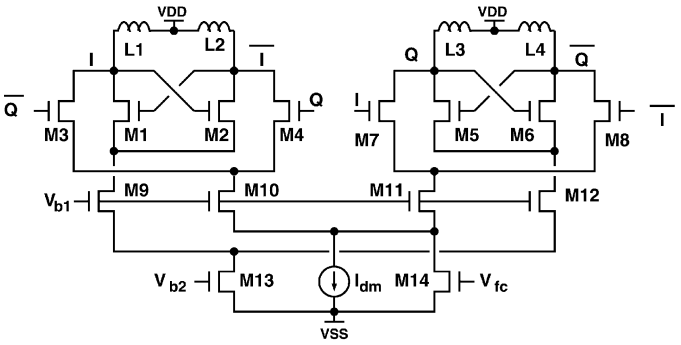

Fig. 3. VFO circuit schematic.

the output phasors (X, Y) of the two oscillators ($OSC1$ and $OSC2$) must satisfy

$$(X + k_2 Y)H(j\omega_1) = X \tag{1}$$

$$(Y + k_1 X)H(j\omega_1) = Y. \tag{2}$$

The combination of these two equations indicates that

$$X = \pm jY.$$

Thus, quadrature phases can be derived at the VCO outputs.

The oscillation frequency ω can be determined by substituting $X = \pm jY$ into (1) or (2), which yields the frequency tuning characteristic equations, as follows:

$$H(j\omega) = \frac{1}{1 \pm jk} \tag{3}$$

$$\angle H(j\omega) = \pm \tan^{-1} k. \tag{4}$$

There will be two solutions, ω_1 and ω_2, which correspond to positive and negative sign, that both satisfy (4). However, only the oscillation frequency ω_1 that is closer to the resonant frequency of the *LC*-tank can be sustained. As OSC's phase response can be varied by adjusting the coupling coefficient k, the VCO's output frequency can be changed accordingly [6].

The detailed circuit schematic of the quadrature phase VCO is shown in Fig. 3. Here, $OSC1$ is composed of (M1, M2, M9, L1, L2), and $OSC2$ is composed of (M5, M6, M12, L3, L4). These two oscillators are mutually coupled by two differential amplifiers (M3, M4, M10) and (M7, M8, M11), and the coupling coefficient is determined by the current source M14. The VCO's output frequency can be varied by tuning the bias voltage V_{fc}. In order to avoid loss of coupling in the extreme case of frequency tuning, i.e., k approaching zero, an extra current source I_{dm} is added in parallel to M14. Thus, quadrature output phases can be maintained at any output frequency.

Let the VCO's outputs at I, $\overline{I}$, Q, and $\overline{Q}$ be represented as $A\sin(\omega_1\, t)$, $A\sin(\omega_1\, t + 180°)$, $A\sin(\omega_1 t + 90°)$, and $A\sin(\omega_1\, t + 270^o)$. The drain voltages of M10 and M11 can be derived as

$$V_{DM10} \approx V_{DC_1} + \frac{\alpha \cdot \sin(2\omega_1\, t)}{2V_{DC_2}} \tag{5}$$

$$V_{DM11} \approx V_{DC_1} - \frac{\alpha \cdot \sin(2\omega_1\, t)}{2V_{DC_2}}. \tag{6}$$

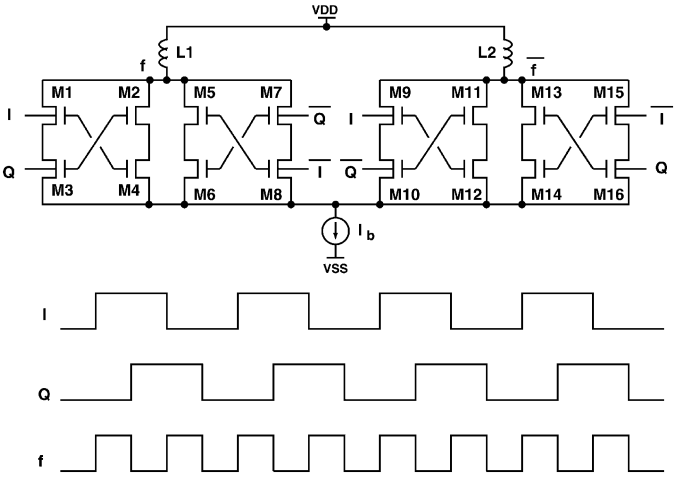

Fig. 4. Frequency doubler.

Equations (5) and (6) show that V_{DM10} and V_{DM11} will be modulated by the second-order harmonic of the VCO's oscillation frequency, which will result in tail current variation due to the finite output resistance of the current source. As long as the tail current variation of $OSC1$ is out of phase to that of $OSC2$, in the steady state, the summation of the $OSC1$ and $OSC2$ switching currents should approximate a constant. In this design, $OSC1$ together with $OSC2$ are biased at a constant current source M13. Thus, the tail current variation can be alleviated. From another viewpoint, the constant current biased scheme becomes another constraint to synchronize quadrature phases at VCO output and improves amplitude matching. Also, the proposed architecture could improve phase noise performance by suppressing AM-to-PM noise conversion.

B. Frequency Doubler

The proposed frequency doubler is depicted in Fig. 4. By means of I/Q phase mixing, the pulsewidth of the differential amplifier is reduced to 1/4 VCO period, which results in double frequency at the output. The NAND functions of the quadrature phases are decomposed into four pass transistor logic in parallel and swap-connected to balance the loading effects as seen by the VCO. Moreover, inductive loads are employed in the frequency doubler to speed up voltage switching. On the other hand, the inductive loads perform as a resonator in conjunction with parasitic capacitance at the output node. This provides bandpass filtering to suppress spurious tones caused by phase mixing. According to simulation results, the output power variation of the frequency doubler is less than 0.5 dB while the spurious free dynamic range is higher than 50 dB with phase mismatches larger than $\pm 5\%$. This indicates that the frequency doubler has high immunity to phase mismatch due to its fully symmetrical architecture and bandpass filtering. In this prototype, (L1, L2) of the frequency doubler are made up of bonding wires, and therefore, no extra on-chip spiral inductors are required.

III. Experimental Results

Fig. 5 shows the measured VCO frequency transfer characteristic. The output frequency of the VCO ranges from 1.87 to

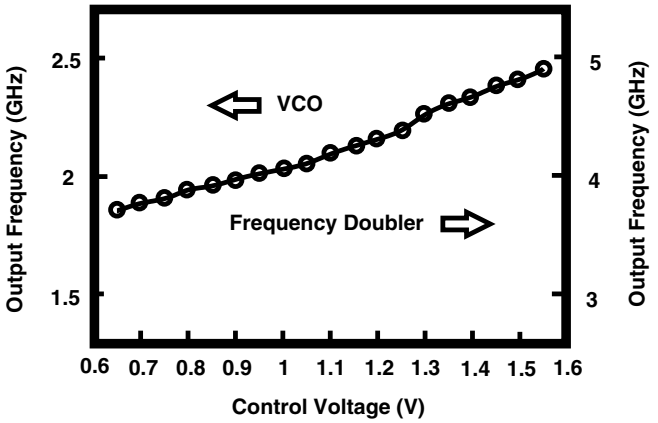

Fig. 5. Measured VCO frequency tuning characteristic.

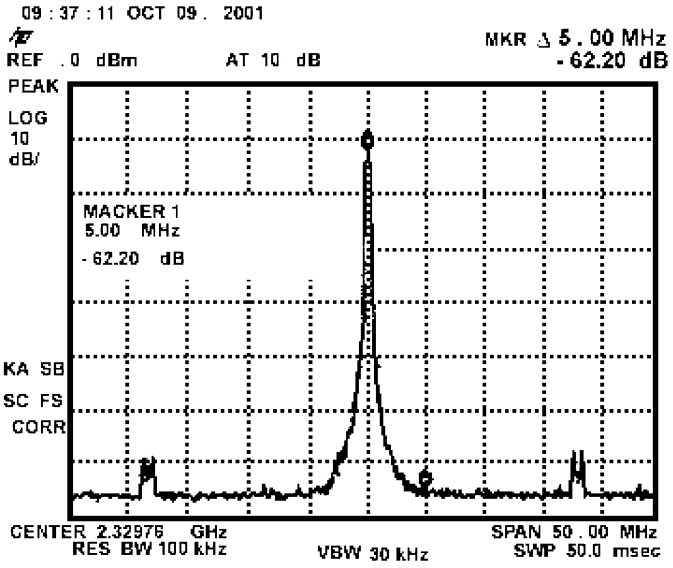

Fig. 6. Measured VCO output spectrum.

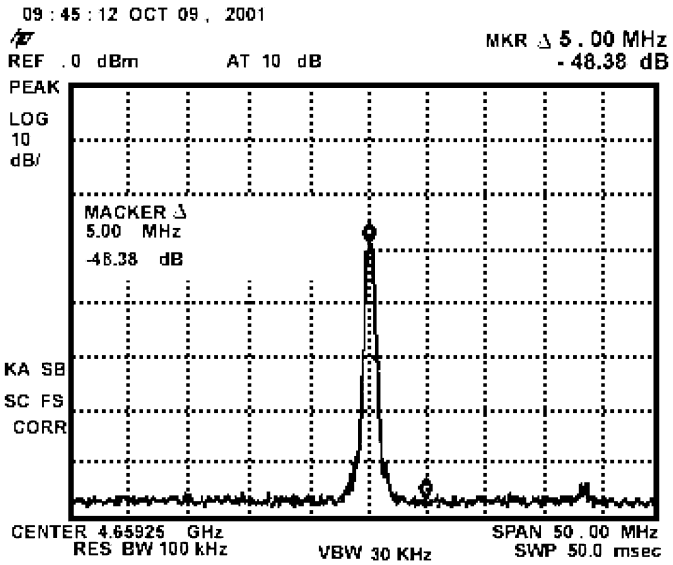

Fig. 7. Measured frequency doubler output spectrum.

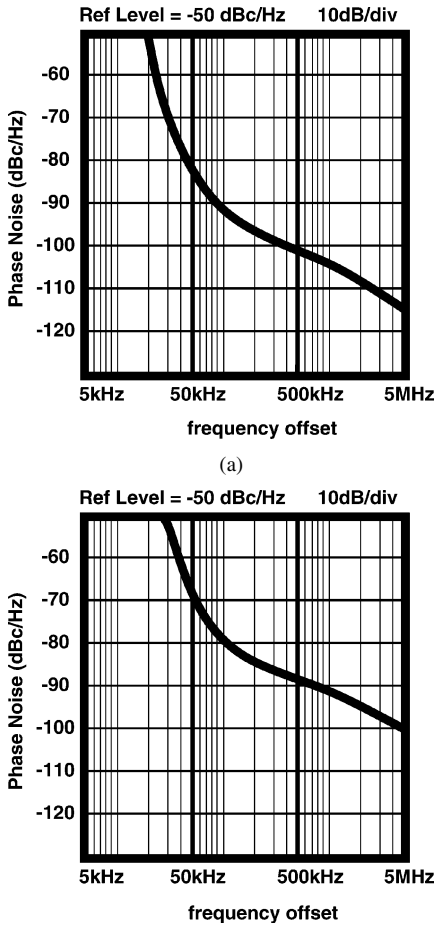

Fig. 8. Phase noise plot at (a) 2.33 GHz and (b) 4.66 GHz.

2.3 GHz and from 3.74 to 4.6 GHz. The highest output frequency is limited by the prescaler. The conversion gain of the VCO is about 430 MHz/V. The loop bandwith is about 120 kHz and the damping factor is 0.55. The measured output spectrum at 2.33 GHz is shown in Fig. 6, while the frequency doubler output signal at 4.66 GHz is shown in Fig. 7. The measured phase noise plots of the 2.33 and 4.66 GHz carriers are shown in Fig. 8. At 5-MHz offset, the phase noise is -114 dBc/Hz and -100 dBc/Hz, respectively, from a 2.33- and 4.66-GHz output signal. The phase noise performance is improved by 3 dB at 2 GHz and 4 GHz as the output frequency is tuned to the resonant frequency of the *LC* tank. The measured frequency spurs are 60 and 48 dB below the main carrier at 2.3- and 4.6-GHz output, respectively.

The reasons for moderate phase noise performance are mainly due to two factors. First, in this prototype, the conversion gain of the VCO is relatively high, which makes the VCO susceptible to noise coupling. Second, as the frequency of oscillation deviates from the resonance frequency of the standalone oscillator, the effective Q of the tank is reduced. This results in the degradation of phase noise performance.

Fig. 9 shows the chip photograph of the frequency synthesizer, including a quadrature VCO, an on-chip loop filter, a frequency doubler, a programmable divider, and dual-band output buffers. Implemented in a 0.35-μm digital CMOS process, the core area of the PLL occupies a chip area of

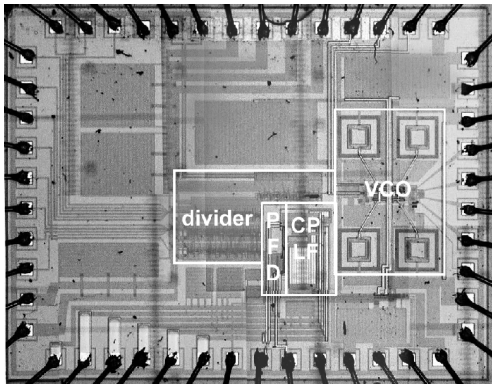

Fig. 9. Die micrograph of the frequency synthesizer.

2200 μm $\times$ 1600 μm. This chip is pad-limited by numerous modulus-control inputs. Under a single 2-V supply, this chip drains a total power of 80 mW, including 8 mW for the VCO core, and 45 mW for output buffers at both 2.3 and 4.6 GHz to drive 50-Ω load.

IV. Conclusion

This paper describes the design of a single-chip dual-band frequency synthesizer in a low-cost digital CMOS process. In this design, a varactorless VCO composed of two identical oscillators is utilized. Frequency tuning is achieved by varying mutual coupling of the two fixed frequency oscillators. Quadrature output phases can be derived from the VCO. The two VCOs are biased by a constant current source to improve both amplitude and phase matching performance. In addition, output phase noise is reduced by this constant current biased scheme. Finally, a novel frequency doubler is proposed in this design, which relaxes the operating speed of the VCO and prescaler. Thus, lower power consumption can be obtained. Doubled frequency output is indirectly synthesized by quadrature phase mixing. The inherent bandpass filtering of the frequency doubler can suppress the spurious tones caused by phase mixing.

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