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Electrical properties of sputter deposited $SrTiO_3$ gate dielectrics

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Abstract

We report the electrical properties of gate dielectric $SrTiO_3$ (STO) thin films on Si substrates grown by radio-frequency magnetron sputtering. The interfacial layer between STO and Si degrades the performance of the gate dielectric. We used SiON as a sacrificial layer for incorporating nitrogen into Si substrate surface, which can retard the formation of interfacial layer during the high temperature growth of STO gate dielectric. The polycrystalline STO film grown on nitrogen incorporated Si substrate exhibited lower leakage current due to better interfacial properties and higher dielectric constant. The repeated spike heating technique was also employed to deposit polycrystalline STO film for improving the thermal uniformity of the wafer, which leads to lower gate leakage current. The processing parameters including working pressure, oxygen mass ratio and plasma power also show obvious effect on the electrical properties of the films.

Keywords: Electrical properties; Films; Gate dielectric; $SrTiO_3$

1. Introduction

Following the device continuously scaling down, the conventional SiO_2 gate oxide thickness will be less than 2 nm in the near future.[1] However, the use of ultrathin SiO_2 gate dielectric results in a number of issues, including high gate leakage current, reduced drive current, reliability degradation, boron penetration, and the necessity to grow ultra-thin and uniform SiO_2 layer. Any of these effects will fundamentally limit the usefulness of SiO_2 as a gate dielectric. According to the fundamental quantum mechanical law, the direct tunneling current increases exponentially with decreasing film thickness. The leakage current increases by one order of magnitude when each 0.2 nm thickness decreases. As the SiO_2 thickness scales below 2 nm, the gate leakage current will increase significantly due to direct tunneling. Many high-k materials have been investigated as potential replacements for SiO_2 to provide a physically thicker film for reducing leakage current and improving gate capacitance. The physical thickness of such high-k material can be much larger to reduce the tunneling current, so alternative gate dielectrics with high dielectric constant are necessary. $SrTiO_3$ (STO) thin films have been proposed for applications in high charge storage capacity devices, such as DRAM capacitors, because of their high dielectric constant. Recently, STO thin films have been successfully epitaxially grown on Si by using molecular beam epitaxy at Motorola Labs[2] as a gate dielectric of MOSFETs. On the other hand, STO films with low equivalent oxide thickness (EOT) and low leakage current can also be a potential insulating layer as in metal/ferroelectric/insulator/semiconductor (MFIS) structure, which is a basic structure for ferroelectric gate non-volatile ferroelectric memory application.[3] In general, interfacial layer will naturally form between high-k metal oxide materials and Si due to Si oxidation and inter-diffusion at high temperature. The resultant interfacial layer of low permittivity materials will limit the highest possible gate capacitance or the lowest achievable EOT. Several methods have been employed to reduce the interfacial reaction. Incorporating nitrogen in silicon substrate has been used to grow ultra thin oxide because nitrogen can suppress the growth of silicon oxide effectively.[4] A repeated-spike-heating technique has been proposed by Hong et al.[5] to grow ultrathin oxide. The radiation heat absorption in two different temperature regions on a wafer could be

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compensated by repeated-spike-heating technique,[6] so such technique can improve the thermal uniformity to grow uniform SiO_2. In the present study, we incorporated nitrogen into the silicon surface to alleviate the reaction of the silicon surface into SiO_x thin interface layer during rf-sputtered deposition STO gate dielectric and to obtain better EOT value. The repeated-spike-heating technique was also employed to deposit STO films for improving the thermal uniformity of the wafer. Electrical characterizations of STO thin films were also performed. Besides the study of the interface improvement, the influence of the processing parameters including working pressure, oxygen mass ratio (OMR), and plasma power on electrical properties of STO thin films was also investigated.

2. Experimental

Boron doped *p*-type silicon (100) wafers with 1–10 Ω-cm resistivity were used as the starting substrates. After standard RCA clean, a 8-nm SiON film was grown on silicon wafer at 950 °C in pure N_2O gas as the sacrificial oxide. For comparison, 8-nm SiO_2 was thermally grown in pure O_2 ambient as the control sample. After SiON and SiO_2 films were removed by HF dip, the 20-nm STO thin films were deposited on the above pre-treated substrates by using rf magnetron sputtering at a substrate temperature of 500 °C at the same time. The fabrication flow chart is illustrated as Fig. 1(a). The repeated-spike-heating and typical profiles used for depositing STO films are shown in Fig. 1(b). The repeated-spike-heating method was set the temperature to ramp up and down between 450 and 550 °C, while the typical profile was held at a constant temperature of 500 °C. The rapid thermal annealing (RTA) was performed in N_2 ambient to improve the quality of films. To investigate the effect of the processing parameters such as working pressure, OMR, and plasma power on the electrical properties of the films, the other parameters were fixed while one was varied. For the electrical measurement, Al top electrode with an area of 7.0×10^{-4} cm^2 was formed by thermal evaporation, followed by electrode patterning using a wet lithography process. Al was also used as backside electrode for obtaining ohmic contact. The capacitance–voltage (C–V) measurements were performed using a HP 4284A at 100 k to 1 M Hz. The current–voltage (I–V) measurements were recorded using a HP 4156A Semiconductor Parameter Analyzer.

3. Results and discussion

After the removal of SiON and SiO_2 sacrificial oxide by dipping in HF, the X-ray photoelectron spectroscopy (XPS) profiles of the silicon substrates were recorded. The XPS profiles are illustrated in Fig. 2. It can be easily seen that nitrogen has been moderately incorporated onto the silicon substrate surface. The amount of nitrogen on the N_2O pre-treatment wafer calculated from the XPS measurement data is 0.895% atomic ratio. While the STO dielectric capacitance was measured by HP4284A at 100 k to 1 M Hz, the C–V curves were found frequency dependence, as shown in Fig. 3. The phenomena are due to extrinsic parasitic inductance and resistance. After being calibrated by the two-frequency four-element model,[7] illustrated in the insert of Fig. 3, the calibrated C–V curves of the N_2O pre-treatment and control samples are shown in Fig. 4. We can observe that the EOT of N_2O pre-treatment sample is smaller than that of the control sample. The quantum mechanical curve fitting[8] is also shown in Fig. 4, from which the EOT is extracted to be 3.0 and 3.3 nm for N_2O pre-treatment and control samples, respectively. The slight shift of the measured C–V curves in comparison with the theoretical curve is due to the interface trap density. Fig. 5 shows the leakage current densities of the N_2O pre-treatment sample and the control sample. The N_2O pre-treatment sample has leakage current density 2–3

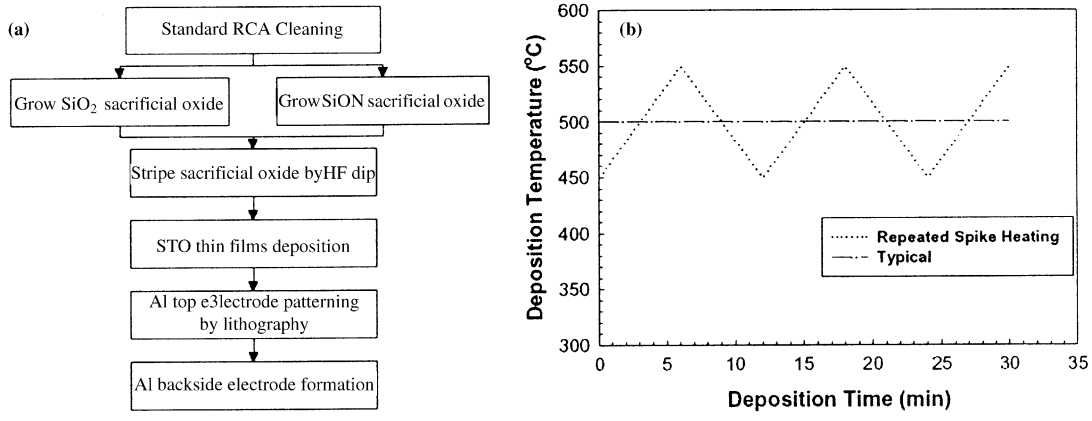

Fig. 1. (a) Fabrication flow chart (b) Deposition temperatures for repeated-spike-heating and typical samples.

order-magnitude lower than the control sample at the positive bias, while the leakage current of the N_2O pre-treatment sample is little less than that of control sample at the negative bias. The EOT of 500 °C deposited 20 nm thick STO thin films on silicon substrates prepared with various working pressures, 5, 25, 35, and 45 mTorr, are shown in Fig. 6. As expected, the growth rate of the sputtered STO thin films decreases with increasing working pressure. Film thicknesses were fixed at 20 nm through controlling the deposition time in order to eliminate effect of thickness on dielectric properties. The composition of STO films is influenced by the working pressure and may affect the dielectric constant of the films accordingly. This may be the main reason for the EOT decreasing with the increase of working pressure for the samples indicated in Fig. 6. We can also observe that the N_2O pre-treatment samples have lower EOT than the control samples. Fig. 7 shows the transmission electron microscopy (TEM) images of the N_2O pre-treatment and the control samples with working pressure of 45 mTorr, indicating that the interfacial layers of N_2O pre-treatment sample and the control sample are 1.9 and 2.6 nm, respectively. Therefore, the N_2O pre-treatment sample with lower EOT is attributed to its smaller thickness of interfacial layer between STO and Si. The variation of the leakage current density with working pressure for control and N_2O pre-treatment samples is illustrated in Fig. 8. The N_2O pre-treatment samples have leakage current densities 2–3 order-magnitude lower than control samples at 3 V. This difference may be due to the formation of the high band gap interfacial layer between STO and Si or the nitrogen can fill the dangling bonds at the interface leading to reduce the gate leakage current. The repeated spike heating technique was also employed to rf-sputtered STO film for improving the thermal uniformity of the wafer. After the STO thin films were deposited on Si substrate at 500 °C, RTA was performed in N_2 ambient at the temperatures ranged from 650 to 800 °C to improve the quality of the films. With the same EOT, the repeated spike heating samples have leakage current densities 1–2 orders of magnitude lower than typical samples at −3 V, as illustrated in Fig. 9. The reason for the reduction

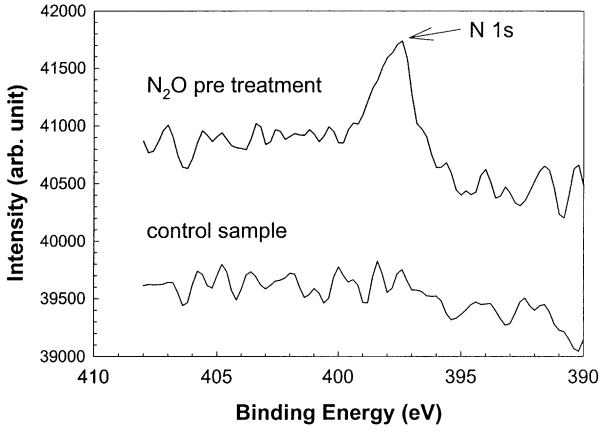

Fig. 2. XPS profiles of the silicon substrate surface after SiON and SiO_2 sacrificial oxides removed by HF dip.

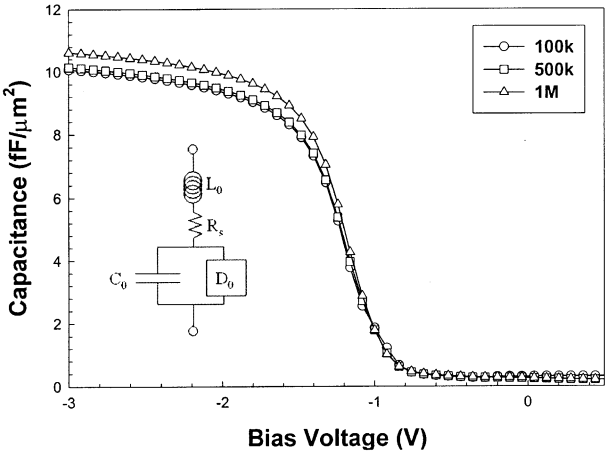

Fig. 3. Measured capacitance of MOS capacitors with STO gate dielectric at three different frequencies. The inset is the equivalent circuit of the calibrated four-element model.

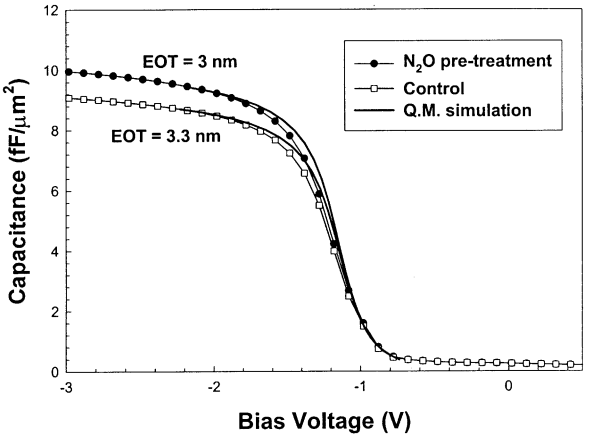

Fig. 4. Calibrated C–V curves of control and N_2O pre-treatment samples and their quantum mechanical (Q.M.) fitting.

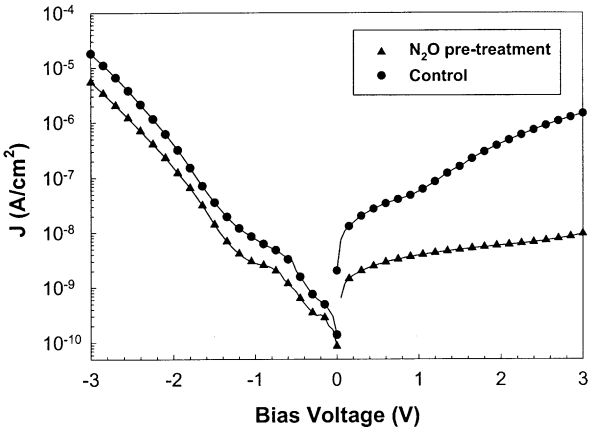

Fig. 5. I–V curves of control and N_2O pre-treatment samples.

of leakage current in repeated spike heating samples might be due to the improvement of the thermal uniformity of the substrate. Such thermal uniformity may lead to the formation of uniform grain size films, which affects the properties of the STO films. Another possible reason may be due to the smaller interface state density. Fig. 10 indicates the normalized C–V curves of typical and repeated-spike-heating samples. We can observe that the repeated-spike-heating sample has smaller interface trap density than the typical sample. The wagging and stretching of Si–O bond are temperature dependent. Therefore, during the temperature ramping up and down in repeated-spike-heating recipe, it is possible that the residual oxygen in films has more chance to fill the silicon dangling bonds and thus, better interface has been formed. The C–V curves of 500 °C deposited STO thin films on silicon substrates with various $O_2/(O_2 + Ar)$ (OMR) ratios, 10, 20, 40, and 50%, are shown in Fig. 11. The accumulation capacitance increases with increasing OMR up to 40%, and then further increase of the OMR decreases the capacitance. In 10–40% OMR deposited films, the dielectric constant of STO films increases with the increasing OMR (insert of Fig. 11), which is due to the enhanced

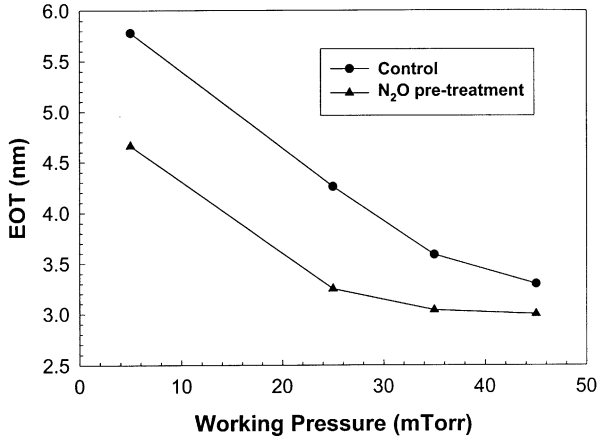

Fig. 6. Variation of EOT with working pressure for control and N_2O pre-treatment samples.

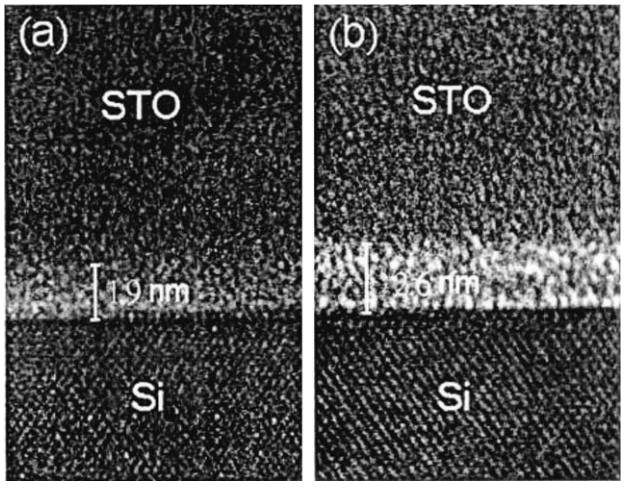

Fig. 7. TEM micrographs of (a) N_2O pre-treatment STO thin film and (b) control sample.

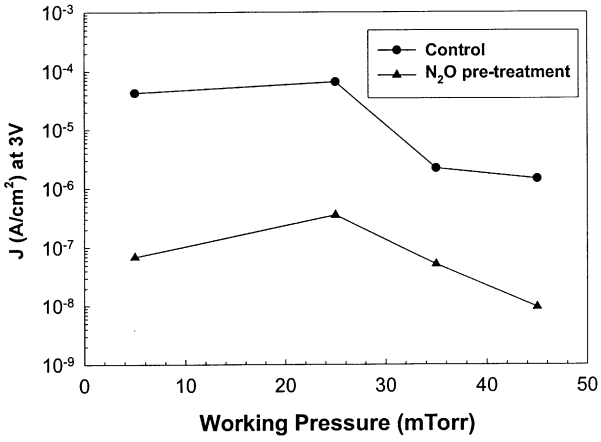

Fig. 8. Gate leakage current density at 3 V of N_2O pre-treatment and control samples prepared at various working pressures.

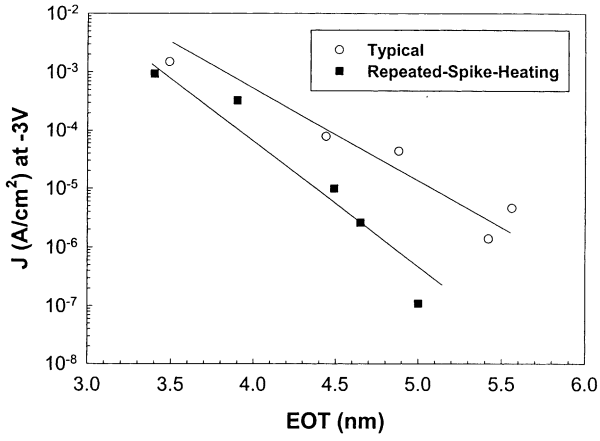

Fig. 9. Variation of gate leakage current density with EOT for typical and repeated-spike- heating samples.

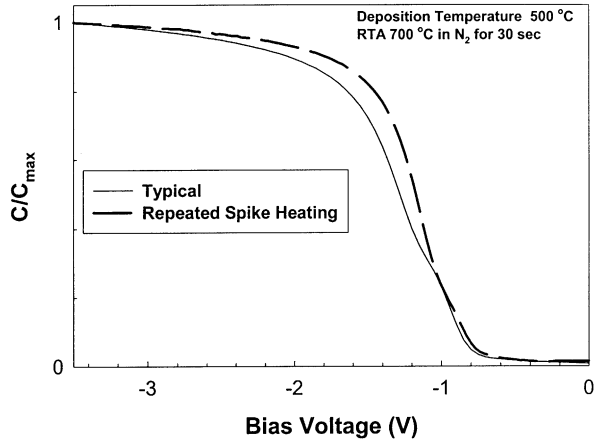

Fig. 10. Normalized C–V curves of typical and repeated-spike-heating samples.

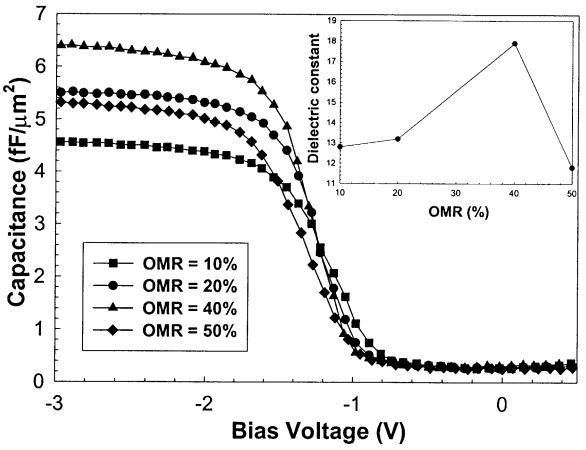

Fig. 11. High frequency (100 kHz) C–V curves of MIS capacitors with various OMR STO films. The insert shows the dielectric constant of the films with various OMR.

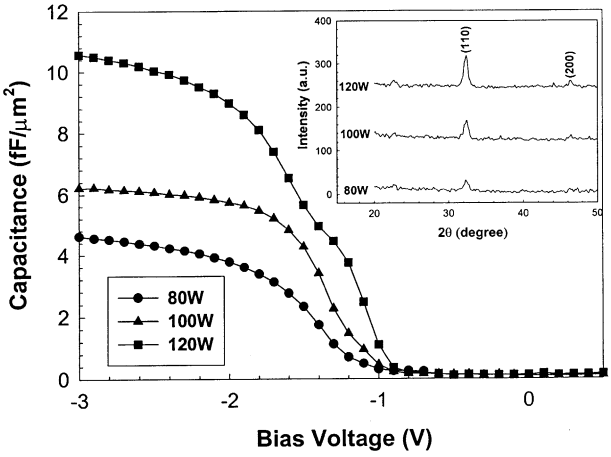

Fig. 12. High frequency (100 kHz) C–V curves of MIS capacitors with various plasma power STO films. The insert shows the XRD patterns of the films with various plasma power.

polarization after oxygen incorporation in the films. The decreased dielectric constant in 50% OMR deposited film may be attributed to thicker interfacial layer and smaller grain size of the films. Fig. 12 shows the high frequency C–V curves of MIS capacitors with various plasma powers deposited STO thin films. It is indicated that the accumulation capacitance increases with the increasing plasma power. Such higher capacitance is due to better crystallized films prepared at higher plasma power, which is confirmed by the XRD patterns as illustrated in the insert of Fig. 12. The kink observed in the C–V curve of 120 W STO film may be due to the trap resulting from the high plasma damage.

4. Conclusions

We have grown the SiON sacrificial oxide in pure N_2O ambient and then stripe it to incorporation nitrogen in the silicon surface. Nitrogen incorporation method was carried out to improve the C–V and I–V properties of the STO films. The EOT values of N_2O pre-treatment samples are 10–24% lower than those of the control samples while their leakage current densities also have 2–3 order-magnitude lower than those of control samples at the positive bias. The difference may be attributed to the incorporation of certain amount of nitrogen onto the substrate surface during the N_2O pre-treatment to depress the formation of the interfacial layer and reduce the interface states during the high temperature growth of STO gate dielectrics. Besides, the repeated spike heating method was also studied to improve the film quality with the same EOT, this method can reduce the leakage current density 1–2 order-magnitude compared with normal samples, which may be due to resultant interface trap density reduction and uniform grain size. The processing parameters, such as working pressure, OMR, and plasma power have significant influence on the electrical properties of STO thin films.

Acknowledgements

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