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ORIGINAL ARTICLE

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A daily production model for wafer fabrication

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Abstract The complex process and high variation in wafer fabrication make its production management very difficult. Problems such as planned target achievement and line balancing are not unusual in the industry. Such problems reveal the importance of developing a daily production policy for wafer fabrication. Planned target achievement and line balancing are the major concerns of this investigation in developing a daily production model. This investigation divides the process of wafer fabrication into two sections, i.e., the front and the rear, according to the last sputtering operation step. In the rear section, the objective is attaining the planned output target. In the front section, the major focus is to satisfy the demand of the rear section so that the production line is balanced. Release and dispatch policies are incorporated in this study to achieve both objectives. A real-world numerical example is used as simulation data. Results show that the proposed daily production model gives a better performance in the achievement of monthly planned output but suffers a little in the performance of line balancing.

Keywords Wafer fabrication · Planned target · Line balancing · Cycle time

1 Introduction

Because it requires more than 500 operational steps, it usually takes at least one to two months to complete the production of a wafer. Compared with other manufacturing industries, wafer fabrication experiences many shop floor variations, such as machine breakdowns, preventive maintenance, engineering and hot lots, yield problems, etc. All these factors make the development of dispatch rules in wafer fabrication important and complicated. Many studies concerning release and dispatch policies for wafer fabrication have been presented in the last decade. Some simulation studies show that the wafer release mechanism has more impact on system performance than the dispatch rules [5,6,8,12,15,18]. However, the function of release policy is degraded without incorporation with an appropriate dispatch policy. The release policy of wafer fabrication can be classified as closed-loop and open-loop systems. In general, the closed-loop policy is better than the open-loop policy [15]. The main objective of the closed-loop control policy is to keep an optimal WIP level in the factory. The wafer release policy is determined according to the discrepancy between the actual and projected WIP levels [7]. The starvation avoidance (SA) method [5,6] considers re-entrant flows in wafer fabrication. The major objectives of SA algorithms are to increase utilization of equipment and to maintain a low level of WIP. The Two-Boundary (TB) algorithm [13,14,19] is based on the concept of flow rate control. In the TB policy, it is assumed that random machine failure is the only source of interference. Two indices are employed to determine the releasing policy: (1) the discrepancy between the actual accumulated production output and the planned accumulated production output in the first processing step; and (2) the discrepancy between the actual inventory level and the planned inventory level in the second operational step. Release is admitted only when both of the two indexes are negative. The TB method is only applied to the bottleneck equipment. For non-bottleneck equipments, the FIFO (First In First Out) rule is used. According to the TB approach, the dispatch method is identical to that of the release policy. The re-entrant-flow characteristics of wafer fabrication as well as bottleneck resources are considered in the

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workload regulating (WR) policy [18,19]. The release policy of WR is based on the total workload of the bottleneck equipment. When the workload of a bottleneck machine is less than the safety value, the release action is implemented immediately. The WR method is only a release policy, which lacks a dispatching policy to coordinate with. In the fixed WIP (FW) method [1,5,6,16] the release of wafers is conducted when the actual inventory level of the second operational step is less than its planned inventory level. The dispatch policy of the FW method concentrates only on the release policy of bottleneck machines. The wafer lot has a higher priority while its actual inventory level is less than the planned inventory level. Chang et al. [4] developed a TG & MA (Target Generation & Machine Allocation) algorithm for wafer fabrication. The TG & MA algorithm is cooperated with a release and dispatch strategy to achieve the production target. Wang [17] pointed out that the TG & MA algorithm is able to make the system WIP reach a standard distribution after a certain time period. However, the required output may not be attained because the TG & MA algorithm focuses only on line balancing. Cheng [3] proposed a simulation procedure to obtain the system WIP level and distribute the total WIP to each layer through a queuing model.

In this paper, a daily production model is proposed to achieve two objectives: (1) to attain the monthly required output and (2) to maintain the line balancing. A simulation model with real factory data is experimented with to verify results.

2 Framework of a daily production procedure

Two stages are contained in the proposed model, namely the production planning stage and the production control stage. Figure 1 shows the framework of the proposed model.

2.1 Production planning stage

Because the photolithography workstations determine the total output of the wafer fabrication, these workstations are usually bottlenecks. Furthermore, the processing steps between any two consecutive photolithography re-entries constitute a layer. Therefore, the wafer fabrication process is divided into the front and the rear in this investigation. Each section adopts a distinct method for seeking its corresponding target. Release and dispatch procedures for photolithography area are designed to achieve the required output as well as the line balancing requirement. In this investigation, the required output is determined according to the master production schedule (MPS) from the Production Control (PC) department. The standard system WIP level is determined by employing Chan's [2] approach. In addition, by applying the procedure developed by Cheng [3], the WIP level for each product can be derived in each layer, according to the following procedure. Step 1 Input the standard system WIP level into Mansim software to perform the simulation. Step 2 Calculate the planned WIP level for each product by the following equation:

$$L_i = L \times \frac{P_i F_i}{\sum_i P_i F_i} \tag{1}$$

where L is the standard system WIP level; i the product index in system; L_i the planned WIP level of product i; P_i the proportion of product i in product mix; F_i the average flow time of product i. Step 3 Calculate the

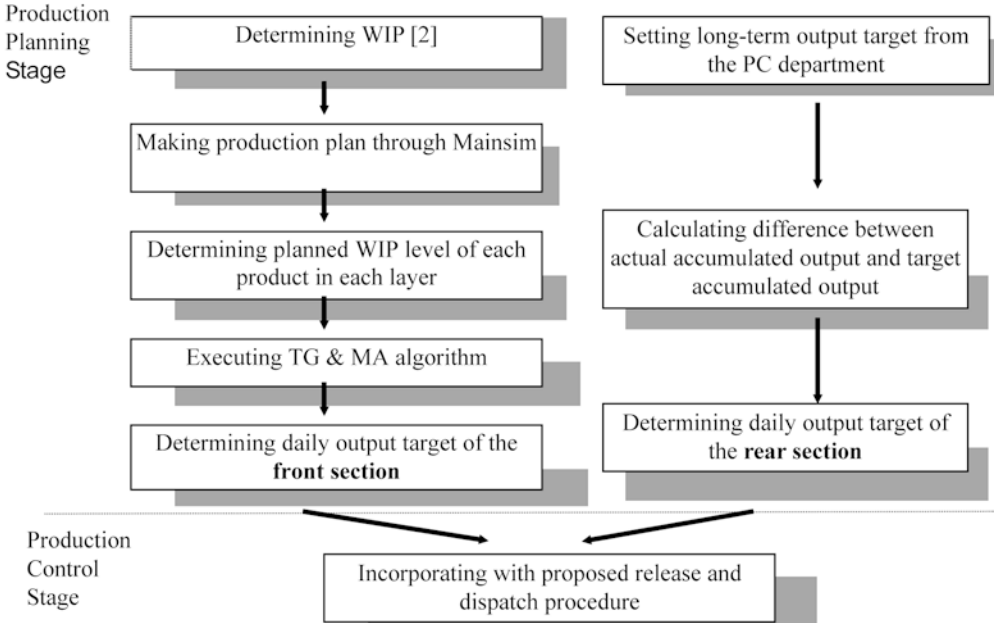

Fig. 1 Framework for the daily production

planned WIP level for each product in each layer by the following equation:

$$L_{i,j} = L_i \times \frac{F_{i,j}}{\sum_i F_{i,j}} \tag{2}$$

where j is the layer index visited by each product; $L_{i,j}$ the planned WIP level of product i in layer j; $F_{i,j}$ the average flow time of product i in layer j. Theoretically, a production system has a stable output rate and minimum total WIP level if the actual WIP distribution approaches the standard system WIP distribution. Because complex flow characteristics and variations exist in wafer fabrication, the actual WIP distribution may differ from the standard one. Therefore, in the front end, the TG & MA [4] algorithm is borrowed here to make the system approach to the standard WIP level. In the rear end, the model focuses on the achievement of the required output. The daily target of which is determined by the following equation.

$$AC_{ij} = \max\left(0, AP_{ij} - AA_{ij}\right) \tag{3}$$

where AC_{ij} is the daily production target of product i in layer j; AP_{ij} the planned accumulated output of product i in layer j; AA_{ij} the actual accumulated output of product i in layer j.

2.2 Production control stage

Lee [10] pointed out that the release policy, Fixed-WIP, has a significant effect on maintaining system stability. Therefore, the Fixed-WIP algorithm is employed here as the release policy. Because the layer is divided by the photolithography operation, it is usually the bottleneck of the system as well as a distribution centre. Thus, to develop a dispatch rule for the photolithography area is crucial. According to results in the first stage, the production target for each product in each layer is derived. The production target is the quantity of wafers that is supposed to be processed at the photolithography workstations each day. If more than one wafer lot of different products is queued in the photolithography workstation, the lot has a higher priority. The proposed procedure is as follows.

Step 1. Determine the dispatch priority in the front section by the following equation.

$$R_{ij} = Ph_{ij} - UB_{ij} \tag{4}$$

where Ph_{ij} is the actual output of product i in layer j, i.e. quantity of wafer lots of this product i in layer j which must be processed through a photolithography workstation. The dispatch priority is defined as: the less the value of R_{ij}, the higher priority of this kind of product i.

Step 2. Determine the dispatch priority in the rear section by the following equation.

$$R_{ij} = Ph_{ij} - AC_{ij} \tag{5}$$

The dispatch priority is defined as: the less the value of R_{ij}, the higher the priority of this kind of product i.

Step 3. If there are several lots that can be dispatched with the same R_{ij} value, a lot has a higher priority if its j value is the largest. If the j value remains the same, then FIFO (first in first out) is used to break the tie. Another issue encountered in wafer manufacturing is the frequent changes in masks on the photolithography equipment. This increases set-up times and the of waste equipment capacity. Industrial experience shows that a mask is mandatorily changed after processing four lots consecutively. Changing a mask not only avoids wasting capacity due to frequent set-ups but also maintains the quality of the product at a higher level. The change-of-mask influences line balance due to the blocking of the photolithography equipments. Therefore, the change-of-mask requirement is included in the proposed procedure. Figure 2 illustrates the dispatch procedure for photolithography equipments.

3 Simulation experiments

To evaluate the performance of the proposed daily production model, a simulation with a real-world numerical example is conducted in this investigation. A total of 33 workstations consisting of 150 machines are demonstrated in the simulation. The 23rd workstation is a photolithography workstation, and the 29th workstation is a sputter machine. The data of machines is shown in Table 1. For each scenario, 30 replicates of simulation with common random number streams are conducted. Each simulation run takes 330 days, with the first 90 days serving as a warm-up period. There are six product types, namely A, B, C, D, E, and F. Each product type visits the photolithography workstation 14, 13, 12, 11, 10, and 9 times, respectively. The product mix of A:B:C:D:E:F is 4:3:6:5:2:1. The set-up time is five minutes when a different recipe is required on the photolithography workstation. Lots with the same recipe are processed in a batch. The maximum batch size is six lots at furnace workstations. The recipe and corresponding processing time, mean time between failures (MTBF), and mean time to repair (MTTR) for each type of equipment are shown in Tables 1 and 2, respectively. The processing time, MTBF, and MTTR are all normally distributed. There are 23 layers divided by the photolithography workstations in the system. The detailed data are provided in Table 3.

Two indices: (1) achievement of required output and (2) the linear output are used to evaluate the performance of the proposed procedure. To evaluate the performance of the required output achievement, the variance of the actual output with the required output target is calculated. In order to measure the performance more accurately, the variance is divided into positive and negative variances. The positive variance is defined as

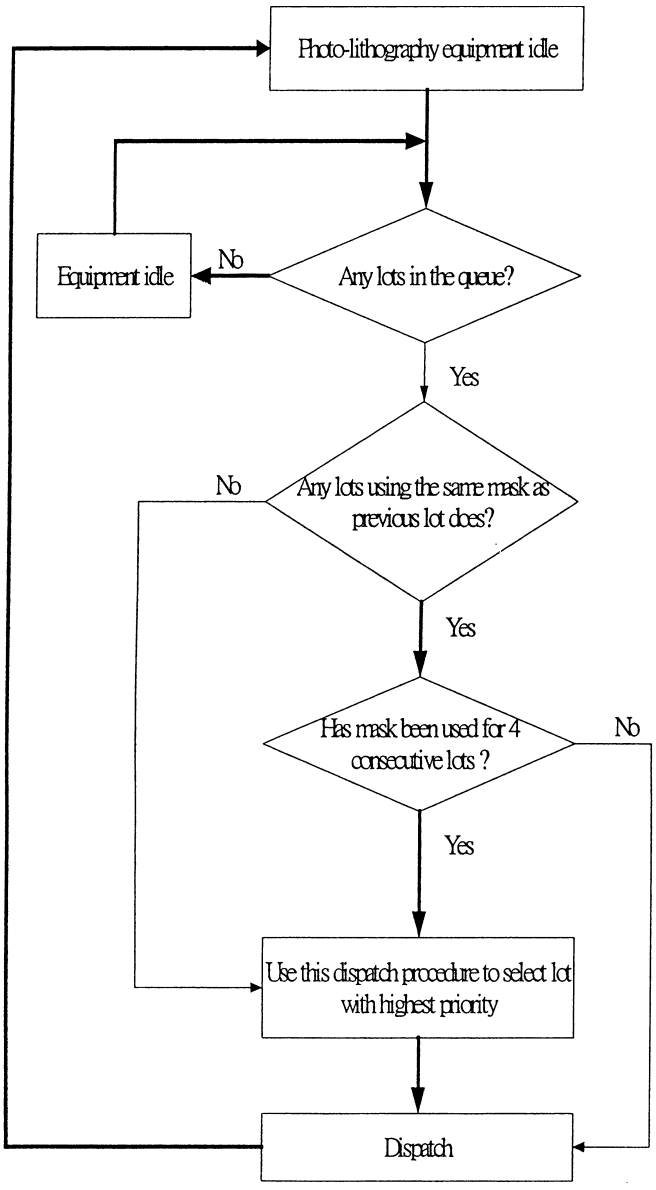

Fig. 2 A dispatch procedure for photolithography equipments

$$\sum_{m=4}^{11} (X_m - T_m)^2 \tag{6}$$

while $X_m \geq T_m$; where i is the month index; T_m the required output of m-th month; X_m the actual output of i-th month. The negative variance is defined as

$$\sum_{m=4}^{11} (Y_m - T_m)^2 \tag{7}$$

while $Y_m \leq T_m$; where Y_m is the actual output of m-th month. A Duncan's Multiple Range Test is used here to analyse indices. The grade is divided into three levels: A, B, and C. Table 4 shows that the proposed method obtains the best digits while the TB method obtains the worst. However, these three policies do not differ significantly. On the aspects of negative variances, Table 5 shows that the proposed model outperforms the other two methods significantly. The performance of the TB method appears much worse than of the others. From Table 4 and Table 5, it is concluded that the proposed method has a better performance in the achievement of the required output. Furthermore, the performance of line balancing is evaluated by measuring the degree of linear output. The degree of linear output is measured by calculating the standard deviation of lots completed every week. Table 6 shows that the proposed model does not outperform the other two methods in line balancing.

Table 1 Workstation data

Work station ID	Number of machines	Recipe type	Mean processing time	Variance of processing time	Production type
1	1	1	104	5.2	B
2	2	1	66	3.3	S
3	7	1	157	7.9	S
4	3	1	99	5.0	S
5	3	1	129	6.5	S
		2	144	7.2	
6	6	1	86	4.3	S
7	4	1	121	6.1	S
8	4	1	105	5.3	S
		2	99	5.0	
		3	105	5.3	
9	3	1	58	2.9	S
		2	58	2.9	
		3	62	3.1	
10	3	1	69	3.5	S
11	5	1	342	17.1	B
		2	342	17.1	
		3	480	24	
12	3	1	57	2.9	S
13	6	1	77	3.9	S
14	5	1	71	3.6	S
15	4	1	45	2.3	S
		2	272	13.6	
16	4	1	16	0.8	S
17	4	1	47	2.4	S
18	5	1	518	25.9	B
		2	415	20.8	
19	4	1	309	15.5	B
20	3	1	485	24.3	B
		2	505	25.3	
		3	505	25.3	
21	5	1	427	21.4	B
22	4	1	71	3.6	S
		2	70	3.5	
23	10	1	48	2.4	S
		2	60	3.0	
		3	50	2.5	
		4	48	2.4	
24	1	1	321	16.1	B
		2	326	16.3	
		3	334	16.7	
25	5	1	326	16.3	B
		2	322	16.1	
26	7	1	86	4.3	S
27	1	1	172	8.6	B
28	3	1	62	3.1	S
29	24	1	346	17.3	S
30	4	1	417	20.9	B
31	1	1	77	3.9	S
32	4	1	518	25.9	B
33	2	1	35	1.8	S

B: Batching production type
S: Serial production type

Table 2 Machine downtime data (min)

Workstation ID	MTBF	Variance of MTBF	MTTR	Variance of MTTR
1	14400	720	1440	72
10	2880	144	480	24
12	14400	720	1440	72
16	7200	360	300	15
17	7200	360	300	15
22	14400	720	1440	72
23	14400	720	1440	72
24	14400	720	1440	72
25	14400	720	1440	72
27	2700	135	330	16.5
28	14400	720	1440	72
32	14400	720	1440	72

MTBF: Mean time between failures
MTTR: Mean time to repair
Workstations not shown in this table are assumed to be available all the time

Table 3 Data for standard WIP in each layer (lot)

	Product A	Product B	Product C	Product D	Product E	Product F
Layer 0	3.22	2.46	4.84	3.94	1.56	0.78
Layer 1	8.49	6.03	11.99	9.74	3.85	1.94
Layer 2	1.60	1.37	2.49	2.06	0.84	0.44
Layer 3	9.69	0	0	0	4.40	2.20
Layer 4	0	0	11.44	0	0	0
Layer 5	0	3.50	0	5.69	0	0
Layer 6	2.98	0	0	0	0	0
Layer 7	0	3.80	0	7.22	0	0
Layer 8	0	0	7.25	0	0	0
Layer 9	0	2.53	0	4.04	1.58	0.79
Layer 10	5.33	3.54	0	5.99	2.38	0.87
Layer 11	5.11	0	0	0	0	0
Layer 12	1.53	0	2.25	0	0	0
Layer 13	0	0	2.30	0	0	0
Layer 14	0	0	5.24	0	0	0
Layer 15	1.44	1.13	2.15	1.81	0.71	0
Layer 16	3.03	2.25	4.49	3.78	1.50	0.80
Layer 17	3.91	2.65	5.62	4.26	1.69	0
Layer 18	2.30	1.70	0	0	0	0
Layer 19	0	0	0	0	0	1.17
Layer 20	2.29	0.90	0	0	0	0
Layer 21	2.11	2.38	3.27	2.81	1.15	0.62
Layer 22	1.74	1.28	2.39	2.07	0.82	0.43
Total	54.77	35.52	65.73	53.47	20.48	10.03

4 Conclusion

In this investigation, a procedure is proposed first to attain the goals of required output and then line balancing. The production characteristics of the front and rear sections in the wafer fabrication process are first analysed. The daily production targets are then determined respectively by different methods according to the different production characteristics. A dispatch policy for the photolithography is designed to achieve the daily production target. In addition, the Fixed-WIP discipline is used as the release policy. The simulation results show the trade-off between two objectives. Although the proposed model does not outperform the other two algorithms on both objectives, it is an appropriate approach for decision makers to increase the achievement of the required output without simultaneously reducing the line balancing performance dramatically.

Table 4 Average of monthly required output: positive variance (lot^2)

Policy	Average of positive variance	Duncan grouping
TB	461.73	A
TG & MA	459.43	A
Proposed Model	445.35	A

Table 5 Average monthly required output: negative variance (lot^2)

Policy	Average of negative variance	Duncan grouping
TB	2645.53	A
TG & MA	1210.07	B
Proposed model	958.23	C

Table 6 Average of standard deviation of output per week (lot)

Policy	Average of standard deviation of output per week	Duncan grouping
Proposed model	4.01	A
TG & MA	3.69	B
TB	3.36	C

References

1. Burman DY, Gurrola-Gal FJ, Nozari A, Sathaye S, Sitarik JP (1986) Performance analysis techniques for IC manufacturing lines. AT & T Tech J 65(4):46–57
2. Chan WS (1997) A relationship model for production performance indices in wafer fabrication factories. Master Thesis, National Chiao Tung University, Hsin-chu, Taiwan
3. Cheng CM (1996) The design of a due date assignment model for a wafer fabrication factory. Master Thesis, National Chiao Tung University, Hsin-chu, Taiwan
4. Chang SC, Lee LH, Pang LS, Chang YC, Lin PC, Chen TWY (1992) Daily target generation and machine allocation for integrated circuit fabrication. In: The Second International Conference on Automation Technology 4:47–52
5. Glassey CR, Resende MGC (1988) Closed-loop job release control for VLSI circuit manufacturing. In: IEEE Transactions on Semiconductor Manufacturing 1:36–46
6. Glassey CR, Resende MGC (1988) A scheduling rule for job release in semiconductor fabrication. Oper Res Letters 7:213–217
7. Graves RJ, Konopka JM, Milne RJ (1995) Literature review of material flow control mechanisms. Prod Plann Control 6(5):395–403
8. Kager PW, Lou S (1989) A robust production control policy for VLSI wafer fabrication. In: IEEE Transactions on Semiconductor Manufacturing 2:159–164

9. Lawton JW (1990) Workload regulating wafer release in a GaAa fab facility. In: International Semiconductor Manufacturing Science Symposium, pp. 33–38
10. Lee KJ (1995) The construction of a production planning system for wafer fabrication factories. Master Thesis, National Chiao Tung University, Hsin-chu, Taiwan
11. Li S, Tom T, Donald CW (1996) Minimum inventory variability schedule with applications in semiconductor fabrication. IEEE Transactions on Semiconductor Manufacturing 9:145–149
12. Lin Y-H, Lee C-E (2001) A total standard WIP estimation method for wafer fabrication. Eur J Oper Res 131:78–94
13. Lou SXC (1989) Optimal control rules for scheduling job shops. Ann Oper Res 17:233–248
14. Lou SXC, Kager PW (1989) A robust production control policy for VLSI wafer fabrication. In: IEEE Transactions on Semiconductor Manufacturing 2(4):159–164
15. Miller DJ (1990) Simulation of a semiconductor manufacturing line. ACM 33(10):99–108
16. Roderick LM, Philips DT, Hogg GL (1992) A comparison of order release strategies in production control systems. Int J Prod Res 30(3):611–626
17. Wang TH (1994) Design and analysis of a short term scheduling method for semiconductor manufacturing. Master Thesis, National Taiwan University, Taipei, Taiwan
18. Wein LM (1988) Scheduling semiconductor wafer fabrication. In: IEEE Transactions on Semi-conductor Manufacturing 1(3)115–130
19. Yan HS, Lou SS, Gardel A, Deosthali P (1996) Testing the robustness of two-boundary control policies in semiconductor manufacturing. In: IEEE Transactions on Semiconductor Manufacturing 9(2):285–288