

The Changing Effect of N_2/O_2 Gas Flow Rate Ratios on Ultrathin Nitrogen-Enriched Oxynitride Gate Dielectrics

Kow-Ming Chang, Wen-Chih Yang, Chu-Feng Chen, and Bing-Fang Hung

Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu 30050, Taiwan

We report the growth of an ultrathin 1.0 nm (equivalent oxide thickness = 0.86 nm) oxynitride gate dielectric by rapid thermal processing (RTP) in high- N_2 but low- O_2 gas flow ambient. The effect of the changing N_2/O_2 gas flow ratio on the characteristics of oxynitride films was investigated. High-quality oxynitride film could be formed by RTP in an optimum N_2/O_2 gas flow ratio of 5/1. Detailed characterization (transmission electron microscopy, *J-E* capacitance-voltage, stress-induced leakage current, charge-trapping properties) demonstrated the high quality of the oxynitride dielectric and showed that low leakage current density $J_g = 0.1 \text{ A/cm}^2$ at 1 V, was 1.85 orders of magnitude lower than that of SiO_2 . These improvements are attributed to the presence of nitrogen at the interface and in the bulk of the oxynitride.

© 2004 The Electrochemical Society. [DOI: 10.1149/1.1688799] All rights reserved.

Manuscript submitted July 14, 2003; revised manuscript received November 14, 2003. Available electronically March 19, 2004.

Highly reliable and aggressively scaled gate dielectric films (equivalent oxide thickness, EOT ≤ 1.0 nm) are necessary for developing complementary metal oxide semiconductor (CMOS) technologies in the sub-50 nm regime. However, when the thickness of SiO_2 is reduced below 2 nm, as for ultrathin oxides, important concerns of gate leakage and device reliability arise. ¹⁻³ For these reasons, alternative gate dielectrics must be considered. In the course of searching for such an alternative gate dielectric, ultrathin NH₃-nitride SiO₂, N₂O/NO oxynitride, N/O stack, plasma-nitrided SiO₂, and high-k dielectrics have been widely studied as the promising replacements for thermal oxide as gate dielectrics, while maintaining a low gate leakage and increased capacitance for future sub-50 nm CMOS devices. 4-18 Desirable gate dielectrics should have good uniformity, small defect density, and high dielectric strength; they should endure hot-electron injection for maintaining device reliability. As mentioned above, much work in this field has been focused on the nitridation of SiO2. NH3-nitrided SiO2 films can be effectively used to increase the proportion of incorporated N atoms; increasing the fixed charge and interface trap densities is unavoidable, due to the generation of electron traps related to -NH_x, -H, and -OH bonds introduced from NH₃. ⁴ The NH₃-nitrided films have also been reported to show degraded mobility due to heavy nitridation and increased electron trapping.⁵ N₂O and NO have been proposed as alternatives without the disadvantages of NH3 for oxidation and nitridation; the resulting films exhibit favorable electrical characteristics; however they do not have enough nitrogen (only \sim 1-2 atom %) at the dielectric silicon interface to prevent boron penetration. 6-9 The ultrathin nitride/oxide (N/O) stack has been investigated as a promising structure for suppressing leakage current and boron penetration, while maintaining the excellent oxide/Si interface. ^{10,11} The results of such investigations indicate that dielectric films formed by N/O stacks have higher nitrogen concentrations in both the bulk of the film and at the dielectric-silicon interface. However, most of the proposed N/O stacks are currently thicker than 1.6 nm, making them inappropriate for future sub-50 nm ultra large scale integrated (ULSI) technology. Recently, remote plasma nitridation (RPN) and decoupled plasma nitridation (DPN) of SiO₂ have been considered. 12-14 Although plasma nitridation reduces gate leakage by incorporating nitrogen on the top surface of the SiO2 dielectric, plasma-induced damage and the fixed charge associated with nitrogen incorporation cause a large Vt shift and transconductance degradation, which represent important disadvantages of the method. Recently, HfO2 and ZrO2 have been considered as promising high-k dielectrics. Although superior electrical characteristics of HfO₂ and ZrO₂ have been demonstrated, these high-k materials have

the disadvantage of low crystallization temperature, poor interface quality, and very poor thermal stability. ¹⁵⁻¹⁸ Various kinds of gate dielectrics have been investigated, but so far, none has been successful as the next generation gate dielectric to replace SiO2. It is technologically important to find a near-term solution to ensure the scalability in CMOS technology. 35 nm gate length CMOS technology has been reported with 1.0 nm oxynitride gate dielectrics formed by base oxide formation and NO gas annealing. ¹⁹ It has been found that the thinning of base oxide thickness should still be effective for current drive improvement, even in the region of less than 1.0 nm base oxide thickness. However, it has been found difficult to realize both (i) the thinning of the physical dielectric thickness and (ii) the incorporation of much more nitrogen into the gate dielectric simultaneously by the NO gas annealing method. Hence, oxynitride growth processes that can provide defect-free SiO2/Si interface and improved electrical characteristics must be established to solve these problems and achieve an ultrathin film (physical thickness <1.0 nm) with enhanced nitrogen incorporation. This paper develops a new technique for fabricating ultrathin oxynitride films down to a physical thickness of 1 nm by RTP in a high N₂ but low O₂ gas flow rate ambient (RTNO) to achieve a nitrogen-rich oxynitride film with nitrogen located away from SiO2/Si interface and to reduce the leakage current. Then, the optimum conditions of the growth of oxynitride films by RTNO, and their effects on the electrical characteristics are also demonstrated.

Experimental

pMOS capacitors with high quality 1.0 nm thick RTP oxynitride film was fabricated using a compatible 0.13 µm CMOS processing technology. The 3-5 Ω cm n-type silicon (100) wafers were cleaned by the standard RCA clean. The wafers were then washed in 1% HF acid immediately prior to dielectric film growth. The 1.0 nm thick nitrogen-rich gate oxynitride film was grown by RTP with a $N_2/O_2 = 1/1, 3/1, 5/1, \text{ and } 10/1 \text{ (slm)}$ gas flow ratios at 900°C for 15 s. A schematic time-temperature profile of the RTP oxidation processing for capacitor fabrication is shown in Fig. 1. A comparison was made with an oxide film of approximately the same thickness grown by RTP in pure oxygen ambient, gas flowing at 2 slm at 900°C for 10 s. Then, polysilicon film was deposited in a conventional low pressure chemical vapor deposition (LPCVD) system and doped by boron implantation 15 keV 5×10^{15} /cm². After activating the impurities, nickel salicide was formed and borophosphosilicate glass (BPSG) was deposited. Finally, 500 nm Al was deposited and patterned to provide an electrode pad. The thickness of the ultrathin oxynitride film in this work, including the RTO SiO₂ film, was measured using both an ellipsometer with three angles of incidence (65°, 70°, and 75°) and high-resolution transmission electron microscopy (HRTEM). MOS capacitors were analyzed electrically.

^z E-mail: wzyang.ee89g@nctu.edu.tw

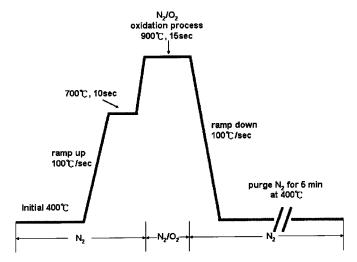


Figure 1. A schematics time-temperature profile of oxynitridation processing for the capacitor fabrication.

An HP 4156A semiconductor parameter analyzer and HP 4284A LCR meter was used to obtain the intrinsic properties of the gate dielectrics such as current-voltage (I-V), high frequency capacitance-voltage (C-V) curves, and reliability on 100×100 μ m² capacitors under 100 KHz signal frequency operation.

Results and Discussion

Figure 2 shows an high resolution TEM (HRTEM) micrograph of the oxynitride film. The physical thickness of the RTNO oxynitride films was determined by HRTEM as 1.0 nm. The HRTEM image provided sufficient contrast to discern the 1.0 nm thick oxynitride layer. The resulting oxynitride film is quite uniform and very smooth at the $SiO_{\scriptscriptstyle x}N_{\scriptscriptstyle \nu}/Si$ interface. Uniformity is very important, since it reduces anomalously large gate leakage currents through weak points where the oxide is thinner. Smoothness is also crucial to higher carrier mobility.²⁰ Figure 3a shows the thickness of the dielectric as a function of oxidation temperature for 15 s. Clearly, the film thickness linearly increases with as the oxidation temperature increases. The oxidation rate in N_2/O_2 mixed ambient was found to be slower than that in pure O_2 ambient. Obviously, the oxidation rate decreases as the N2/O2 gas flow rate ratio increases. This is attributed to the high N2 gas flow rate dilutes the O2 oxidation ambient, and the nitrogen atoms in the oxynitride film suppress oxygen diffusion, reducing the oxidation rate.²¹ Figure 3b shows the thickness of the dielectric vs. oxidation time relationship for various N_2/O_2 gas flow rate ratios at 900°C. It can be seen that the oxidation rate decreases as the N2/O2 gas flow rate ratio increases for different oxidation times. The different growth rates between RTO oxidation and RTP oxynitridation with various N2/O2 gas flow rate

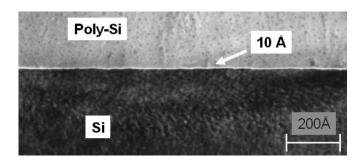


Figure 2. High-resolution cross-sectional TEM micrographs of MOS capacitor with 1.0 nm thick oxynitride gate dielectric. The capacitor was formed by depositing 1000 Å poly-Si/10 Å oxynitride on Si substrate.

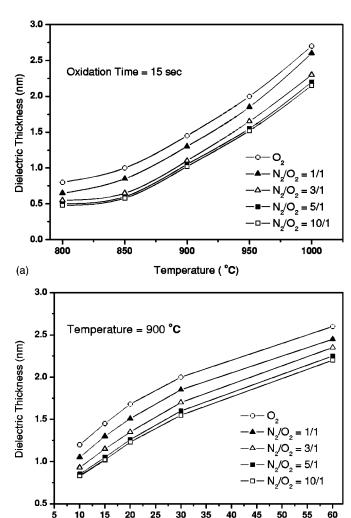


Figure 3. Oxynitride thickness variations as a function of (a, top) oxidation temperature and (b, bottom) oxidation time.

Oxidation Time (sec)

ratios, was attributed to the block effect of nitrogen atoms in the oxynitride film, as discussed above. The time dependence of oxynitride thickness shows a diffusion self-limited feature, and the average growth rate at 60 s (0.36 Å/s) is slower than that at 30 s (0.53 Å/s) for a $\rm N_2/O_2$ gas flow rate ratio of 5/1 (slm) sample at 900°C, because of the blocking effect of nitrogen. Although, a thinner 0.5 nm thick film could be obtained by RTP oxynitride when the growth temperature was below 800°C and the $\rm N_2/O_2$ gas flow rate ratio was increased to more than 5/1. However, such an ultrathin film is quite leaky and the leakage current was not acceptable for analysis, so the related data are not presented.

Figure 4 shows the high frequency C-V characteristics of p⁺-poly/oxide/n-Si MOS capacitors for oxidation conditions of $N_2/O_2=1/1,\ 3/1,\ 5/1,\ 10/1,$ and RTO. The area of capacitor is $100\times100\ \mu\text{m}$, and the small signal frequency is $100\ \text{KHz}$. It should be noted that sharp transitions are observed and the C-V curve of the RTO grown dielectric is greatly distorted since the leakage current through the dielectric is much larger than the nitrogen-incorporating oxynitride films. It is clear that the capacitance increases with the N_2/O_2 gas flow rate ratio, and a commensurate increase in drive current can be expected. The EOT = 0.86 nm of RTNO51 sample is extracted from the measured C-V in the strong accumulation region by a C-V simulator, which takes into account the quantum mechanical effect and the gate depletion

(b)

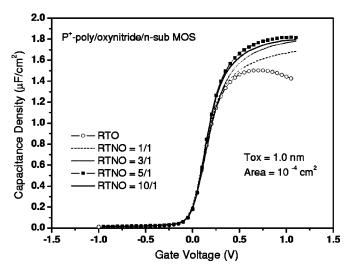


Figure 4. Measured 100 KHz high frequency C-V characteristics for 1.0 nm thick oxynitride and silicon dioxide MOS capacitors.

effect. 22,23 Additionally, it is obvious that flatband voltage shift of the RTNO oxynitride samples are quite small, which means that few fixed charges are trapped in the oxynitride bulk and its interfaces.²⁴ Finally, based on the agreement between the measured and calculated flatband voltages, there is no measured boron transport to the oxynitride/Si interface. Figure 5 shows the current density (J_g) vs. gate voltage characteristics of p+-poly/oxynitride/n-silicon(100) capacitors. Obviously, the oxynitride gate dielectric that was grown at an N₂/O₂ gas flow rate ratio of 5/1 shows a significantly lower gate leakage current than that of RTO SiO_2 . The RTNO = 5/1 sample has the lowest leakage current density, 0.1 A/cm² at $V_g = 1.0 \text{ V}$, and the current density is almost 1.85 orders of magnitude lower than 6.8 A/cm² at 1 V, as for RTO SiO₂. Additionally, RTNO51 provides a reduction of about one order of magnitude in the gate leakage current at 1 V + $V_{\rm FB}$, as compared to that of 16 Å thick pure SiO₂, even though the thickness of the oxynitride film is about 6 Å less than that of SiO₂. ¹⁰ The leakage current reduction can be explained such that the effective mass of the tunneling electron increases monotonically with increasing nitrogen concentration while the dielectric constant increases monotonically. 25,26 Hence, the im-

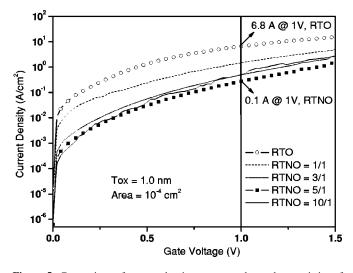


Figure 5. Comparison of current density vs. gate voltage characteristics of p⁺-polysilicon/oxynitride/n-Si capacitor structures with 1.0 nm thick oxynitride and RTO SiO₂.

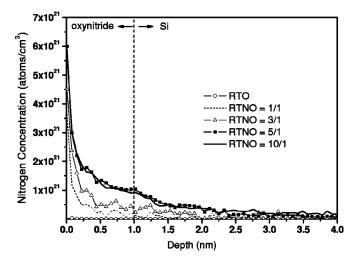


Figure 6. The SIMS depth profiles of nitrogen in the 1.0 nm thick RTNO oxynitride film. The ultrathin films under SIMS analyses were not capped polysilicon layer and the nitrogen concentration was evaluated immediately after the RTP oxidation process was finished.

provements provided by RTNO oxynitrides are thought to be due to the accumulation of nitrogen atoms. This result examines the gate leakage current as a function of the oxygen and nitrogen contents in ultrathin silicon oxynitride films. It is also reported that one striking aspect of the theoretical results is that, with as little as 10% nitrogen in the film, the direct tunneling current below 1 V can be reduced by more than two orders of magnitude compared to its pure oxide counterpart. Finally, a series resistance is observed in the high current density region of the J_g -V curve. This substantial series resistance at high current density should be the series resistance of the poly-gate, the ultrathin oxide, and the Si bulk substrate.

Figure 6 shows the secondary ion mass spectroscopy (SIMS) depth profiles of nitrogen in the RTNO oxynitride films and the RTO SiO_2 film. The oxynitride films analyzed by SIMS were not capped polysilicon layers and their nitrogen concentrations were evaluated immediately after the RTP oxynitridation process was finished. The layer composition evaluated by SIMS measurement indicates that a large amount of N atoms ($>6 \times 10^{21}$ atom/cm³) pile up at the top surface of the oxynitride film, and are distributed in the bulk oxynitride. This phenomenon proves that large amounts of nitrogen exist in the oxynitride film. The nitrogen concentrations of the RTNO = 5/1 oxynitride film and the RTO SiO₂ film were 1.05×10^{21} and 2.26×10^{18} atom/cm³, respectively, at the oxynitride/Si interface. The N concentration of the oxynitride film with RTNO = 5/1 was clearly about 2.5 orders of magnitude higher than that of the SiO₂ film. This observation confirmed that large amounts of nitrogen were present in the oxynitride film, which showed that almost all of the nitrogen atoms were confined near the oxynitride dielectric. Notably, the nitrogen concentration did not increase with the N2/O2 gas flow rate ratio up to 5/1, because an excess of N₂ gas seriously diluted the O2 gas, causing the RTP oxynitridation process to become similar to the nitridation process, and the process temperature of 900°C is too low for the nitridation process. Hence, the N concentration saturated when the N_2/O_2 gas flow rate ratio was more than 5/1. Additionally, it is also reported that boron penetration was suppressed enough by high nitrogen concentration (>1 \times 10²¹ atom/cm³) oxynitride even in 1.0 nm thick oxide.²⁷ The nitrogen concentration of RTNO51 at the oxynitride/Si interface was achieved at 1.05×10^{21} cm⁻³, implying that the boron penetration from p⁺ poly gate was enabled to be suppressed.

It is widely known that the addition of nitrogen in silicon oxide, or the addition of oxygen in silicon nitride, affects their reliability as a gate dielectrics. ^{28,29} Figure 7 shows the stress-induced leakage

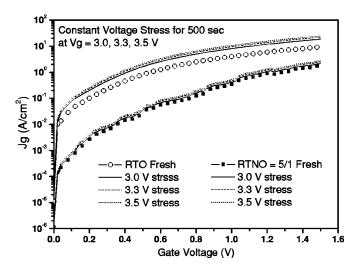


Figure 7. SILC of capacitors with 1.0 nm thick oxynitride or RTO SiO₂.

current (SILC) results after the application of constant voltage stresses of 3.0, 3.3, and 3.5 V for samples RTNO = 5/1 and RTO. Fresh J-V curves were measured before the samples were stressed. The leakage current density was also monitored during stressing to ensure consistent behavior from device to device. No significant stress-induced leakage current was observed in RTNO = 5/1 sample after stressing in a high electric field for 500 s. The much lower SILC of this oxynitride film can again be attributed to lower current fluence during the constant voltage stress, which in return causes less trap generation and thus a much lower SILC. Figure 8 shows the charge-trapping characteristics of n-MOS capacitors were stressed at a constant current density, 10 A/cm², for 500 s. No significant charge trapping occurred during stress, and the RTNO = 5/1 sample exhibits less electron trapping than the RTO sample. The reduced electron trapping characteristic leads to less field buildup within the oxynitride film, resulting in prolonged device lifetime. The charge-trapping properties dependence on the N_2/O_2 gas flow rate ratio which is quite obvious, because, as the N_2/O_2 ratio becomes higher, $\Delta V_{\rm g}$ becomes smaller. Figure 9 shows the $Q_{\rm BD}$ characteristics of RTNO ultrathin oxynitride films and conventional RTO SiO₂. p-MOS capacitors were stressed at a constant current until either the device broke or it had been stressed for

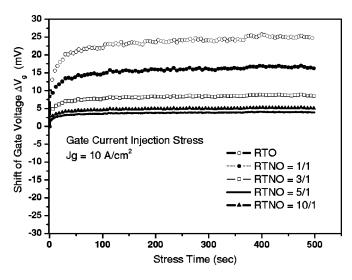


Figure 8. Charge-trapping characteristics by monitoring the change in gate voltage ($\Delta V_{\rm g}$) as a function of stress time.

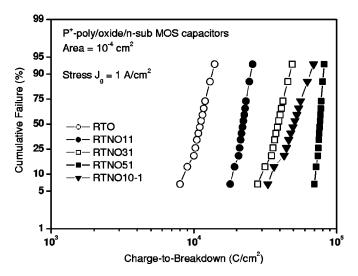


Figure 9. Charge-to-breakdown characteristics ($Q_{\rm BD}$) under constant current stress ($J=1~{\rm A/cm^2}$). The charge to breakdown of the oxynitride film grown in an N_2/O_2 gas flow ratio of 5/1 is significantly improved over that of RTO SiO₂ films.

 $10,\!000$ s. The $Q_{\rm BD}$ was found to increase as the N_2/O_2 ratio was increased. The $Q_{\rm BD}$ of the RTNO51 sample is one order of magnitude higher than that of the RTO $\rm SiO_2$ counterpart. The longer time-to-breakdown for the oxynitride film is primarily attributed to its lower leakage current, which causes less damage to the dielectric and thus contributes to a longer dielectric lifetime.

Conclusions

Ultrathin oxynitride dielectric films 1.0 nm thick were produced by RTP in mixed ambient with high $\rm N_2$ but low $\rm O_2$ gas flow rates. Such films exhibit a lower leakage current, a larger $\rm \it Q_{BD}$, and less charge trapping and trap generation than their RTP $\rm SiO_2$ counterpart. The leakage current of RTNO = 5/1 sample was as much as 1.85 orders of magnitude lower than that of their RTO $\rm SiO_2$ counterpart. These results suggest that the oxynitride film may be considered as a potential candidate for alternative gate dielectric for advanced CMOS devices.

Acknowledgments

The authors thank the National Science Council of the Republic of China, Taiwan, for financially supporting this research under contract no. NSC-91-2215-E-009-014.

National Chiao-Tung University assisted in meeting the publication costs of this article.

References

- 1. J. H. Stathis and D. J. DiMaria, Tech. Dig. Int. Electron Devices Meet., 1998, 167.
- N. Yang, W. K. Henson, and J. J. Wortman, IEEE Trans. Electron Devices, 47, 1636 (2000).
- 3. A. Meinertzhagen, C. Petit, D. Zander, O. Simonetti, T. Maurel, and M. Jourdain, *J. Appl. Phys.*, **91**, 2123 (2002).
- A. Teramoto, H. Umeda, H. Tamura, Y. Nishida, H. Sayama, K. Terada, K. Kawase, Y. Ohno, and A. Shigetomi, J. Electrochem. Soc., 147, 1888 (2000).
- S. C. Song, H. F. Luan, C. H. Lee, A. Y. Mao, S. J. Lee, J. Gelpey, S. Marcus, and D. L. Kwong, in *Tech. Dig. Symp. VLSI Technol.*, 1999, 137.
 M. L. Green, E. P. Gusev, R. Degraeve, and E. L. Garfunkel, *J. Appl. Phys.*, 90,
- 2057 (2001).Y. Okada, P. J. Tobin, P. Rushbrook, and W. L. DeHart, *IEEE Trans. Electron*
- Devices, **ED-43**, 191 (1994).
- Y. Suizu, M. Fukumoto, and Y. Ozawa, J. Electrochem. Soc., 148, F51 (2001).
 S. M. Shank, W. F. Clark, and W. J. Hodge, J. Electrochem. Soc., 149, G532 (2002).
- Y. Wu, Y. M. Lee, and G. Lucovsky, *IEEE Electron Device Lett.*, EDL-21, 116 (2000).
- 11. C. H. Chen, Y. K. Fang, C. W. Yang, S. F. Ting, Y. S. Tsair, M. F. Wang, T. H. Hou,

- M. C. Yu, S. C. Chen, S. M. Jang, Douglas C. H. Yu, and M. S. Liang, *IEEE Trans. Electron Devices*, **ED-48**, 2769 (2001).
- C. H. Chen, Y. K. Fang, W. Yang, S. F. Ting, Y. S. Tsair, M. C. Yu, T. H. Hou, M. F. Wang, S. C. Chen, C. H. Yu, and M. S. Liang, *IEEE Electron Device Lett.*, EDL-22, 378 (2001).
- H. N. Al-Shareef, A. Karamcheti, T. Y. Luo, G. Bersuker, G. A. Brown, R. W. Murto, M. D. Jackson, H. R. Huff, D. Lopez, C. Olsen, and G. Miner, *Appl. Phys. Lett.*, 78, 3875 (2001).
- H.-H. Tseng, Y. Jeno, P. Abramowitz, T.-Y. Luo, L. Hebert, J. J. Lee, J. Jiang, P. J. Tobin, G. C. F. Yeap, M. Moosa, J. Alvis, S. G. H. Anderson, N. Gave, T. C. Chua, A. Hegedus, G. Miner, J. Jeon, and A. Sultan, *IEEE Electron Device Lett.*, EDL-23, 704 (2002)
- J. Schaeffer, N. V. Edwards, R. Liu, D. Roan, B. Hradsky, R. Gregory, J. Kulik, E. Duda, L. Kulik, E. Duda, L. Contreras, J. Christiansen, S. Zollner, P. Tobin, B.-Y. Nguyen, R. Nieh, M. Ramon, R. Rao, R. Hegde, R. Rai, J. Baker, and S. Voight, J. Electrochem. Soc., 150, F67 (2003).
- M. Houssa, J. L. Autran, V. V. Afanas'ev, A. Stesmans, and M. M. Heyns, J. Electrochem. Soc., 149, F181 (2002).
- S. J. Lee, C. H. Lee, Y. H. Kim, H. F. Luan, W. P. Bai, T. S. Jeon, and D. L. Kwong, in *Proceedings of Solid-State and Integrated-Circuit Technology Conference*, p. 303 (2001).
- 18. W. Vandervorst, B. Brijs, H. Bender, O. T. Conard, J. Petry, O. Richard, S. Van Elshocht, A. Delabie, M. Caymax, S. De Gendt, V. Cosnier, M. Green, J. Chen, in

- Proceedings of Plasma- and Process-Induced Damage, 8th International Symposium, p. 40 (2003).
- S. Inaba, K. Okano, S. Matsuda, M. Fujiwara, A. Hokazono, K. Adachi, K. Ohuchi, and H. Suto, Tech. Dig. - Int. Electron Devices Meet., 2001, 641.
- T. Yamanaka, S. J. Fang, H. C. Lin, J. P. Snyder, and C. R. Helms, *IEEE Electron Device Lett.*, EDL-17, 178 (1996).
- 21. W. Ting, H. Hwang, J. Lee, and D. L. Kwong, Appl. Phys. Lett., 57, 2808 (1990).
- 22. K. Yang, Y. C. King, and C. Hu, in Tech. Dig. Symp. VLSI Technol., 1999, 77.
- 23. S.-H. Lo, D. A. Buchanan, and Y. Taur, *IBM J. Res. Dev.*, **43**, 327 (1999).
- Z. Wang, C. G. Parker, D. W. Hodge, R. T. Croswell, N. Yang, V. Misra, and J. R. Hauser, IEEE Electron Device Lett., EDL-21, 170 (2000).
- Hongyu Yu, Y. T. Hou, M. F. Li, and D. L. Kwong, IEEE Trans. Electron Devices, ED-49, 1158 (2002).
- 26. X. Guo and T. P. Ma, IEEE Electron Device Lett., EDL-20, 207 (1998).
- S. Inaba, T. Shimizu, S. Mori, K. Sekine, K. Saki, H. Suto, H. Fukui, M. Nagamine, M. Fujiwara, T. Yamamoto, M. Takayanagi, I. Mizushima, K. Okano, S. Matsuda, H. Oyamatsu, Y. Tsunashima, S. Yamada, Y. Toyoshima, and H. Ishiuchi, *Tech. Dig.* - Int. Electron Devices Meet., 2002, 651.
- K. Kushida-Abdelghafar, K. Watanabe, J. Ushio, and E. Murakami, Appl. Phys. Lett., 81, 4362 (2002).
- J. Ushio, T. Maruizumi, and K. Kushida-Abdelghafar, Appl. Phys. Lett., 81, 1818 (2002).