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The Copper Contamination Effect of Al_2O_3 Gate Dielectric on Si

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We have studied the Cu contamination effect on 4.2 nm thick Al_2O_3 metal-oxide semiconductor (MOS) capacitors with an equivalent-oxide thickness (EOT) of 1.9 nm. In contrast to the large degradation of gate oxide integrity of control 3.0 nm SiO_2 MOS capacitors contaminated by Cu, the 1.9 nm EOT Al_2O_3 MOS devices have good Cu contamination resistance with only small degradation of gate dielectric leakage current, charge-to-breakdown, and stress-induced leakage current. This strong Cu contamination resistance is similar to oxynitride (with high nitrogen content), but the Al_2O_3 gate dielectric has the advantage of higher κ value and lower gate dielectric leakage current.
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To reduce the circuit's RC delay from back-end metal lines and parasitic capacitors, Cu and low-κ dielectric are required. However, Cu diffusion into low-κ and front-end metal-oxide semiconductor field effect transistors (MOSFETs) is an important issue.[1-12] The Cu contamination from back-end Cu interconnects or the back-side wafer surface contaminated by Cu accumulates at the Si/SiO_2 interface[6-8] or reacts with Si to form silicide. The precipitate Cu at the oxide interface increases the subthreshold swing of MOSFETs,[7,9] shifts the threshold voltage, and degrades the gate leakage current.[10-12] The Cu silicide also increases the unwanted leakage current in the source-drain junction. To reduce Cu diffusion during back-end thermal cycling, a barrier metal under Cu and thick SiN between each intermetal layer (IML) dielectric are usually added. However, the added SiN of typically 50 nm has a large κ-value of 7.5 and degrades the total κ of combined IML dielectric and SiN. The increasing effective κ is unfavorable because it increases the circuit's back-end resistance-capacitance (RC) delay. In this paper, we have studied the Cu contamination effect in high-κ Al_2O_3 gate dielectric[13-16] with small equivalent-oxide thickness (EOT) of 1.9 nm, where the high-κ gate dielectric is important for continuously scaling down the nanometer-scale MOSFET. In contrast to the large degradation of gate oxide integrity in 3.0 nm thermal SiO_2, the smaller 1.9 nm EOT Al_2O_3 gate dielectric shows much better resistance to Cu contamination-related degradation on gate dielectric leakage current, charge-to-breakdown (Q_{BD}), and stress-induced leakage current (SILC). Therefore, the high-κ gate dielectric with Al_2O_3 ternary compound such as HfAlO or $LaAlO_3$ should have this additional advantage besides the high-κ value. This is the first study of Cu diffusion in high-κ Al_2O_3.

Experimental

Standard 4 in., p-type Si(100) wafers with a typical resistivity of ~10 Ω-cm were used in this study. After standard cleaning, the device active region was formed by thick field oxide and patterning. Then the ~4.2 nm Al_2O_3 was formed by physical-vapor deposition from an Al_2O_3 sputter source, oxidation at 400°C under O_2 ambient for 5 min, and annealed at N_2 ambient for 25 min. From the capacitance-voltage (C-V) measurement, a κ value of 8.5 and EOT of 1.9 nm were obtained. Then the gate electrode was formed by depositing a 300 nm thick aluminum by thermal evaporation and patterning, where the fabricated area of MOS capacitors is 100 × 100 μm. The Cu contamination to the Al_2O_3 metal-oxide semiconductor (MOS) devices was introduced by contacting the front side of devices into a $Cu(NO_3)_2$ solution with 10 ppb or 10 ppm concentration for 1 min followed by driving-in at 400°C N_2 annealing. The existence of Cu within gate SiO_2 by this contamination process was confirmed by secondary ion mass spectroscopy (SIMS) measurements reported previously,[11] where strong Cu accumulation is observed in both poly-Si and SiO_2. A more detailed Cu contamination process and discussion of degradation on gate dielectric integrity of SiO_2 and SiON can be found in our previous publications.[10-12] The Cu contamination effect was studied by current-density and voltage (J-V) measurements in high-κ Al_2O_3 gate dielectric MOS capacitors.

Results and Discussion

Figure 1 shows the J-(V_G-V_{FB}) characteristics of Al_2O_3 gate capacitors with ~4.2 nm physical thickness (1.9 nm EOT), where the V_{FB} is the flatband voltage obtained from the C-V measurement and quantum mechanical calculation. The V_{FB} of −0.7 and −0.85 V are obtained for Al_2O_3 and SiO_2 gate dielectric capacitors, respectively. There is no significant V_{FB} change after Cu contamination. This suggests that the Cu may behave as a neutral trap in the gate dielectric, consistent with our previous report.[12] For comparison, the J-(V_G-V_{FB}) characteristics of a 3.0 nm thick SiO_2 MOS device were also plotted. For samples without Cu contamination, the 1.9 nm EOT Al_2O_3 gate capacitor has *ca.* one order of magnitude lower leakage current than 3.0 nm SiO_2, which is the fundamental advan-

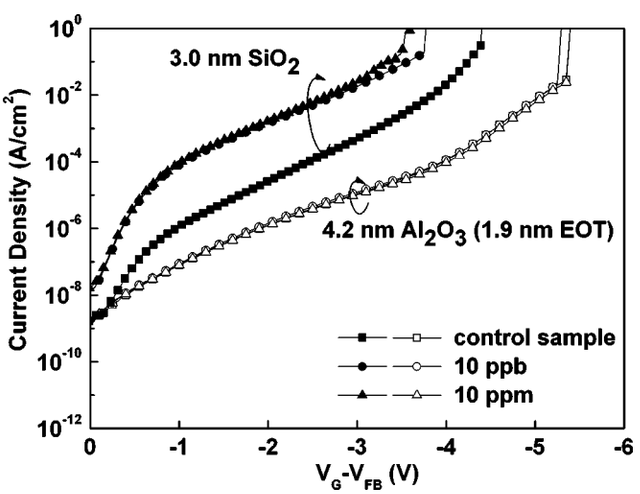

Figure 1. The J-(V_G-V_{FB}) characteristics of MOS capacitors with 4.2 nm Al_2O_3 gate dielectric (1.9 nm EOT) with or without Cu contamination. The MOS devices with 3.0 nm thermal SiO_2 are also added for comparison. The devices were contaminated by 10 ppb or 10 ppm Cu.

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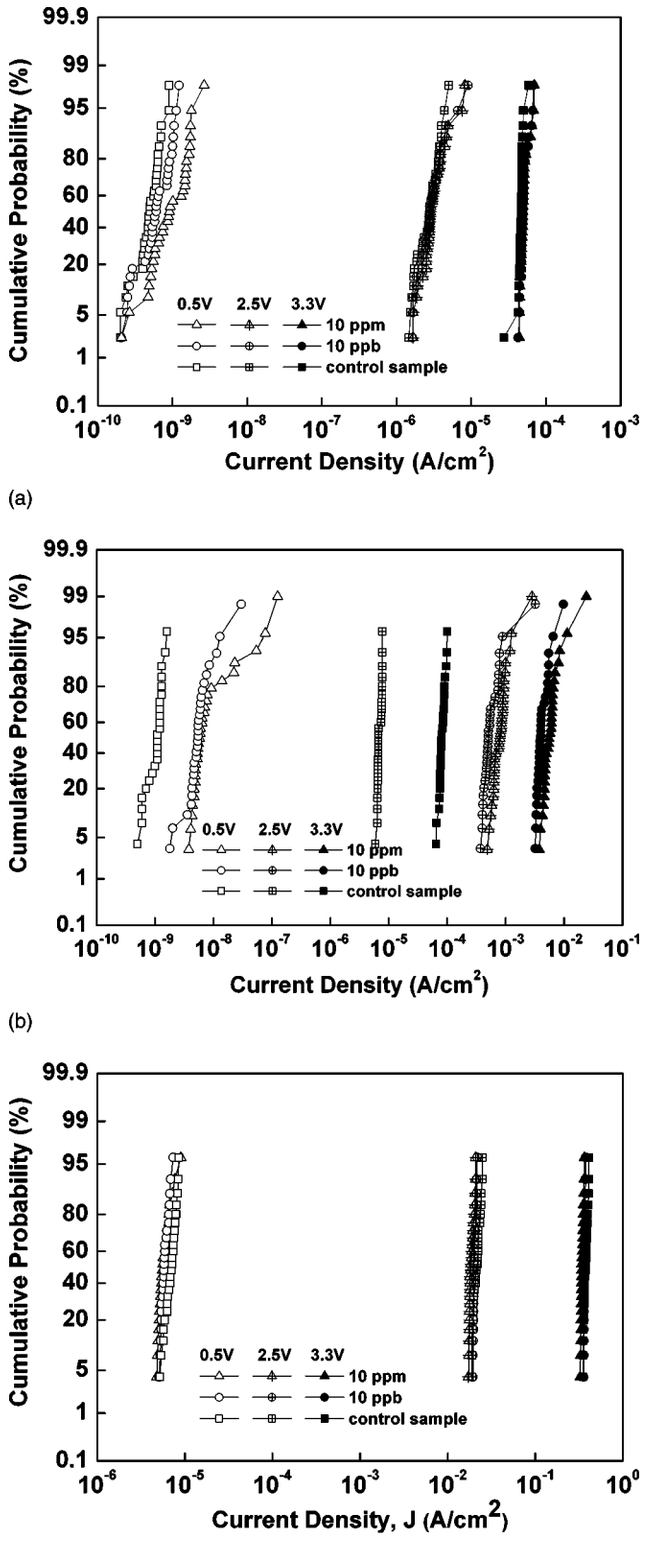

Figure 2. The distribution of leakage current density for (a) 4.2 nm Al_2O_3 gate dielectric (1.9 nm EOT), (b) 3.0 nm thermal SiO_2, and (c) 3.6 nm SiON with 23%N content (3.0 nm EOT) gate dielectrics with or without Cu contamination.

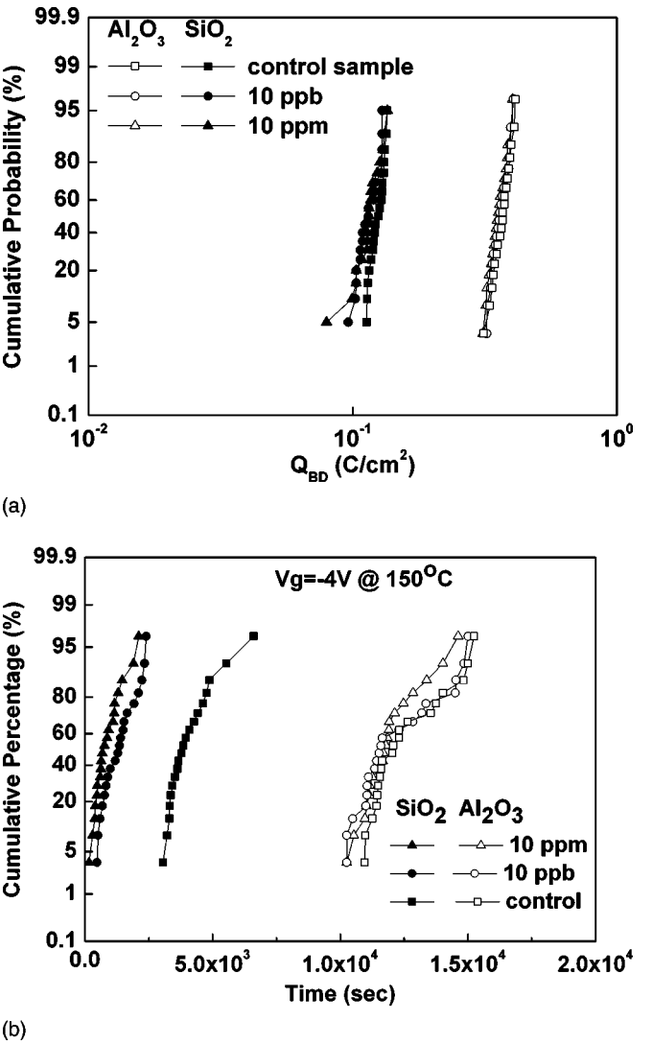

Figure 3. The (a) Q_{BD} and (b) t_{BD} distribution of 4.2 nm Al_2O_3 gate dielectric (1.9 nm EOT) MOS devices under different Cu contamination levels. The distributions of 3.0 nm SiO_2 MOS capacitors with or without Cu contamination are also added for comparison.

tage of high-κ gate dielectric. The Cu contamination in 3.0 nm SiO_2 control devices have a significant effect on gate dielectric leakage current, which was increased by *ca.* two orders of magnitude. The 10 ppb and 10 ppm Cu-contaminated SiO_2 control devices show almost identical leakage current before breakdown voltage (V_{BD}), although the V_{BD} is lower in 10 ppm contaminated devices than the 10 ppb case. Such effect was previously attributed to the Cu trap energy state inside the SiO_2 dielectric;[11] the leakage current shows an exponential relation with the trap energy in direct tunneling regime with less concentration dependence. In contrast to the large increasing leakage current (two orders of magnitude) in SiO_2 MOS capacitors contaminated by Cu, negligible leakage current increase in Al_2O_3 MOS capacitors is measured with high 10 ppm Cu contamination. The reason the Cu contamination has little effect on the Al_2O_3 gate dielectric may be due to the strong diffusion barrier property similar to Si_3N_4, where the Al_2O_3 can even be used as the diffusion barrier for a small H_2 molecule.[17]

Figure 2a-c further compares the cumulative leakage current distributions of the 4.2 nm Al_2O_3 (1.9 nm EOT), 3.0 nm SiO_2, and 3.6 nm oxynitride with 23% N content (3.0 nm EOT), respectively. The control gate oxide leakage current of 3.0 nm SiO_2 MOS device shows an increasing trend by one to two orders of magnitude at 0.5 and 2.5 V bias with increasing Cu concentration from 10 ppb to 10

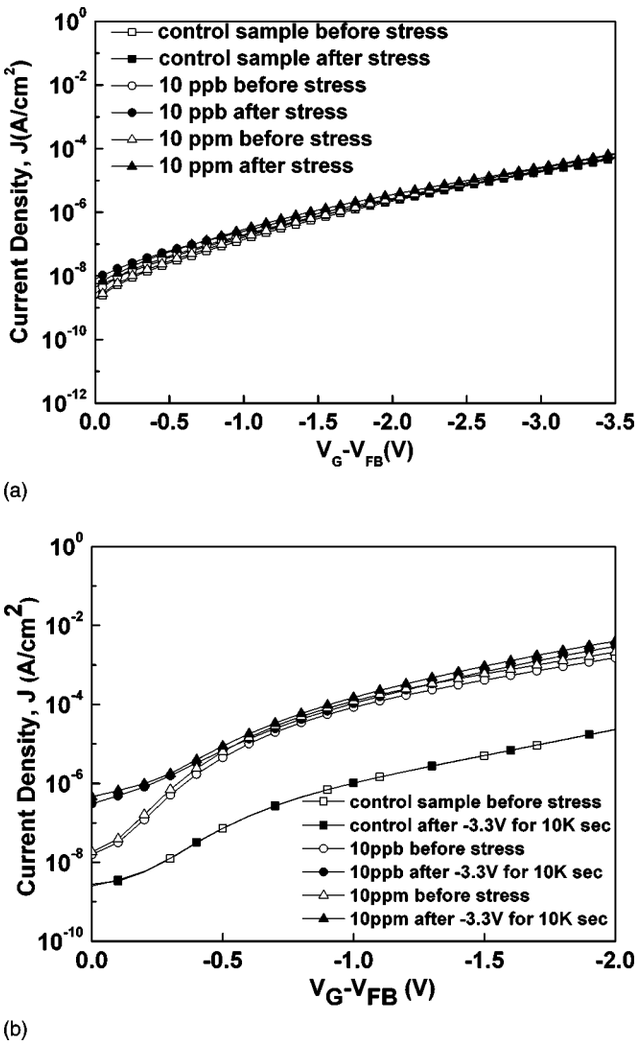

Figure 4. The stress effect on J-(V_G-V_{FB}) characteristics for MOS capacitors contaminated by Cu with (a) 4.2 nm Al_2O_3 gate dielectric (1.9 nm EOT) and (b) 3.0 nm SiO_2. The applied stress condition is at −3.3 V for 10,000 s.

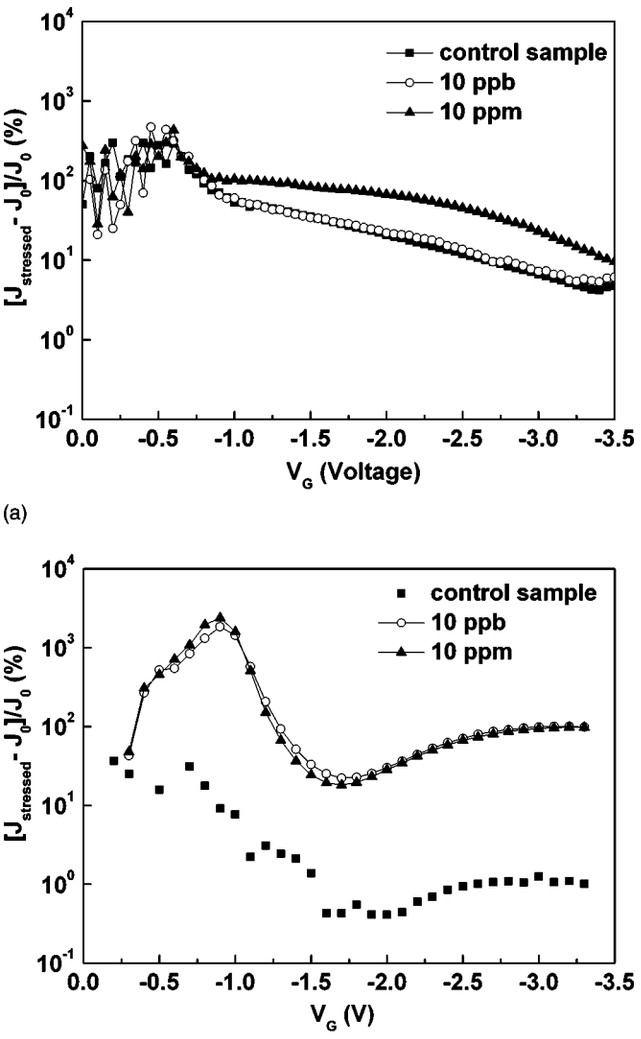

Figure 5. The stress and Cu contamination effect on ΔJ/J-V characteristics of (a) 4.2 nm Al_2O_3 gate dielectric (1.9 nm EOT) and (b) control 3.0 nm SiO_2 MOS capacitors.

ppm. In sharp contrast, only slightly increasing leakage current at lowest 0.5 V bias can be observed in the 4.2 nm Al_2O_3 (1.9 nm EOT). This increasing leakage current in the pretunneling region at low voltage is also previously observed in thick 5.0 nm SiO_2 and oxynitride with 16% N content,[10-12] which is attributed to the trap-assisted tunneling originated by neutral traps formed by Cu inside the oxide matrix. It is noticed that although the degradation of pre-tunneling leakage current is negligible for the 3.6 nm oxynitride with 23% N, the Al_2O_3 still has strong advantage of much smaller EOT of only 1.9 nm than the 3.0 nm EOT oxynitride (23% N). In addition, the κ-value of 8.5 for Al_2O_3 is also higher than the 4.7 κ-value for 23% N oxynitride,[10] which is important for gate dielectric application in nanometer-scale MOSFETs.

Figure 3a shows the comparison of Q_{BD} distribution of 4.2 nm Al_2O_3 gate dielectric (1.9 nm EOT) with the control 3.0 nm thermal oxide, with or without the Cu contamination. The good quality of control 3.0 nm oxide without contamination is evidenced from the high Q_{BD} of ~0.13 C/cm^2 (−4.3 V constant voltage stress) and close to the published data.[18] The Cu contamination effect on SiO_2 gate capacitor lowers the Q_{BD} with a wider distribution, which is consistent with the larger distribution of leakage current shown in Fig. 2b. In sharp contrast, the Cu contamination at both 10 ppb and 10 ppm has only small effects on Q_{BD} distribution of the 1.9 nm EOT Al_2O_3 gate dielectric and is free from the trail Q_{BD} distribution devices. This result is also consistent with the tight gate current distribution shown in Fig. 2a. It is noticed that the Q_{BD} value decreases rapidly with increasing stress voltage, and the mean Q_{BD} of 0.4 C/cm^2 for 4.2 nm Al_2O_3 gate dielectric, biased at a large voltage of 5.8 V, is also comparable to SiO_2 within the same order.[18] This suggests the excellent quality of high-κ Al_2O_3 gate dielectric. Figure 3b further shows the time-to-breakdown (t_{BD}) plot stressed at −4 V at 150°C. The larger t_{BD} decrease of Cu-contaminated SiO_2 than that of Al_2O_3 is due to the larger increase of leakage current in SiO_2 after contamination shown in Fig. 1.

The SILC is another important factor for gate dielectric reliability evaluation. Figure 4a and b shows the comparison of the stress effect on J-V characteristics for MOS capacitors with 4.2 nm Al_2O_3 gate dielectric (1.9 nm EOT) and 3.0 nm thermal oxides, respectively, with or without Cu contamination. In both cases, the applied stress condition is at −3.3 V for 10,000 s. Although the amount of injected charges is less for Al_2O_3 dielectric than SiO_2, this is due to the fundamental advantage for high-κ gate dielectric with largely

improved gate leakage current. Among all the Al_2O_3 and SiO_2 MOS devices with or without Cu contamination, the control 3.0 nm SiO_2 MOS capacitor has the smallest current change and better than the 4.2 nm Al_2O_3 MOS device under the same stress condition. This is due to the robustness of thermal SiO_2 where larger bulk oxide and interface defects are usually found in high-κ dielectric such as Al_2O_3. The amount of these weak defects increases under charge injection during constant voltage stress, which causes higher leakage current in MOS capacitors.

To further analyze the SILC effect, we have plotted the current change $(J_{stressed}\text{-}J_0)/J_0$ as a function of bias voltage in Fig. 5, which is more sensitive than the $J_{stressed}$-V plot shown in Fig. 4. For the uncontaminated Al_2O_3 and SiO_2 MOS devices shown in Fig. 5a and b, respectively, the Al_2O_3 dielectric capacitor has higher SILC current than the SiO_2 devices, even though the dielectric thickness (4.2 nm) for Al_2O_3 is thicker than the SiO_2 (3.0 nm). This is due to the higher bulk and interface defects in high-κ Al_2O_3 gate dielectric than thermal SiO_2. However, the SILC of $\Delta J/J_0$ increases rapidly in the SiO_2 devices even under the smallest Cu contamination of 10 ppb. The increasing SILC with Cu contamination is previously attributed to the formation of neutral traps inside the oxide and interface.[12] In contrast, the $\Delta J/J_0$ only increases slightly at 10 ppb Cu contamination and the amount of increase at 10 ppm Cu is still less than the SiO_2 case. The smaller amount of Cu-contamination-generated SILC in Al_2O_3 gate dielectric suggests the good diffusion barrier property and is also consistent with the smaller degradation on dielectric leakage current and Q_{BD} shown in Fig. 1 and 3.

Conclusion

We have studied the Cu contamination effects on gate dielectric integrity of 4.2 nm Al_2O_3 dielectric. By comparing with the control 3.0 nm SiO_2 MOS capacitors contaminated by Cu, much smaller degradation of gate dielectric leakage current, Q_{BD} and SILC is found in 1.9 nm EOT Al_2O_3 MOS devices. The much better resistance of Cu contamination in ultrathin 1.9 nm EOT Al_2O_3 MOS capacitor is the strong advantage for high-κ Al_2O_3 gate dielectric.

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