Journal of The Electrochemical Society, **151** (9) G606-G611 (2004)
0013-4651/2004/151(9)/G606/6/$7.00 © The Electrochemical Society, Inc.

Improvement in Leakage Current and Breakdown Field of Cu-Comb Capacitor Using a Silicon Oxycarbide Dielectric Barrier

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This work investigates in the first place, the improvement in leakage current and breakdown field of the copper metal-insulator-semiconductor (Cu-MIS) capacitor with a plasma-enhanced chemical vapor deposited (PECVD) amorphous silicon oxycarbide (α-SiCO, $k = 3.7$) dielectric barrier. This is followed by investigating the improvement in leakage current and breakdown field of the Cu-comb capacitor with a carbon-doped low-*k* PECVD organosilicate glass ($k = 3$) as the intermetal dielectric and an α-SiCO dielectric film as the Cu cap barrier. The leakage current and breakdown field of Cu-MIS and Cu-comb capacitors are dependent on the species of the dielectric barrier. The Cu-MIS and Cu-comb capacitors with an α-SiCO dielectric barrier exhibit a leakage current at least three orders of magnitude smaller than those with an amorphous silicon carbide (α-SiC, $k = 4.4$) dielectric barrier at an applied electric field of 1.6 MV/cm between 25 and 250°C. Moreover, the breakdown field of the Cu-MIS and Cu-comb capacitors with an α-SiCO dielectric barrier, measured at 200°C, are 60 and 25%, respectively, higher than that of the capacitors with an α-SiC barrier. The decreased leakage current and increased breakdown field of the Cu-MIS and Cu-comb capacitors with an α-SiCO dielectric barrier are attributed to the higher density, oxygen-improved film property, non-semiconductor behavior, and lower fringe- or surface-electric field of the α-SiCO dielectric film.
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Manuscript submitted November 10, 2003; revised manuscript received February 21, 2004. Available electronically August 11, 2004.

The interconnect resistance-capacitance (RC) delay is a dominant factor in determining the performance of integrated circuits beyond 0.18 μm node technology, in which the use of Cu metal and low-*k* dielectrics is indispensable in the back-end-of-line (BEOL) process. Cu metal reduces the electrical resistance of interconnect lines because of its low electrical resistivity; moreover, Cu line also exhibits a better electromigration resistance than conventional Al-based wires. Low-*k* dielectrics in the interconnect system reduce the wire capacitance, signal-propagation delay, cross talk noise between metal lines, and power dissipation of integrated circuits. While many low-*k* ($k < 3$) materials have been used as inter- and intralayer dielectrics (ILD), high dielectric constant ($k > 7$) silicon nitride is still the primary candidate for the Cu cap barrier and etching stop layer (ESL) required in the Cu damascene structure. It is desirable to replace silicon nitride with dielectric materials of lower *k* value ($k < 5$) to further reduce the effective dielectric constant of the Cu interconnect system. In recent years, amorphous silicon carbide (α-SiC), amorphous silicon nitricarbide. (α-SiCN), and amorphous silicon oxycarbide (α-SiCO) deposited by plasma-enhanced chemical vapor deposition (PECVD) using organosilicate gases have received extensive attention for applications as Cu cap-barrier and ESL in Cu interconnection scheme because of their lower k value, better etching selectivity with organosilicate glass (OSG), robust chemical mechanical polishing (CMP) strength, good photoresist poisoning resistance, higher antireflective ability, and superior properties as a Cu barrier/passivation layer in terms of Cu restraint, electromigration resistance, and Cu hillock density.[1-6] The fine-tuned α-SiC is better than α-SiCN and α-SiCO in the aspects of *k* value, etching selectivity, photoresist poisoning, antireflective coating lithography behavior, adhesion strength to Cu and OSG IMD, electrical property, and reliability performance.[2,3,7] However, the film stress of α-SiC is tensile or less compressive as compared with that of α-SiCN and α-SiCO, which results in a poor stack stability of Cu-OSG interconnect system and a degraded interface quality of α-SiC/OSG.[2,3,8] In this work, we investigated the improvement in leakage current and breakdown field of the copper metal-insulator-semiconductor (Cu-MIS) and Cu-comb capacitors with an α-SiCO dielectric barrier over those with an α-SiC dielectric barrier having a comparable compressive film stress.

Experimental

The leakage current and breakdown field of Cu-MIS and Cu-comb capacitors were measured on the TaN/Cu-gated MIS structure and 0.12/0.12 μm (linewidth/space) Cu-OSG single damascene structure, respectively. For the fabrication of Cu-MIS capacitor, 50 nm thick PECVD dielectric films were deposited on p-type, (100)-oriented Si wafers at 300-400°C, a gas pressure of 1-5 Torr, and a plasma power of 100-300 W using a parallel-plate system operated at 13.56 MHz. The flow rate ratio of 3MS $[(CH_3)_3SiH]$ precursor with He carrier gas was maintained at 2/5, while the flow rate of CO_2 reaction gas was controlled separately at 0 and 1200 sccm, which resulted in the 3MS-based α-SiC and α-SiCO films, respectively, with different elemental compositions. A Cu layer, 200 nm thick, was sputter-deposited on the α-SiC and α-SiCO dielectric films using a dc magnetron sputtering system; this was followed by reactive sputter deposition of a 50 nm thick TaN layer on the Cu surface in the same sputtering system without breaking the vacuum. The TaN film served as a passivation layer to prevent the Cu electrode from oxidation in the subsequent high-temperature processes or measurements. The metal electrodes with a circular area of 0.84 mm diameter were defined by a lift-off process to prevent unexpected deterioration of the dielectric films by chemical wet etching. To ensure good contact in electrical measurements, a 500 nm thick Al layer was thermally evaporated on the back surface of the Si substrate for all samples. The completed Cu-MIS capacitors were thermally annealed at 400°C for 30 min in an N_2 ambient. This annealing step eliminates the plasma-induced damage during the sputter deposition of the TaN/Cu electrodes. Figure 1 shows the schematic top and cross-sectional view of the Cu-comb capacitor test structure. A 40 nm PECVD 3MS-based α-SiCO ($k = 4.5$) ESL was deposited on the PECVD oxide ILD. A single level Cu damascene (metal 1) process with a 250 nm PECVD methylsilane-based carbon-doped low-*k* OSG as the IMD was employed to fabricate the Cu-comb capacitor. After patterning of 0.12/0.12 μm linewidth/space trenches in the OSG/ESL/ILD dielectric stack, the damascene Cu feature was electrochemically deposited on a 15 nm physical vapor deposited (PVD) TaN liner barrier. Following the Cu CMP,

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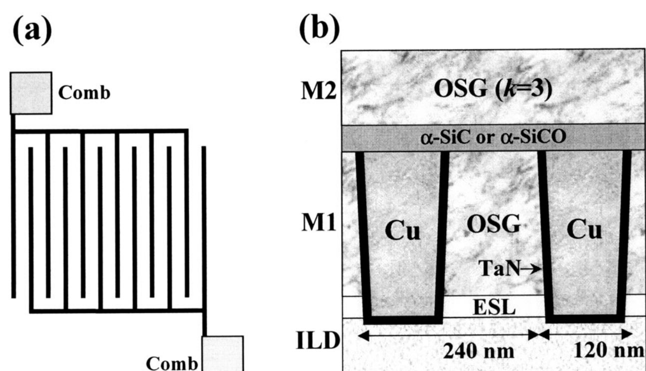

Figure 1. Schematic (a) top view and (b) cross-sectional view of the Cu-comb capacitor test structure.

the 3MS-based α-SiC or α-SiCO cap barrier was deposited in a PECVD system. Another layer of PECVD OSG was deposited for the next Cu damascene (metal 2) process.

An HP4145B semiconductor parameter analyzer was used to measure the leakage current and breakdown field of the Cu-MIS and Cu-comb capacitors. During the measurement, an N_2 purging was used to prevent possible oxidation of the Cu metal and moisture uptake in the dielectric films. Raphael modeling (provided by Avant! business unit) was used to obtain the distribution of electric field in the Cu-MIS and Cu-comb capacitors. Auger electron spectroscopy (AES) was used to obtain the chemical composition of the dielectric barrier films. The film thickness and refractive index were measured using an n&k analyzer at 633 nm wavelength, and the k value of the dielectrics was determined by the maximum capacitance of the Al-gated MIS capacitors measured at 1 MHz using a Keithley package 82 C-V measurement system. The film density was calculated directly by the ratio of mass to volume of the film, whereas the film mass was measured by an electronic microbalance and the film volume was calculated by the film thickness and the area of the substrate wafer. The film stress was measured using a well-calibrated thin-film stress analyzer.

Results and Discussion

Physical property of α-SiC and α-SiCO.—Table I shows the basic film properties of 3MS-based α-SiC and α-SiCO dielectrics studied in this work. Although the chemical composition indicates that the oxygen content in SiCO is much higher than that in SiC, both dielectrics have nearly the same deposition rate and compressive film stress. The compressive stress of about −200 MPa in the SiC and SiCO dielectric films is high enough to achieve a robust stack stability.[2,3] However, it is conceivable that the SiC may exhibit inferior thermal stability and electrical and barrier properties because of its lower density (*i.e.*, higher degree of porosity).[9,10] Nonetheless, the refractive index of the SiCO is lower than that of the SiC; this results in lower electronic-dielectric constant, and thus lower dielectric constant (at 1 MHz) of SiCO film because of the replacement of Si-C with Si-O bond and the higher electronegativity of oxygen atom.[11]

Table I. Basic film properties for 3MS-based α-SiC and α-SiCO dielectric barriers 50 nm thick used in this study.

Sample ID	SiC	SiCO
Structure	α-SiC	α-SiCO
Chemical composition	$SiC_{0.92}O_{0.04}$	$SiC_{0.97}O_{0.66}$
Deposition rate (nm/min)	100.4	102.6
Film stress (MPa)	−200	−210
Film density (g/cm^3)	1.24	1.80
Refractive index at 633 nm	2.04	1.72
Dielectric constant at 1 MHz	4.41	3.73

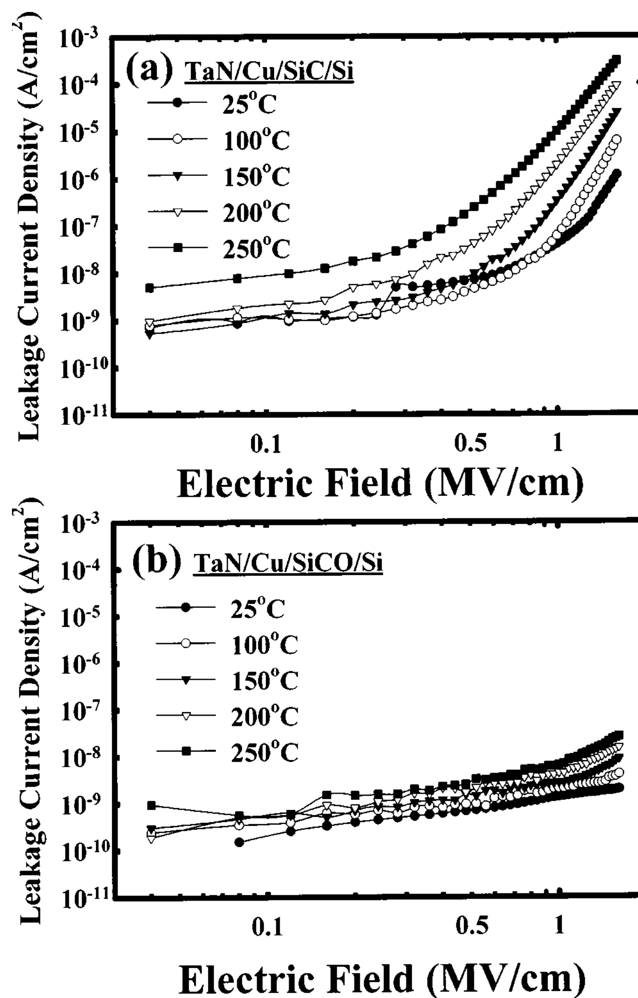

Figure 2. Leakage current density *vs.* electric field in a log-log plot, measured at various temperatures, for Cu-MIS capacitors with (a) α-SiC and (b) α-SiCO dielectric films.

Electrical property of Cu-MIS capacitor.—Figure 2 shows the leakage current of Cu-MIS capacitors with SiC and SiCO dielectrics measured at various temperatures. Generally, the leakage current of the SiCO sample is three orders of magnitude smaller than that of the SiC sample at an electric field of 1.6 MV/cm and at temperatures ranging from 25 to 250°C, presumably due to the higher density of the SiCO film (Table I). The higher density (*i.e.*, lower degree of porosity) of film prohibited the diffusion/drift of Cu owing to the miniature free volume.[10,12-16] Higher oxygen content in the α-SiCO dielectric film would also effectively reduce the film leakage current.[17] Because single-crystal SiC is a semiconductor with a bandgap of 2.3-3.0 eV, the polycrystal or amorphous SiC possibly also has a semiconductor nature of high conductivity. Therefore, it is natural to reduce the leakage current of SiC by doping with oxygen and making SiCO. From the log-log plot of the leakage current *vs.* electric field data, two different electric-field-dependent conduction mechanisms are observed in the Cu-MIS capacitors. First, all Cu-MIS capacitors exhibit ohmic conduction at low electric fields (<0.3 and <1 MV/cm for SiC and SiCO, respectively) because the leakage current (I) is linearly correlated with the electric field ($\mathbf{E}$),[18] and the current can be expressed by Eq. 1.[19] The ohmic conduction is carried by thermally excited electrons hopping from one isolated

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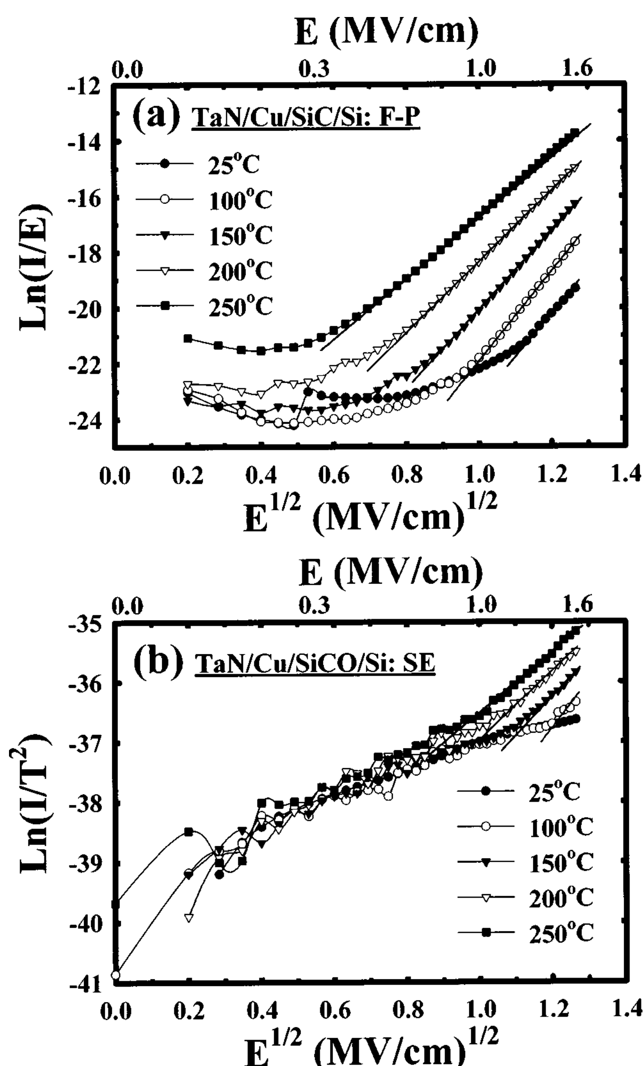

Figure 3. Conduction mechanism of (a) Frenkel-Poole emission in TaN/Cu/α-SiC/Si and (b) Schottky emission in TaN/Cu/α-SiCO/Si samples.

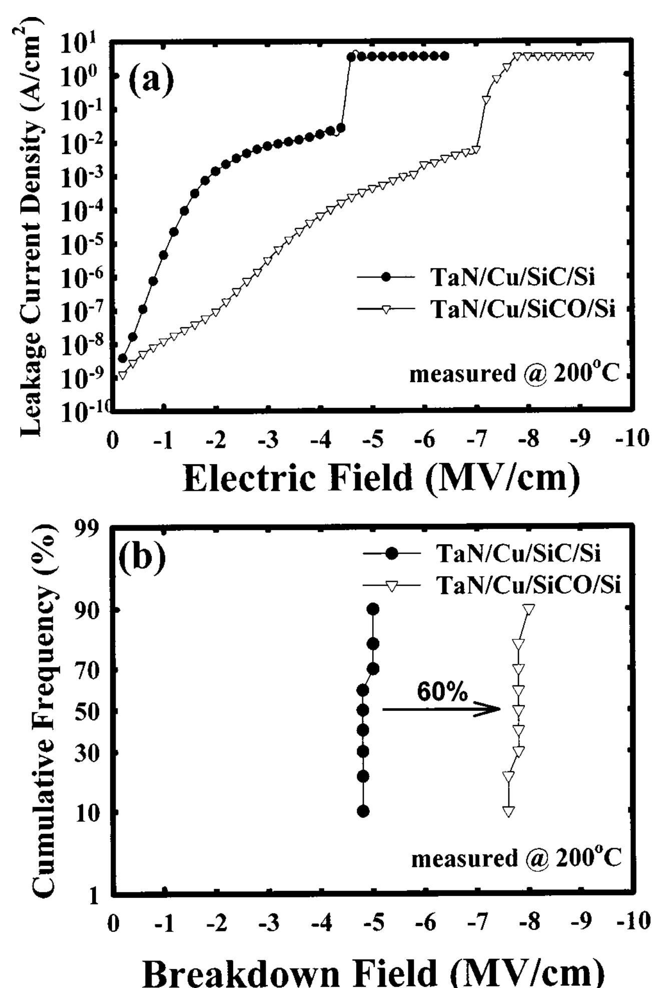

Figure 4. (a) Leakage current density *vs.* electric field and (b) distribution of breakdown field for the α-SiC and α-SiCO Cu-gated MIS capacitors measured at 200°C.

state to the next.[18,19] However, at high electric fields (>0.3 and >1 MV/cm for SiC and SiCO, respectively), the Cu-MIS capacitors with SiC and SiCO dielectrics exhibit different slopes in their I-$\mathbf{E}$ plot, particularly above 200°C. This implies that the SiC and SiCO samples have different conduction mechanisms at high electric fields. From some replots of the known conduction mechanisms in dielectrics,[18,19] we found that the SiC sample exhibits Frenkel-Poole (F-P) emission, while the SiCO sample reveals Schottky emission (SE), as shown in Fig. 3. The F-P emission shows $\mathrm{Ln}(I/\mathbf{E})$ linearly correlated with $\mathbf{E}^{1/2}$ (Fig. 3a), and the current can be expressed by Eq. 2.[18,19] The SE conduction shows $\mathrm{Ln}(I/T^2)$ linearly correlated with $\mathbf{E}^{1/2}$ (Fig. 3b), and the current can be expressed by Eq. 3.[19] The F-P emission is due to field-enhanced thermal excitation of trapped electrons in the dielectrics into the conduction band, while the SE conduction is derived from the thermionic emission across the metal-dielectric interface or the dielectric-semiconductor interface[18-20]

$$\text{Ohmic} \quad I \sim \mathbf{E}\exp(-\Delta E_{ae}/kT) \quad [1]$$

$$\text{FP} \quad I \sim \mathbf{E}\exp(2\beta\mathbf{E}^{1/2}/kT - q\Phi_B/kT) \quad [2]$$

$$\text{SE} \quad I \sim T^2\exp(\beta\mathbf{E}^{1/2}/kT - q\Phi_B/kT) \quad [3]$$

where ΔE_{ae} is the activation energy of electron, β represents $(q^3/4\pi\varepsilon)^{1/2}$, and ε is the dielectric dynamic permittivity, k is the Boltzmann constant, q is an electron charge, and Φ_{FP} is the barrier height of trap potential well, and Φ_{SE} is the barrier height of metal/dialectric interface.[19] The F-P emission and higher leakage current of the SiC sample are presumably due to the presence of defects and/or traps[18-20] possibly resulting from the film lower density. Clearly, temperature enhances the F-P emission and SE conduction in the SiC and SiCO samples, respectively (Fig. 3). Figure 4 shows the leakage current and breakdown field for the SiC and SiCO Cu-gated MIS capacitors measured at 200°C. The measurements were performed with the MIS capacitors biased in the accumulation region. The breakdown field is defined as the field strength such that the leakage current of the MIS capacitor reaches the current limit of the HP4145B semiconductor parameter analyzer. Notably, the breakdown field of the SiCO sample is about 60% higher than that of the SiC sample. This increase in breakdown field is presumably due to the enhanced Si-O bond that has a high thermochemical energy.[21] Moreover, the oxygen atoms and the higher density of the SiCO dielectric film would also effectively increase the breakdown field.[11,18] In addition, the lower k value of the SiCO film would induce lower fringe-electric field around the metal-gate corner, as illustrated in the model shown in Fig. 5, which is derived from the high-k gate dielectrics used in the front-end-of-line (FEOL) technology.[22] It is conceivable that the lower fringe-electric field in the SiCO film would result in lower leakage current and higher breakdown field for the SiCO sample.

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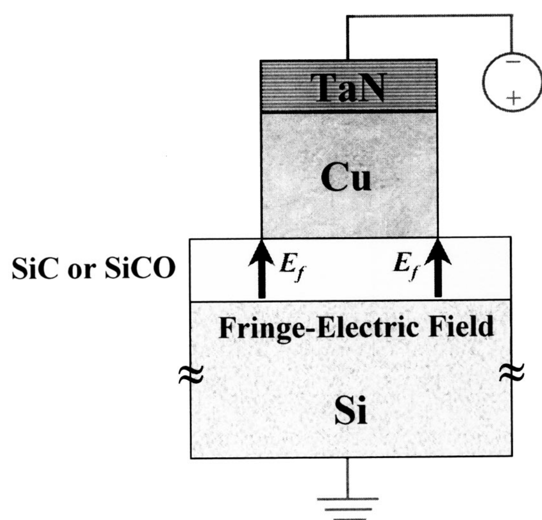

Figure 5. Proposed fringe-electric field in the MIS capacitor.

Figure 6 shows the fringe-electric field obtained from Raphael simulation for the Cu-gated MIS capacitors of SiC as well as SiCO dielectric biased with an electric voltage of 10 V, which would produce an electric field of 2 MV/cm in the dielectric layer of the Cu-MIS capacitor. Notably, the SiC sample exhibits about 10% increase of fringe-electric field near the Cu electrode as compared with the SiCO sample.

Electrical property of Cu-comb capacitor.—Figure 7 shows the leakage current, measured at various temperatures, for the Cu-comb capacitors with SiC as well as SiCO dielectric cap barriers. Notably, the dependence of leakage current on the cap barrier dielectric material implies that the dominant leakage paths are not in the bulk OSG but in the bulk cap barrier and along the cap barrier/OSG interface (CMP surface).[23,24] That the leakage current of the SiCO sample at a field of 1.6 MV/cm between 25 and 250°C is at least three orders of magnitude smaller than that of the SiC sample, may be attributed to the semiconductor nature of SiC and the better electrical property of the SiCO film, as studied in the previous paragraph using the MIS capacitors. Moreover, the CMP surface leak-path may be efficiently eliminated in the SiCO sample because both the SiCO

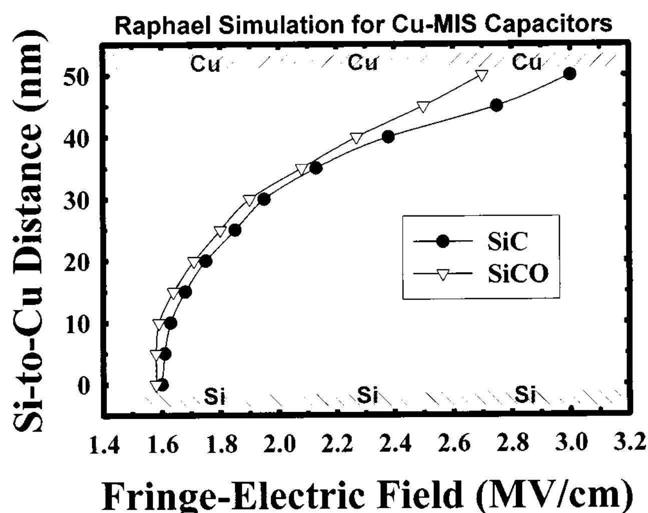

Figure 6. Fringe-electric field obtained from Raphael simulation for the Cu-gated MIS capacitors of α-SiC as well as α-SiCO dielectric biased with an electric voltage of 10 V (equivalent to an electric field of 2 MV/cm).

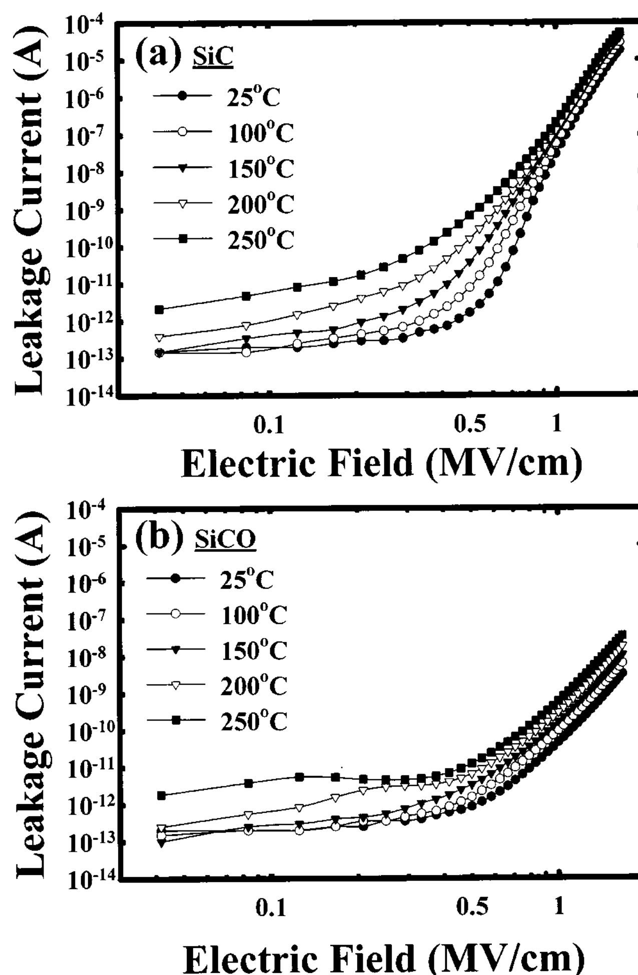

Figure 7. Leakage current *vs.* electric field in a log-log plot, measured at various temperatures, for Cu-comb capacitors with (a) α-SiC and (b) α-SiCO cap barriers.

cap barrier and the OSG layer are similar materials of Si-C-O compounds, while the SiC cap barrier is an oxygen-absent Si-C compound. Similar presumption was reported for the CMP surface at the α-SiCN (cap barrier)/α-SiCN (hard mask) interface of the same material in the Cu damascene interconnect.[23] Two different electric-field-dependent conduction mechanisms were also observed in the Cu-comb capacitors. First, all Cu-comb capacitors exhibit ohmic conduction at low electric fields (<0.3 and <0.4 MV/cm for SiC and SiCO cap barriers, respectively) because the leakage current (I) is linearly correlated with the electric field ($\mathbf{E}$).[18,19] Nevertheless, at high electric fields (>0.3 and >0.4 MV/cm for SiC and SiCO cap barriers, respectively), the Cu-comb capacitors with SiC and SiCO cap barriers exhibit quite different nonlinear I-$\mathbf{E}$ relation, particularly at temperatures above 200°C. This implies that the SiC and SiCO samples have different conduction mechanisms at high electric fields. From the best fitting of the known conduction mechanisms in dielectrics,[18,19] we found that the SiC sample exhibits F-P emission, while the SiCO sample reveals SE conduction, as shown in Fig. 8. The Cu-comb capacitors and the Cu-MIS capacitors exhibit the same electric-field-dependent conduction mechanisms. This further confirms that the dominant leakage paths are not only along the cap barrier/OSG interface (CMP surface) but also in the bulk cap barrier. Furthermore, in our previous work the more leaked CMP surface of Cu-comb capacitor also enhanced the leakage current and F-P emission.[8] Thus, the semiconductor nature of the conductive bulk SiC and the more leaked CMP surface at the SiC/OSG interface resulted in the increased leakage current and F-P emission for the

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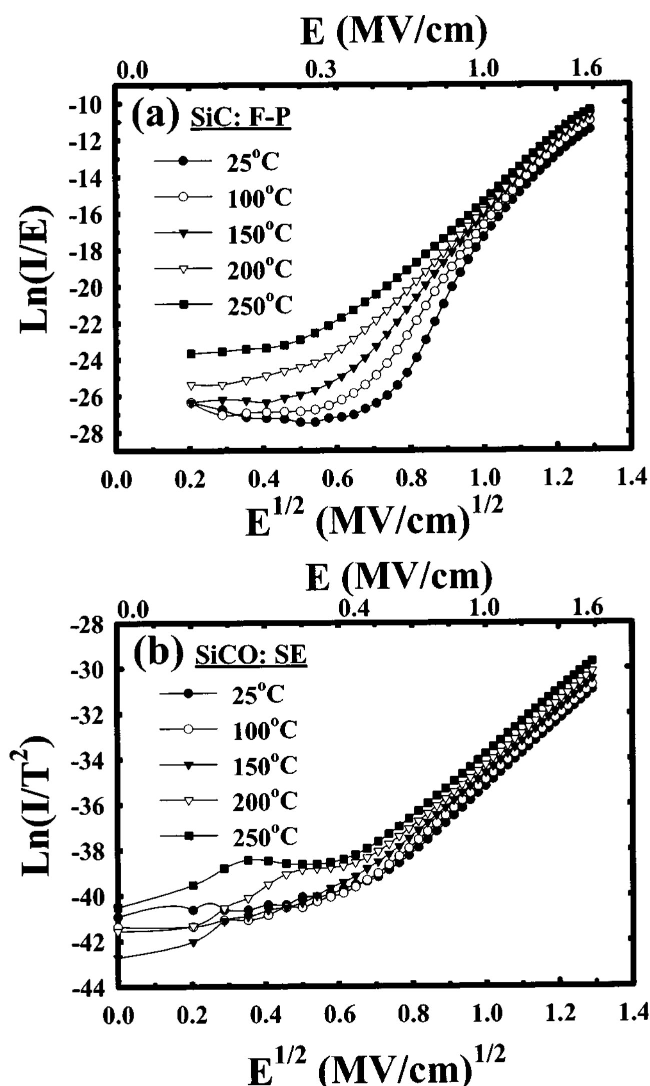

Figure 8. Conduction mechanism of (a) Frenkel-Poole emission in Cu-comb capacitor with α-SiC cap barrier and (b) Schottky emission in Cu-comb capacitor with α-SiCO cap barrier.

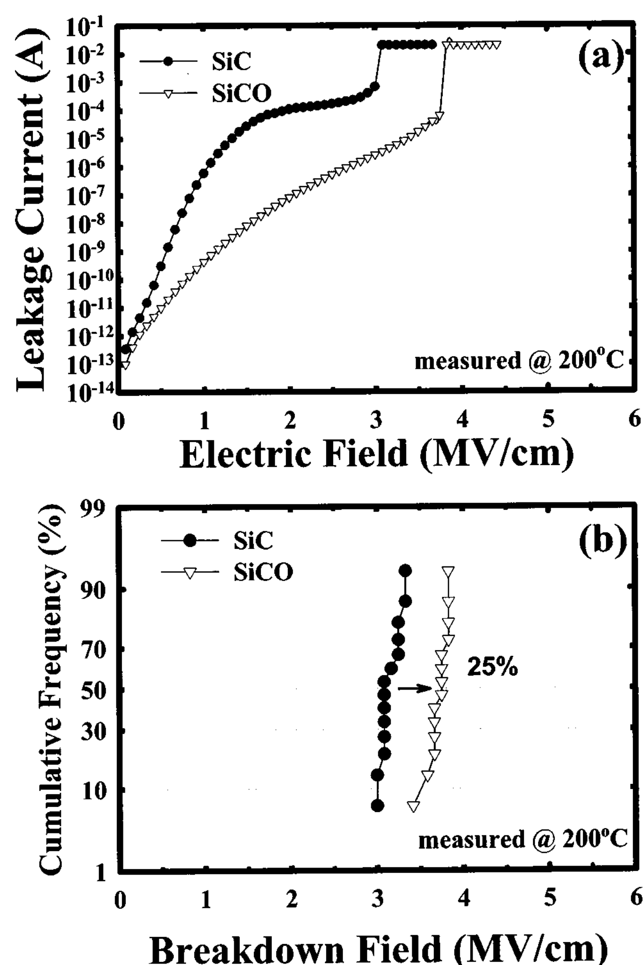

Figure 9. (a) Leakage current *vs.* electric field and (b) distribution of breakdown field for the α-SiC and α-SiCO Cu-comb capacitors measured at 200°C.

Cu-comb capacitor with a SiC cap barrier. Figure 9 shows the leakage current and breakdown field for the Cu-comb capacitors with SiC and SiCO dielectric cap barriers measured at 200°C. Notably, the breakdown field of the SiCO sample is about 25% higher than that of the SiC sample. This increase in breakdown field is presumably due to the better electrical property of bulk SiCO and the diminution of CMP-surface leak-path. In addition, the lower **k** value of the SiCO film also reduces the surface-electric field at the cap barrier/OSG interface (CMP surface), as illustrated in Fig. 10.[24,25] The lower surface-electric field at the CMP surface results in a lower leakage current and higher breakdown field for the SiCO sample. Figure 11 shows the surface-electric field obtained from Raphael simulation for the Cu-comb capacitors biased with an electric voltage of 24 V, which produces an electric field of 2 MV/cm in the dielectric layer of the Cu-comb capacitor. Notably, the surface-electric field near the Cu line of the SiCO sample is about 6% lower than that of the SiC sample.

Conclusion

The leakage current and breakdown field of the Cu-MIS and Cu-comb capacitors are dependent on the dielectrics (α-SiC and α-SiCO) used as insulator and dielectric cap barrier, respectively. The Cu-MIS and Cu-comb capacitors with an α-SiCO ($k = 3.7$) dielectric barrier exhibit a leakage current at least three orders of

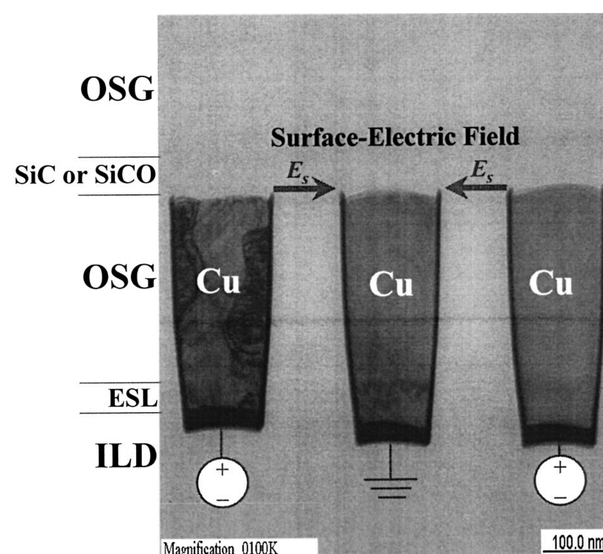

Figure 10. Proposed surface-electric field in the Cu-comb capacitor.

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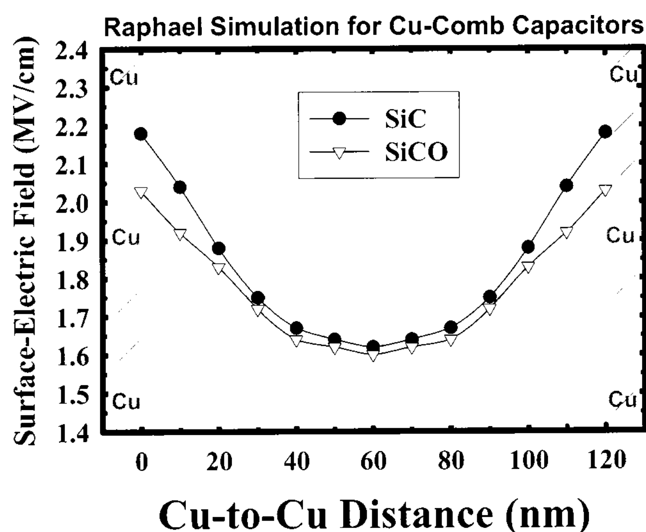

Figure 11. Surface-electric field obtained from Raphael simulation for the Cu-comb capacitors with α-SiC and α-SiCO cap barrier biased with an electric voltage of 24 V (equivalent to an electric field of 2 MV/cm).

magnitude smaller than those with an α-SiC ($k = 4.4$) dielectric barrier at an applied electric field of 1.6 MV/cm between 25 and 250°C. Moreover, the breakdown field of the Cu-MIS and Cu-comb capacitors with an α-SiCO dielectric barrier, measured at 200°C, are 60 and 25%, respectively, higher than that of the capacitors with an α-SiC barrier. The decreased leakage current and increased breakdown field of the Cu-MIS and Cu-comb capacitors with an α-SiCO dielectric barrier are attributed to the higher density, oxygen-improved film property, non-semiconductor behavior, and lower fringe- or surface-electric field of the α-SiCO dielectric film.

Acknowledgment

The authors express their gratitude to Dr. Chih-Feng Huang of National Chiao-Tung University for his valuable help of Raphael simulation.

National Chiao-Tung University assisted in meeting the publication costs of this article.

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