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An Alternative Process for Silicon Nanowire Fabrication with SPL and Wet Etching System

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Silicon nanowire fabrication of nanoscale dimensions on a single-crystal silicon surface by scanning probe lithography (SPL) and potassium hydroxide (KOH) aqueous wet etching system has proven to be adequate technological processes. Using SPL directly to define patterns on a single-crystal silicon surface showed that the linewidth of ~50 nm can be further shrunk to ~20 nm with KOH wet etching and orientation-dependent etching (ODE) processes on (110)-oriented silicon samples. In addition, this lithography technique also showed a great ability to define patterns on fluorocarbon mask layers. This method performed the fine linewidth of silicon nanowires around 20 nm by operating with lower applied voltages and higher scanning speeds (shorter exposure time) with SPL and ODE techniques and KOH wet etching on (100)-oriented silicon samples. These alternative processes provide the capability to fabricate nanoscale structures with high reliability and repeatablility for applications in the nanofields.
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In the past few years, nanotechnology and nanofabrication have been vigorously investigated because of their potential applications in nanoelectronics, nanoelectromechanical systems, nanobiology, and other fields. The silicon nanowire is a proven material for fabricating electron devices which show the quantization results of single-electron transportation and fabricating biosensor devices with extremely high sensitivity.[1,2] The fabrication process of silicon nanowires can be divided into two categories, the top-down process and the bottom-up process.[3] The most acceptable methods for defining the silicon nanowire patterns with the top-down process include electron beam lithography (EBL) and scanning probe lithography (SPL). SPL has the advantages of low equipment cost as well as good performance with nanostructure fabrication and the ability to observe immediate results. SPL uses a probe, which scans the sample surface using excess voltage between the probe and the sample. This excess applied voltage builds an electric field that forces the radical ions (OH^-, O^{-2}) to penetrate into the sample surface about 2-3 nm in depth and results in a protruded oxide layer of about 2-4 nm as shown by the pioneering work of Dagata *et al.*[4] By using this method, the desired oxide patterns can be defined directly onto the silicon sample surface. This protruding oxide layer can be used as a mask layer for the underlying silicon etching by using potassium hydroxide (KOH) solution and yielding the linewidth of silicon nanowires to about 20 nm shown in our prior study.[5] Chien *et al.*[6] and Clement *et al.*[7] fabricated several nanostructures and nanocircuits by combining SPL and wet etching, demonstrating the excellent ability of SPL to directly pattern in nanofabrication. However, the area of definition patterning by using SPL field induced oxidation directly is small and depends upon the material of the scanning tips. This limits the application of SPL in large areas of industrial applications. Finding a suitable resistant layer for SPL to define large-area patterns becomes critical for increasing the area of applications. With the different SPL operation modes, the built-up electric field forces the electrons to emit from the probe to the sample to obtain the narrow patterns on the electron resistant layer. Wilder *et al.* showed that by using noncontact mode atomic force microscope (NC-AFM) lithography and reactive ion etching (RIE) system resulted in the high-resolution silicon nanowires of feature sizes around 30 nm.[8] Also Avramescu *et al.*[9] showed that the deposition of a carbonaceous film as a mask layer on the semiconductor surface with electron-beam irradiation resulted in a minimum linewidth of 22 nm on this layer after AFM lithography. Direct patterning on the substrate material and on the mask layer provides a convenient way for SPL to define the desired patterns which are very similar to the positive and negative photoresist processes in optical lithography.

In SPL, excess applied voltage and scanning speed between the probe and sample are the main factors for controlling the feature size of silicon nanowire fabrication. For example, the applied voltage was higher than 84 V for patterning the narrow wire on the electron resistant layer at scanning speed 10 μm/s, while the scanning speed was 0.1 μm/s for patterning the narrow wire on thin silicon nitride (4.5 nm) layer at applied voltage of 4-10 V.[8,10] It is found that the protruded oxide thickness and linewidth increase with increasing the applied voltage and decrease with increasing scanning speed. Therefore, finding a suitable mask layer, which can be operated at lower applied voltage and higher scanning speed, for SPL patterning is very important for silicon nanowire fabrication.

In this study, we demonstrated the fabrication of silicon nanowires in the following two alternative processes. (*i*) The protruded oxide linewidth is controllable by applying voltage and scanning speed for direct patterning on the single-crystal silicon sample surface. (*ii*) The plasma-induced fluorocarbon layer on the silicon surface is used as a mask layer for SPL patterning when operating at lower voltages and higher scanning speeds.[11] We also show that the KOH wet etching process can provide highly reliable silicon etching and can further shrink the silicon nanowire linewidth by orientation dependence etching (ODE).[12]

Experimental

In this study, two different processes of experiments were investigated. The relevant steps of SPL on single-crystal and fluorocarbon layer are schematically summarized in Fig. 1a and b, respectively. In Fig. 1a, the silicon samples were cut from n-type (110)-oriented silicon wafers with resistivity around 1-10 Ω cm. The silicon wafers were cleaned by the standard RCA process. Before SPL patterning, the silicon samples were dipped in dilute HF solution to remove the native surface oxide for 30 s and a hydrogen passivation was formed on the silicon surface. The surface roughness of the H^+ passivation silicon surface was around 0.241 nm measured by an atomic force microscope (AFM). Field-induced local oxidation was performed by the AFM in ambient air (controlled humidity = 40 ± 2%) with a

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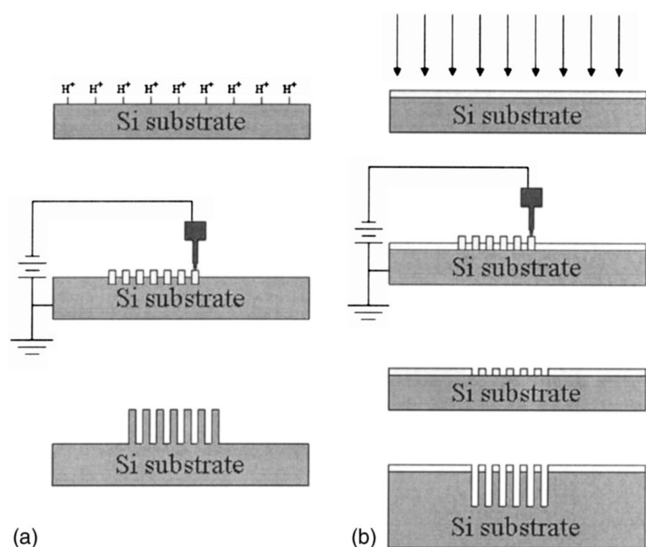

Figure 1. (a) Process flow chart of SPL for direct patterning on the (110)-oriented silicon sample followed by the wet etching process in 34 wt % KOH solution. (b) The process flow of SPL on the fluorocarbon layer and KOH wet etching process after dipping the sample in dilute HF solution to remove the induced oxide.

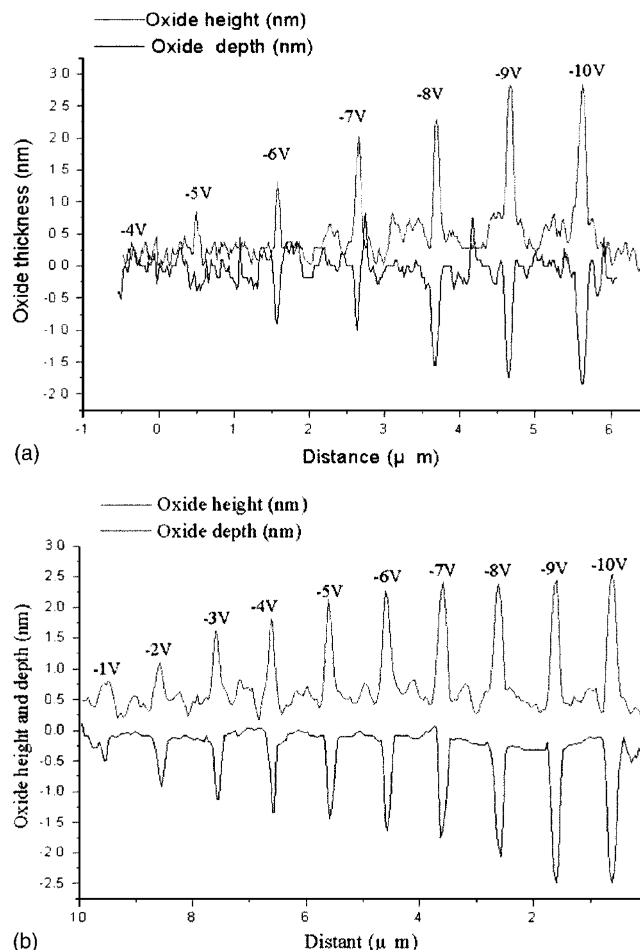

Figure 2. (a) Single-crystal silicon sample showing the oxide height and depth, induced by SPL local oxidation. The linear region appears at −5 to −8 V and the scanning speed dominant region appears at −9 to −10 V. (b) The fluorocarbon layer showing the oxide height and depth. The linear region appears at −1 to −6 V, and the scanning speed dominant region appears at −7 to −10 V.

highly doping silicon cantilever tip (resistivity 0.01-0.0025 Ω cm and diameter, ~10 nm, Nanosensors). After AFM local oxidation, the samples were dipped in a 34 wt % KOH solution at temperature of 50°C with acoustic agitation. The other experiments are shown in Fig. 1b. The silicon samples were cut from p-type (100)-oriented silicon wafers with resistivity 0.01-0.001 Ω cm. The fluorocarbon layer was formed by an inductively coupled plasma (ICP) dry etching system with 40 sccm CF_4 gas source, an rf power of 400 W, and dc power of 100 W at 60°C for 20 s. The local oxidation was performed by AFM under the same conditions as the process shown in Fig. 1a. After local oxidation, the samples were dipped in dilute HF for 30 s to remove the field-induced oxide and sequentially dipped in 34 wt % KOH solution at temperature 40°C.

Results and Discussion

We had two groups of experiments, (*i*) SPL directly patterned on (110)-oriented single-crystal silicon sample and (*ii*) SPL patterned on the plasma-induced fluorocarbon layer, which was constructed from (100)-oriented single-crystal silicon sample by ICP. Each sample was etched by the KOH solution along with the orientation dependent etching (ODE) technique and finally obtained the silicon nanowire of about ~20 nm.

The effects of scanning speed and probe/sample voltage are equivalent to exposure time and intensity of optical lithography, respectively. The results of probe/sample voltage on SPL process are shown in Fig. 2a. The variation of voltage was from −4 to −10 V, and the scanning speed was maintained at 1 μm/s. The AFM was operated in contact mode, and the contact force was set at a constant value (10 nN). The thickness (h) of the protruded oxide was from 2.8 nm (−10 V) to 0.6 nm (−5 V) and could not be identified at −4 V. The thickness of the protruded oxide was linearly proportional to the applied voltage from −5 to −9 V due to the built up electric field which was also linearly proportional to the probe/sample voltage. The effect of scanning speed was observed at voltages −10 and −9 V. The protruded oxides were 2.8 nm for −10 V and 2.7 nm for −9 V, respectively. We found that the protruded oxide was dominated by the scanning speed at scanning speed 1 μm/s for the applied voltage equal to −10 V. In this case, the negative radical ions, such as OH^-, O^{-2}, did not completely penetrate the silicon surface at this scanning speed (exposure time). The depth (d) of the penetrated oxide also demonstrated a similar result as the protruded oxide. The conversion ratios $(h + d)/d$ of the applied voltage (−5 to −10 V) were 3.95, 2.84, 3.87, 2.77, 3.03, and 2.94, respectively, and the conversion ratio was equal to 2.27 for thermal oxide. The higher conversion ratio indicates that the induced oxide layer is weak for masking the silicon during the sequence KOH etching process.[13] This characteristic implies the oxide quality is an important factor for the underlying wet etching process.

For the case of SPL with fluorocarbon mask layer, the effect of probe/sample voltage on oxidation is shown in Fig. 2b. The contact force, scanning speed, and humidity of the ambient were 10 nN, 1 μm/s, and 40 ± 2%, respectively. The results were similar to Fig. 2a, which included a linear region and a saturation region in which the scanning speed is dominant. The linear region occurs from −1 to −7 V, and the scanning speed dominant region occurs at −7 to −10 V. The scanning speed dominant region appeared at the lower applied voltage *ca.* −7 V instead of −9 V as in prior experimental results. The reason is that the plasma induced the defects on the

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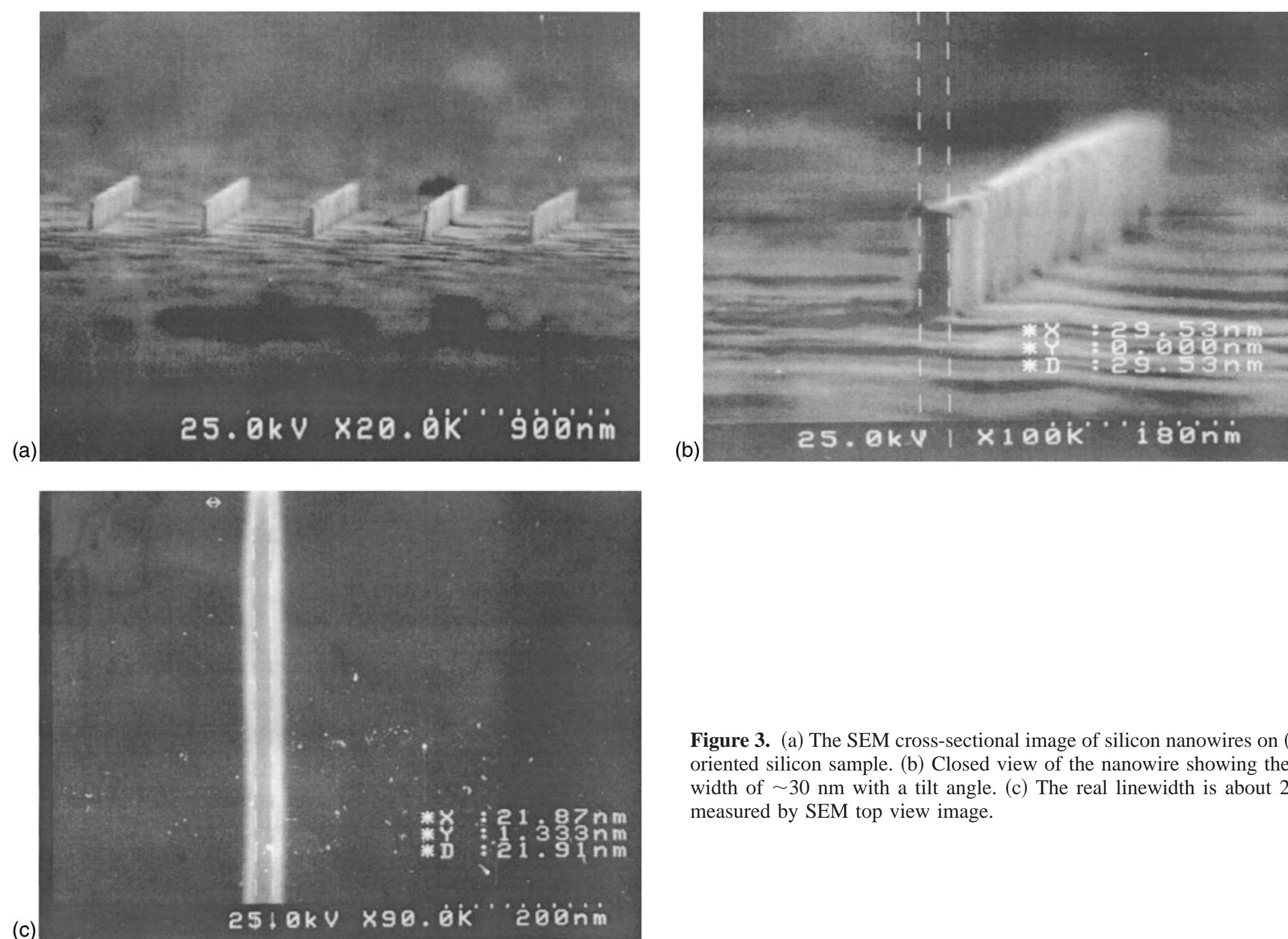

Figure 3. (a) The SEM cross-sectional image of silicon nanowires on (110)-oriented silicon sample. (b) Closed view of the nanowire showing the linewidth of ~30 nm with a tilt angle. (c) The real linewidth is about 20 nm measured by SEM top view image.

surface layer of the (100)-oriented silicon sample. These defects reduced the energy barrier of penetration and enhanced the radical ions to penetrate the deeper location in the same scanning speed (exposure time) such that the depth of induced oxide was deeper than the one in Fig. 2a, respectively. The thickness of the fluorocarbon layer was ~25 Å, measured by a scanning auger microscope (SAM), and the major elements were Si, C, O, and F. The conversion ratios of the fluorocarbon layer were reduced to values between 1.82-2.48. The possible reason is that the defects also increased the induced oxide depth d. These defects provided more space for radical ions to convert into the oxide and resulted in the smaller height of the protruded part h at the same humidity and condition of the quantity of radical ions.

After SPL local oxidation, the underlying desired patterns were performed by the aqueous KOH wet etching system. In Fig. 3, the linewidth of oxide patterns was ~50 nm before etching and was further shrunk to ~20 nm by ODE. ODE is a method whereby using different orientation planes have different etching rates, depending upon the number of chemical bonds, to etch the desired patterns. The etching rate ratio of (110):(100):(111) was 400:200:1 in this study at an etching temperature of 50°C. The 50 nm oxide patterns were generated by −8 V of applied voltage and 1 μm/s of scanning speed. At this condition, the total thickness of the induced oxide was ~3 nm which was thick enough to protect the underlying silicon during KOH wet etching at a temperature of 50°C.

Figure 4a shows the top-view AFM image of the nanowire structure, fabricated by using a fluorocarbon mask layer. The surface roughness (Rq) of the fluorocarbon layer was 0.734 nm before etching and 0.844 nm after 34 wt % KOH etching for 90 s at an etching temperature 40°C. Figure 4b shows the 3D image of Fig. 4a. The surface roughness remains very well intact after etching and the fluorocarbon layer showed a perfect ability to protect the underlying silicon. The line width was ~90 nm and the depth was ~100 nm. The orientation of the sidewall plane is (100)-oriented, which has the same etching rate as the top plane and the (100)-oriented plane has a middle etching rate [faster than (111)-oriented, slower than (110)-oriented] to which the nanowire can be further shrunk by controlling the etching time. Figure 4d shows the shrunk nanowires with ~20 nm of linewidth and 300 nm of depth. The two left nanowires in the figure show the overetching results at the end of line edge.

Conclusions

We have demonstrated the process of scanning probe lithography (SPL) to define the nanopatterns on the silicon surface and on the fluorocarbon layer. In combination with the KOH wet etching process, the silicon nanowire with ~20 nm of linewidth was easily obtained and the surface roughness could be improved by using the fluorocarbon mask layer. SPL and KOH wet etching provide high reliability and uniformity to fabricate nanostructures, which have been widely implemented in nanoelectron devices, biosensors, and nanoelectromechanical systems.

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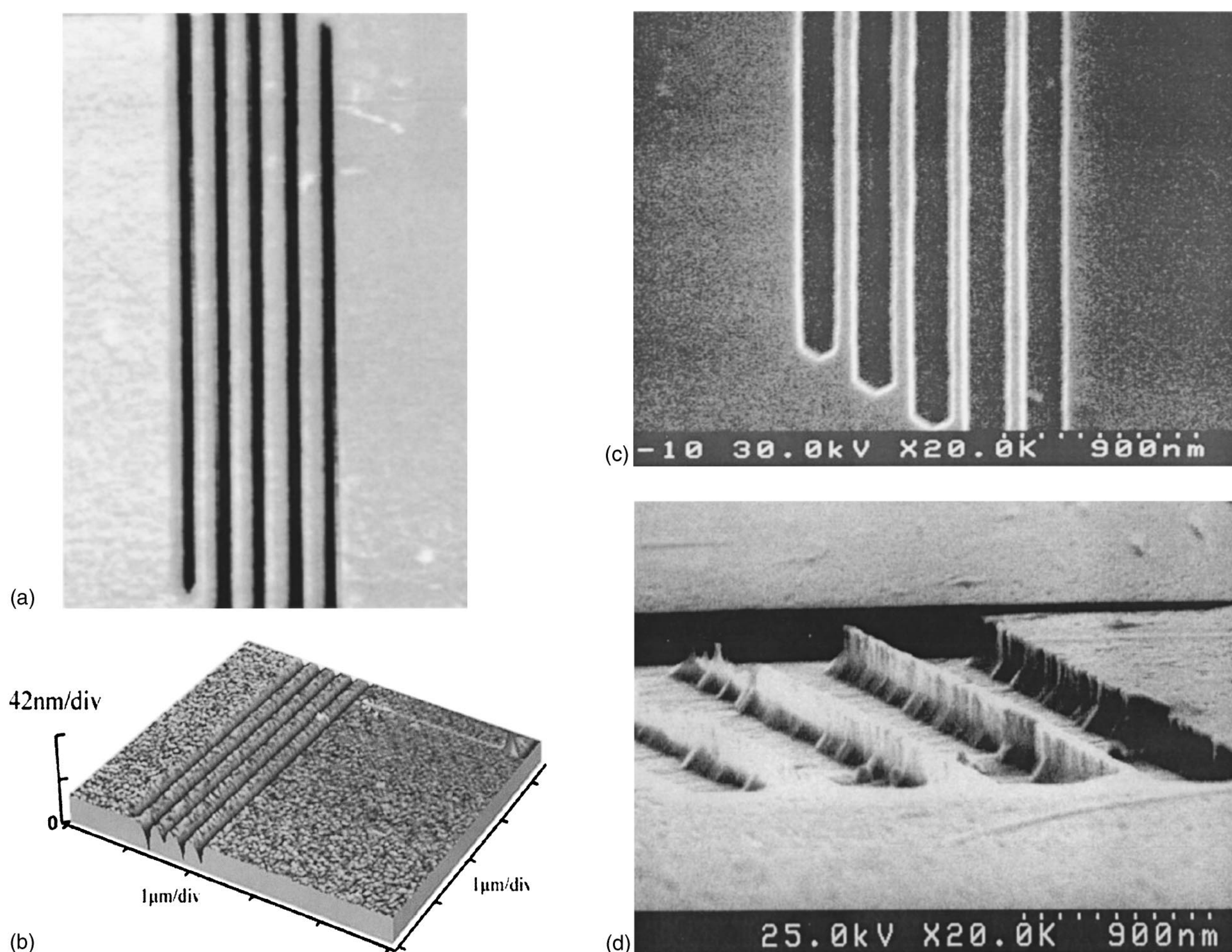

Figure 4. (a) The top view image measured by AFM. (b) The AFM 3D image nanotrench width is ~150 nm and the nanowire linewidth is ~90 nm after KOH etching for 120 s at etching temperature 40°C. (c) The silicon nanowire is ~90 nm and the trench width is ~180 nm measured by SEM. The silicon nanowire with linewidth ~20 nm was obtained with the sidewall shrinking process. (d) The overetching condition shows in the left two nanowires.

References

1. Y. Cui and C. M. Lieber, *Science,* **291**, 851 (2002).
2. Y. Cui, Q. Wei, H. Park, and C. M. Lieber, *Science,* **293**, 1289 (2001).
3. M. K. Sunkara, S. Sharma, R. Miranda, G. Lian, and E. C. Dickey, *Appl. Phys. Lett.,* **79**, 1546 (2001).
4. J. A. Dagata and W. Tseng, *Appl. Phys. Lett.,* **62**, 591 (1993).
5. J. T. Sheu, K. S. You, C. H. Wen, and K. M. Chang, in *Proceeding of IEEE-NANO-2001*, 213 (2001).
6. F. S.-S. Chien, W.-F. Hsieh, S. Gwo, A. E. Vladar, and J. A. Dagata, *J. Appl. Phys.,* **91**, 10044 (2002).
7. N. Clement, A. Francinelli, D. Tonneau, Ph. Scotto, F. Jandard, H. Dallaporta, V. Safarov, D. Fraboulet, and J. Gautier, *Appl. Phys. Lett.,* **82**, 1727 (2003).
8. K. Wilder, C. F. Quate, D. Adderton, R. Bemstein, and V. Elings, *Appl. Phys. Lett.,* **73**, 2527 (1998).
9. A. Avramescu, A. Ueta, K. Uesugi, and I. Suemune, *Appl. Phys. Lett.,* **72**, 716 (1998).
10. F. S.-S. Chien, J. W. Chang, S. W. Lin, Y. C. Chuo, T. T. Chen, S. Gwo, T. S. Chao, and W. F. Hsieh, *Appl. Phys. Lett.,* **76**, 360 (2000).
11. G. S. Oehrlein and Y. H. Lee, *J. Vac. Sci. Technol. A,* **5**, 1585 (1987).
12. K. Sato, M. Shikida, Y. Matsushima, T. Yamashiro, K. Asaumi, Y. Iriye, and M. Yamamoto, *Sens. Actuators, A,* **64**, 87 (1998).
13. K. Morimoto, F. Perez-Murano, and J. A. Dagata, *Appl. Surf. Sci.,* **158**, 205 (2000).

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