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Novel Low-Temperature Polycrystalline-Silicon Power Devices with Very-Low On-Resistance Using Excimer Laser-Crystallization

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Low-temperature poly-Si lateral double-diffused metal oxide semiconductor (LTPS LDMOS) with high voltage and very low on-resistance has been achieved using excimer laser crystallization at 400°C substrate heating for the first time. The ON/OFF current ratios were 2.96×10^5 and 6.72×10^6 while operating at $V_{ds} = 0.1$ and 10 V, respectively. The maximum current limit was up to 10 mA and maximum power limit could be enhanced over 1 W at $V_{ds} = 90$ V and $V_{gs} = 20$ V. The $R_{on,sp}$ with dimensions of $W/L_{ch} = 600$ μm/12 μm could be significantly decreased 6.67×10^2 times in magnitude as compared with conventional offset drain thin-film-transistors.
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Low-temperature poly-Si high-voltage thin-film-transistors (LTPS HVTFTs) have been widely studied to realize glass compatible driver circuits for light valves, high speed printers, liquid crystal displays, plasma displays, etc.[1-3] However, many issues still remain, such as on-state degradation, gate dielectric reliability, circuit/operation complexity, and surface contamination, resulting in unsuitable implementation of integration electronic systems for future system-on-a-panel (SOP) applications.[3]

In this article, a LTPS lateral double diffused metal oxide semiconductor (LDMOS) using excimer laser crystallization has been demonstrated by combination of the thin-film transistor (excimer laser crystallization) and power device technologies (LDMOS architecture) for the first time. Excimer laser crystallization (ELC) is a promising technology in obtaining high current capability due to large grains, fewer defects, and compatible glass substrate against the solid-phase crystallization (SPC) of HVTFTs.[4] LDMOS architecture is a promising design to obtain high blocking capability due to the reduced-surface-field (RESURF) against the only offset drain (drift) region of HVTFTs.[5] Hence, the LTPS LDMOS at room-temperature irradiation can exhibit better characteristics than conventional HVTFTs. Moreover, LTPS LDMOS at 400°C irradiation can perform somewhat like single crystalline silicon (c-Si) LDMOS.

Experimental

The fundamental structure of LTPS LDMOS under room-temperature or 400°C irradiation is shown with the labels of RESURF design from "A" to "E" in Fig. 1. The conventional offset drain (OD) TFT structure is also exhibited for comparison. First, a 1.5 μm thick wet oxide was grown on a silicon wafer. Then, amorphous-silicon (a-Si), 0.1 μm thick, was deposited on the wafer by low-pressure chemical vapor deposition (LPCVD) at 550°C. Next, as shown in label "A", the 50 keV phosphorus dose of 7×10^{11} cm^{-2} was implanted into the above a-Si drift region to reduce the current path resistance. However, conventional OD TFT lacked this drift implantation so as to possess the large on-resistance with its intrinsic region. At label "B", the high energy of 60 keV boron dose of 3×10^{13} cm^{-2} was created as the buried p-well region to increase the depletion width in the n-drift region without adding threshold voltage. Laser crystallization was performed using KrF excimer laser ($\lambda = 248$ nm) with energy densities from 400 to 470 mJ/cm^2 and 99% overlapped shot density at room temperature or 400°C substrate heating. However, conventional OD TFT was crystallized by a furnace at 600°C to produce small grain sizes in its intrinsic region. After that, a 5000 Å thick field oxide (FOX) at label "C" was formed by plasma-enhanced chemical vapor deposition (PECVD) at 350°C to RESURF. A 1000 Å thick PECVD gate oxide and a 2000 Å thick LPCVD a-Si gate were defined across the FOX to split the p-well/n-drift junction electric field at label "D". 50 keV phosphorus and boron doses of 5×10^{15} cm^{-2} were carried out to form an n$^+$ drain. source, gate, and p$^+$ butting regions. Finally, a 6000 Å thick Al extended drain was defined to overlap the 5000 Å thick passive layer and pass through the n-drift/n$^+$ drain junction to split its electric field at label "E". All steps were compatible for standard TFT fabrication and glass process with a maximum temperature of 600°C.

Results and Discussion

Table I lists the transfer characteristics of the conventional OD TFT and the proposed LTPS LDMOS with optimal room-temperature irradiation. The LTPS LDMOS was obtained from the following parameters: $W = 600$ μm, $L_{ch} = 12$ μm, $L_{drift} = 15$ μm, $N_{drift} = 7 \times 10^{11}$ cm^{-2}, $t_{si} = 0.1$ μm, and $t_{oxide} = 1.5$ μm. The OD TFT was established from the parameters: $W/L_{ch} = 100$ μm/16 μm, $L_{drift} = 20$ μm, $t_{si} = 0.3$ μm, and $t_{oxide} = 2$ μm.[6] The comparison of LTPS LDMOS without and with ELC was reported by Chang *et al.*[7] As shown in Table I, the OD TFT exhibited a low threshold voltage (V_{th}) of 0.5 V due to the intrinsic well region which makes the device more sensitive to signal noises. The LTPS LDMOS presented a higher threshold voltage of 4 V at room-temperature irradiation due to the dose of 3×10^{13} cm^{-2} p-well region which operated stably. With respect to the subthreshold swing (SS), the LTPS LDMOS at room-temperature irradiation had a smaller value of 1.18 V than the OD TFT value of 1.92 V. The on-state current (I_{ON}) and off-state current (I_{OFF}) of ON/OFF current ratio were defined at the gate biases of 35 and −10 V, respectively. The LTPS LDMOS at room-temperature irradiation displayed better I_{ON}/I_{OFF} current ratios of 2.19×10^4 and 1.23×10^6 than OD TFT ones of 3×10^3 and 5×10^3 at the drain biases of 0.1 and 10 V. The breakdown voltage (BV) of LTPS LDMOS at room temperature irradiation was also higher at 240 V than conventional OD TFT with a breakdown voltage of 155 V. Thus, in terms of the on-state (V_{th}, SS, I_{ON}/I_{OFF}) and off-state (BV) characteristics, the proposed LTPS LDMOS at room-temperature irradiation was better than the conventional OD TFT.

Figure 2 shows the transfer characteristics of LTPS LDMOS for optimal room temperature and 400°C irradiation. The anomalous

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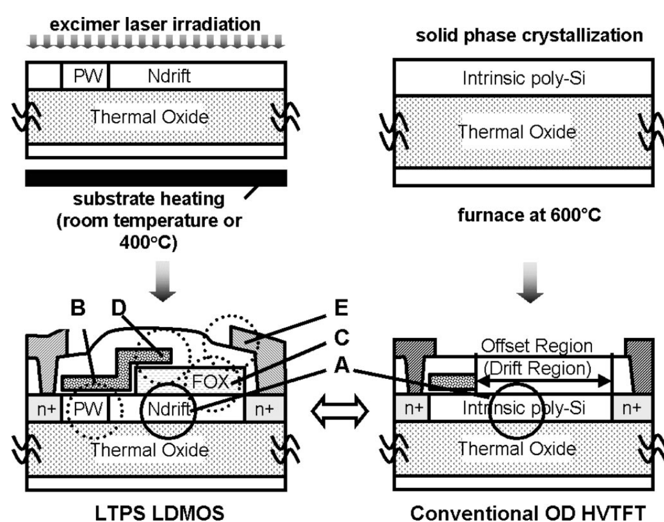

Figure 1. LTPS LDMOS structure fabricated by excimer laser crystallization under room temperature or 400°C irradiation. The broken circles represented the RESURF design and the solid circles indicated the drift with/without doping for reducing the resistance of drift region in LTPS LDMOS and OD TFT devices.

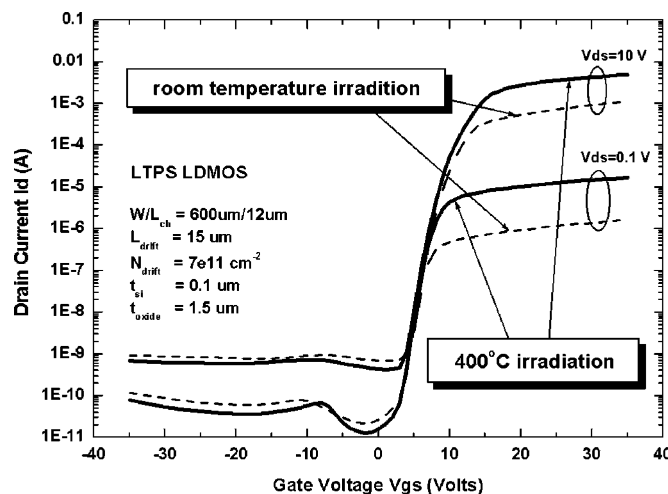

Figure 2. Transfer characteristics of LTPS LDMOS for optimal room-temperature and 400°C irradiation.

I_{OFF} leakage current may be restrained by the drift region (offset region) at negative gate voltages regardless of the drain voltage increase even up to $V_{ds} = 10$ V.[8] The I_{OFF} at 400°C substrate heating was lightly lower than that at room temperature due to the small reduction in the defect trap states.[9] The threshold voltage was not changed at 4 V for 400°C and room temperature due to similar p-well concentrations. The subthreshold swing was reduced from 1.15 V at 400°C irradiation to 1.18 V at room temperature irradiation. It revealed finite improvement of 2.5% by 400°C irradiation. The I_{ON}/I_{OFF} current ratios through 400°C irradiation were further increased from 2.19×10^4 to 2.96×10^5 at $V_{ds} = 0.1$ V and 1.23×10^6 to 6.72×10^6 at $V_{ds} = 10$ V, which were indicated about 14 and 5 times improvement one room-temperature ratios, respectively.

Figure 3a and b shows the output characteristics of LTPS LDMOS for optimal room temperature and 400°C irradiation. While the substrate was heated to 400°C, the maximum current limit was increased about two times from 5 to 10 mA at $V_{gs} = 20$ V. The maximum power limit, where the LTPS LDMOS was burned out, was great in 1.11 W (6852 W/cm^2) at $I_{ds} = 12.3$ mA, $V_{ds} = 90$ V, and $V_{gs} = 20$ V. The latch-up current at $V_{gs} = 16$ V could be suppressed up to 90 V drain voltage with two times drain current from 1.5 to 3 mA. Nevertheless, the latch-up voltage (kink voltage) at $V_{gs} = 16$ V was slightly decreased about 0.95 times from 95 to 90 V. The maximum voltage limit (breakdown voltage) was reduced about 0.75 times from 240 to 180 V in Fig. 3b. The reason may be that the impact ionization path and effective ionization rate (α) were raised by the fewer intra/inter gain defects so that the breakdown voltage dropped below that of room-temperature irradiation.[10] But, on the whole, the safe operating area (SOA) could be still improved about twice (1.5 times) with two times enhancement of the maximum current and 0.75 times degradation of maximum voltage by the 400°C irradiation relative to that at room-temperature (RT) irradiation.

Table I. Summary of the transfer characteristics for conventional OD TFT and the proposed LTPS LDMOS with optimal room-temperature irradiation.

	Conventional OD TFT	Room-temperature LTPS LDMOS
Threshold voltage (V)	0.5	4
Subthreshold swing (V/dec)	1.92	1.18
Max. I_{ON}/I_{OFF} at $V_{ds} = 0.1$ V	3×10^3	2.19×10^4
Max. I_{ON}/I_{OFF} at $V_{ds} = 10$ V	5×10^3	1.23×10^6
Breakdown voltage (V)	155	240

Figure 4a shows the relationships between the specific on-resistance and laser energy density for LTPS LDMOS at RT/400°C irradiation together with OD TFT, variable doping slot (VDS) TFT, and c-Si LDMOS. The variable doping slots (VDS) TFT had a continuous shallow doping profile to reduce the on-state resistance and split the potential drop across the offset region.[6] The specific on-resistances ($R_{on,sp}$) of all structures was defined at $V_{gs} = 20$ V and $V_{ds} = 20$ V. The grain growth regimes were divided into three parts: partial melting, super lateral growth (SLG) (the expected regime for the largest grain size), and ablation of Si film regimes. As a result, the LTPS LDMOS at room-temperature irradiation exhibited better $R_{on,sp}$ of 1.78 Ω-cm^2 by the ELC process and RESURF design than the conventional OD TFT of 360 Ω-cm^2 and V_{DS} TFT of 10 Ω-cm^2 by offset region and SPC process.[6] Nevertheless, the $R_{on,sp}$ of room-temperature irradiation still fell about 18 times behind the 0.10 Ω cm^2 of c-Si LDMOS from Taurus and Athena/Atlas simulators.[11,12] Fortunately, while crystallizing at 400°C, the $R_{on,sp}$ of room-temperature irradiation may be further reduced about three times from 1.78 to 0.54 Ω-cm^2 at the optimal laser conditions of 470 and 435 mJ/cm^2, respectively. The $R_{on,sp}$ of LTPS LDMOS may be greatly decreased from 18 times only five times higher than that of c-Si LDMOS. It was concluded that the solidification velocity at 400°C irradiation could be reduced to about one-fifth and the crystallinity could improve as compared to that at room temperature irradiation.[13,14]

Figure 4b compares the breakdown voltages for the LTPS LDMOS at RT/400°C irradiation together with OD TFT, VDS TFT, and c-Si LDMOS. The Si atoms in the crystalline solids were orderly arranged unlike the segment order of polyerystalline solids. Consequently, the impact ionization path and effective ionization rate (α) of c-Si LDMOS is the longest and largest, which resulted in minimum breakdown voltage of 145 V for comparison with poly-

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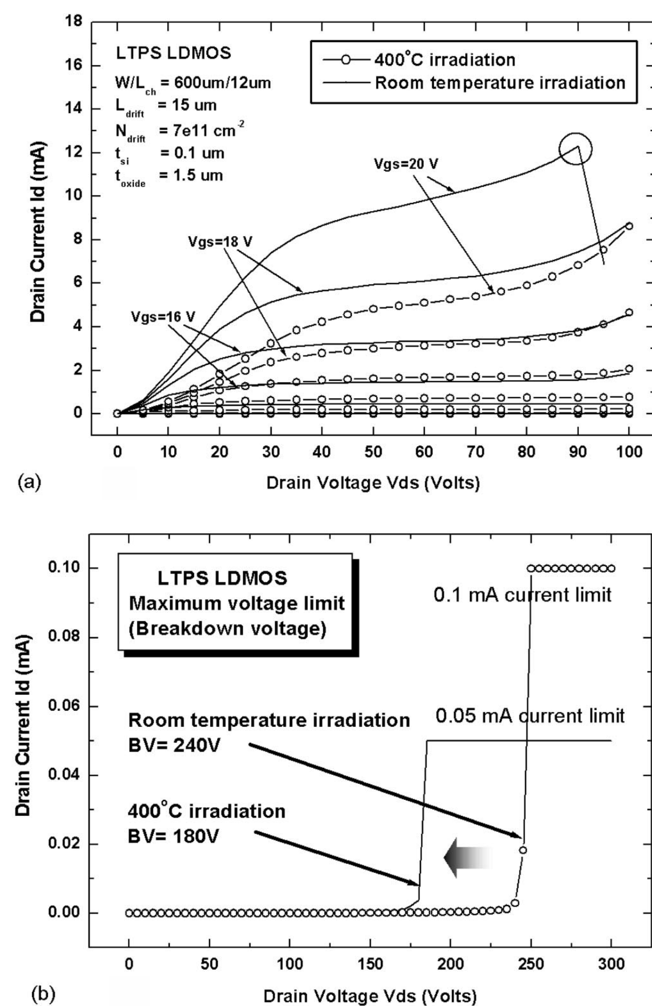

Figure 3. Output characteristics of LTPS LDMOS for optimal room-temperature and 400°C irradiation. (a) The circle indicates the maximum power limit point of 1.11 W. (b) Breakdown voltages were measured by the protective current limits of 0.1 and 0.05 mA for room-temperature and 400°C irradiation, respectively.

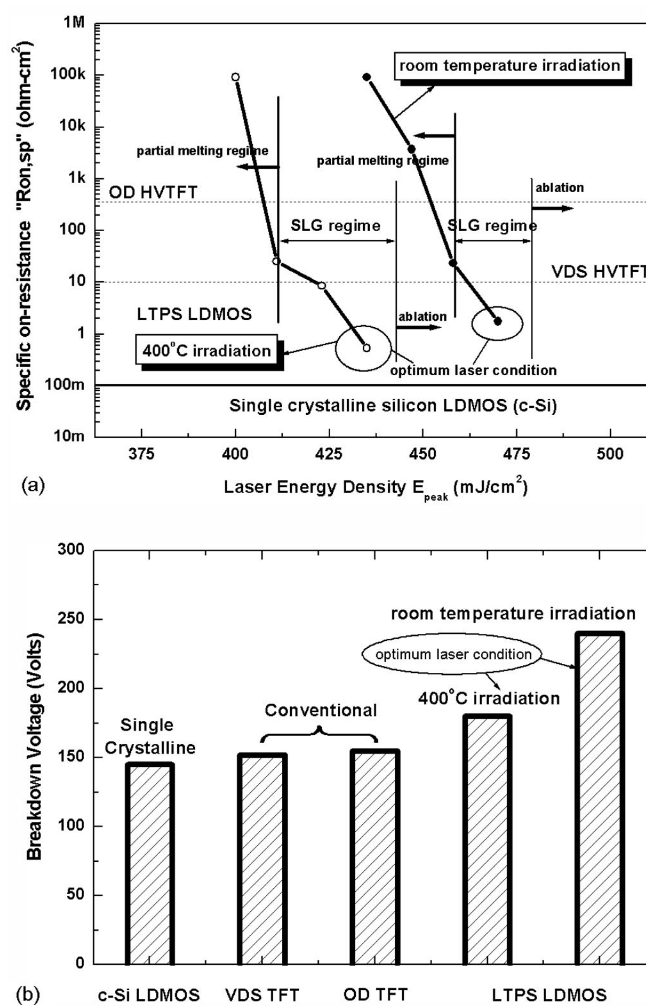

Figure 4. (a). Relationships of the specific on-resistance and laser energy density for LTPS LDMOS at RT/400°C irradiation together with OD TFT, VDS TFT, and c-Si LDMOS. Optimal laser conditions are located at 470 and 435 mJ/cm^2 for room temperature and 400°C, respectively. (b). Comparison of the breakdown voltages for the LTPS LDMOS at RT/400°C irradiation together with OD TFT, VDS TFT, and c-Si LDMOS.

crystalline silicon devices.[10] In regard to the conventional high-voltage TFT, the breakdown voltage of OD TFT (155 V) was slightly larger than that of V_{DS} TFT (152 V). The reason for this was the offset region doping, which generated a higher electric field even though the V_{DS} TFT had utilized a set of variable doping slots to split the potential drop. The proposed LTPS LDMOS at room temperature and 400°C irradiation exhibited excellent breakdown voltages of 240 and 180 V, respectively. Therefore, according to the results of Fig. 4a and b, the LTPS LDMOS, regardless of room temperature or 400°C irradiation, is really a promising power device in low-temperature poly-Si application rather than the conventional high-voltage TFT.

Conclusions

A power device called LTPS LDMOS is reported for the first time to attain the high driving and high blocking capability with excimer laser annealing at 400°C. The device can handle a much higher current of 10 mA, a better power limit of 1.11 W, and provide a much lower specific on-resistance of 0.54 Ω-cm^2. The resultant characteristics for the 400°C irradiation are very close to the c-Si LDMOS. Hence, the proposed LTPS LDMOS devices are suitable for future system-on-a-panel (SOP) applications.

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