Fully Silicided NiSi and Germanided NiGe Dual Gates on SiO_2 n- and p-MOSFETs

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***Abstract*—We have fabricated the fully silicided NiSi and germanided NiGe dual gates n- and p-MOSFETs on 1.9 nm thick SiO_2 gate dielectric. The extracted work functions of fully NiSi and NiGe gates from thickness-dependent flat band voltage were 4.55 and 5.2 eV respectively, which may provide possible wide work function tuning using $NiSi_{1-x}Ge_x$. In additional to the lower gate current than Al gate n- and p-MOSFETs, the fully silicided NiSi and germanided NiGe gates MOSFETs show electron and hole mobilities close to universal mobility values with special advantage of process compatible to current VLSI fabrication line.**

***Index Terms*—MOSFET, NiGe, NiSi.**

I. INTRODUCTION

TO CONTINUE the VLSI scaling trend, high-κ gate dielectrics [1]–[5] on strained Si [6] or Ge-on-insulator (GOI) [7] is required for advanced MOSFET. This is because the high-κ gate dielectrics can reduce equivalent-oxide-thickness (EOT) and the leakage current while the strained Si or GOI can effectively improve the mobility and transistor's drive current. To further improve the MOSFET performance, metal gate [2], [8]–[15] is highly required that can effectively reduce the EOT and increase the drive current similar to use high-κ gate dielectrics. Among various metal gates, the fully silicided gates [6], [11]–[15] have especial advantage of process compatible to current VLSI. In this paper, we have integrated fully silicided NiSi [12]–[15] and novel germanided NiGe dual gates on n- and p-MOSFETs with 1.9 nm thick SiO_2 gate dielectric. By comparing with other high temperature stable metal gates, the newly developed fully germanided NiGe gate has the same advantage as fully silicided NiSi of process compatibility to current VLSI but with higher work function of 5.2 eV than 4.55 eV of NiSi. The same 400 °C low temperature of NiGe germanidation with NiSi silicidation is also important to prevent metal diffusion through gate dielectric [15], [16]. The large work function difference can provide additional merit of wide tuning range using $NiSi_{1-x}Ge_x$[17]. Good device performance of these dual gates on SiO_2 are evidenced from the lower gate leakage current than control Al gate and electron and hole mobilities close to universal mobility values.

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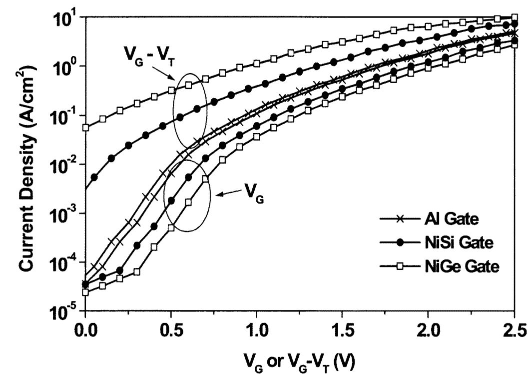

Fig. 1. J_G–V_G and J_G–(V_G–V_T) characteristics of $NiSi/SiO_2$, $NiGe/SiO_2$, and Al/SiO_2 MOSFETs measured under inversion. The oxide thickness is 1.9 nm.

II. EXPERIMENTAL

Standard 4-in p- and n-type Si wafers with resistivity $1 \sim 10\ \Omega$-cm were used for respective n- and p-MOSFETs. After standard RCA clean, a 500 nm isolation SiO_2 was deposited on Si substrate. The source and drain region were implanted with 35 KeV Phosphorus or 25 KeV Boron for n- and p-MOSFETs respectively, followed by RTA activation. Then 1.9-nm thick SiO_2 gate dielectric was grown in dilute O_2 at 900 °C followed by dual silicided and germanided gates formation. The fully NiSi and NiGe gates were formed by depositing 15 nm amorphous Si or Ge on gate oxide, 15 nm Ni for both n- and p-devices, and followed by silicidation and germanidation at 400 °C RTA for 30 s [15]. The excess Ni on gate and source-drain areas was etched by HCl solution, but the excess Ni during NiSi or NiGe formation may diffuse through the ultra-thin gate oxide at higher RTA temperature. For comparison, Al metal gate devices were also fabricated. The fabricated fully silicided and germanided dual gates n- and p-MOSFETs were further characterized by capacitance–voltage (C–V) and current–voltage (I–V) measurements.

III. RESULTS AND DISCUSSION

Fig. 1 shows the comparison of gate dielectric leakage current of $NiSi/SiO_2$, $NiGe/SiO_2$ and Al/SiO_2 MOSFETs. The lower leakage current of fully $NiSi/SiO_2$ and $NiGe/SiO_2$ capacitors

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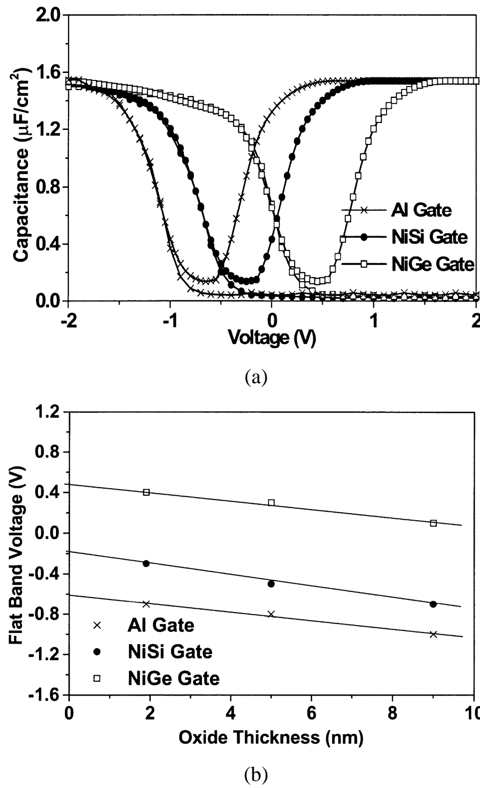

Fig. 2. (a) Quasi-static and 100 MHz C–V characteristics and (b) the V_{fb} versus SiO_2 thickness plot with fully NiSi, NiGe, and Al gates on SiO_2 gate dielectric n-MOSFETs. The gate length is 10 μm and width is 100 μm.

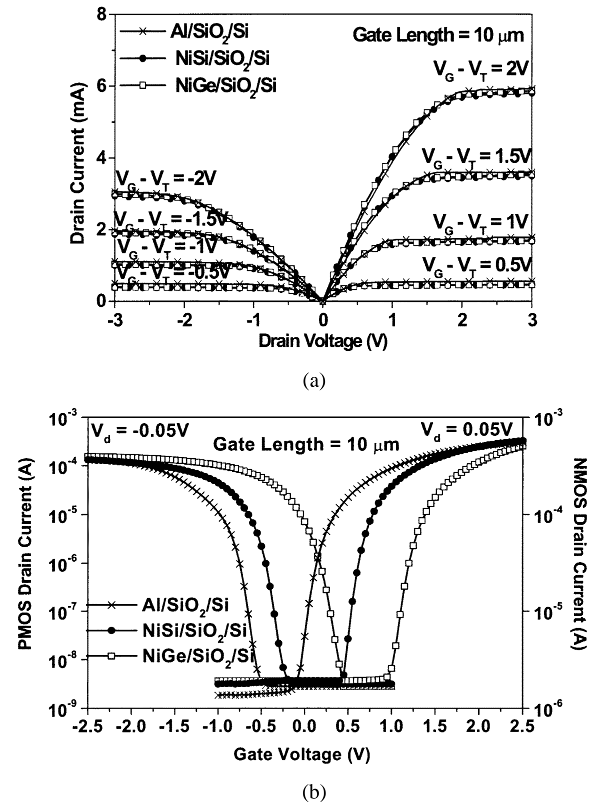

Fig. 3. (a) I_D–V_D and (b) I_D–V_G characteristics of SiO_2 gate dielectric n- and p-MOSFETs with fully NiSi, NiGe, and Al gates. The gate length is 10 μm. The V_t's for Al, NiSi, and NiGe on SiO_2 /n-Si devices are is -0.98, -0.546, and 0.06 V, while on SiO_2 /p-Si cases are 0.05, 0.55, and 1.1 0 V, respectively. The gate length is 10 μm and width is 100 μm.

than Al gate devices may be due to the larger work function than Al [14]. The higher leakage current, after re-plotting the J_G with V_G-V_T, may be due to the slight Ni diffusion [15], [16] to ultrathin 1.9 nm thick gate oxide. Further improvement may be expected using oxynitride and optimized the thermal cycle of source–drain contacts that is formed with gate at the same time. Therefore, the low silicidation and germanidation temperature for fully NiSi and NiGe gates are the important factor to preserve good gate dielectric integrity since the metal diffusion through gate dielectric increases exponentially with temperature.

We have further characterized the NiSi/SiO_2 and NiGe/SiO_2 capacitors. Fig. 2(a) shows C–V characteristics of NiSi/SiO_2, NiGe/SiO_2, and Al/SiO_2 n-MOSFETs. The same inversion and accumulation capacitance value indicates that the NiSi and NiGe gates are fully silicided or germanided without poly-Si depletion. An oxide thickness of 1.9 nm is obtained from the measured capacitance of NiSi/SiO_2, NiGe/SiO_2, and Al/SiO_2 n-MOSFETs, while the shift of C–V curves with different gate electrodes are due to different work function. The work function was further accurately determined from the flat band voltage (V_{fb}) as a function different SiO_2 thickness shown in Fig. 2(b). The extracted work function for NiSi and NiGe is 4.55 and 5.2 eV respectively, which may be due to different lattice constant measured by electron diffraction to give different electron filling level. It is important to note that wide V_{fb} tuning range is possible using $NiSi_{1-x}Ge_x$[17] and the high work function for NiGe is required for high-κ gate dielectric [8].

Fig. 3(a) and (b) present the I_D-V_D and I_D–V_G characteristics of fully silicided NiSi/SiO_2, germanided NiGe/SiO_2, and Al/SiO_2 n- and p-MOSFETs. The nearly same I_D–V_D values, as a function of V_G-V_T, of NiSi and NiGe with Al control MOSFETs indicates little device performance degradation using fully NiSi and NiGe gates. This result also suggests low metal diffusion into NiSi/SiO_2 and NiGe/SiO_2 interface [15], [16], which is due to the 400 °C low formation temperature even though excess Ni must be used to avoid un-reacted poly-Si or poly-Ge to cause poly depletion. The relatively high off-state current in n-MOSFET may be due to the insufficient implant annealing at 900 °C to give large drain leakage current. Further improvement is possible by raising the annealing temperature.

Fig. 4(a) and (b) show the extracted electron and hole motilities versus gate electric field from measured I_D–V_G curves of n- and p-MOSFETs, respectively. The peak electron mobilities of NiSi, NiGe, and Al gates are 412, 416, and 425 cm^2/V-s, and the hole mobilities are 157, 160, and 165 cm^2/V-s, respectively. In additional to close mobilities to Al gate control devices, close values of electron and hole mobility to universal mobility are also observed using fully NiSi and NiGe gates. This indicates the successful integration of fully silicided NiSi and germanided NiGe gates on SiO_2 MOSFETs with advantage of process compatible to current VLSI line.

IV. Conclusion

Good device performance of fully silicided NiSi/SiO_2 and germanided NiGe/SiO_2 n- and p-MOSFETs are demonstrated with electron and hole mobilities close to universal mobility

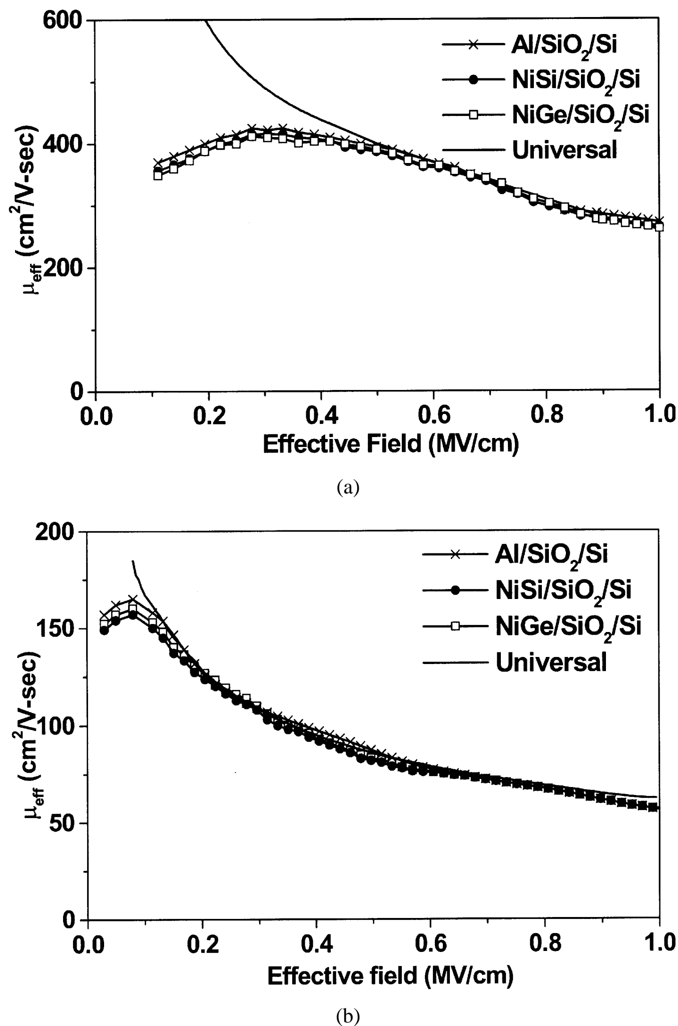

Fig. 4. Extracted (a) electron and (b) hole mobilities from I_D-V_G characteristics of SiO_2 gate dielectric n- and p-MOSFETs with fully NiSi, NiGe, and Al gates.

values. The fully silicided NiSi and germanided NiGe gates with large work function difference are promising for dual gate and work function engineering with process compatible to current VLSI line.

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