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ORIGINAL ARTICLE

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Pull system for control and dummy wafers

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Abstract Various C\D wafers (Control and Dummy wafers) are used in wafer fabrication to enhance product quality and process stability. Most wafer fabs downgrade used C\D wafers into other functional ones and then recycle them to reduce costs. Wafer costs increase with wafer diameter, and thus the downgrading mechanisms and inventory control of C\D wafers have become increasingly important to fab performance. Wafer fabs now are willing to seriously consider C\D wafer management but C\D wafer management remains neglected in the literature. This study presents a novel pull system focusing on inventory and downgrading management of C\D wafers. The proposed system in this study intends to reduce the WIP level of C\D wafers, increase recycled usages (number of times C\D-wafer lots are recycled) before scraping, and reduce machine delay ratio without lowering the product wafer throughput rate.

Keywords Control wafers · Dummy wafers · Pull system · Inventory control · Downgrading path · Recycled usages

1 Introduction

Control wafers (test wafers) and dummy wafers are necessities in wafer fabrication because most equipment requires them to ensure precise process control and normal equipment operation. Control wafers are used to measure manufacturing parameters such as particle numbers, film thickness, refraction indices, and etching rates. Furnaces, on the other hand, utilise dummy wafers to uniformly distribute heat inside the pipes. These two different types of wafers, applied for different purposes, are treated the same in this study because they both face the same downgrading and recycling problems. Most control wafers will finally be downgraded to dummy wafers after recycling.

C\D wafers significantly impact the operational cost of a wafer fab because they are used in very large quantities and the cost increases as the diameter of the wafer grows. Foster et al. [1, 2] indicated that a fab starts 0.1 to 3 test wafers for every product wafer. The WIP level of C\D wafers may reach 30,000 or even more pieces for a wafer fab that yields 30,000 pieces of product wafers a month. This fact implies that the accumulated capital exceeds 1.2 million U.S. dollars if each piece of C\D wafer (8 inches in diameter) costs USD40. Wafer fabs have already realised this issue and commenced with C\D-wafer management, which includes reducing C\D-wafer quantities and increasing C\D-wafer recycled usages.

In practice, each piece of C\D wafer will be applied several times and then downgraded to different functional areas through recycling to prolong its life. In an ideal production environment, each C\D-wafer lot follows the pre-defined route for downgrading. However, different consumption rates of C\D wafers may lead to a shortage as the demand increases when equipment breaks down. In addition, urgent requirements may unexpectedly emerge when the cleanliness of a C\D-wafer lot is out of its specification. Efficient downgrading mechanisms for C\D wafers have therefore become a significant issue in increasing their economic value.

To our knowledge, no systematic scheme of C\D-wafer management has yet been proposed in the various research papers. Downgrading rules and inventory control, in practice, depend on the supervi-

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sor's experience and intuition. This paper proposes a pull system to determine the way of downgrading and the target stock level of C\D wafers.

2 Problem analysis

The consumption process of C\D wafers can be divided into three stages, preparation, in-use, and recycling, termed PUR herein. Figure 1 illustrates a PUR process of a specific functional C\D wafer used to measure etching rates. This C\D wafer requires a photoresist coating on its surface (Photo Resist Coat) and a baking photoresist (PR Bake) coat before it can be applied. These two steps are part of the preparation stage, while the etching itself and pre- as well as post-etching thickness measurements belong to the in-use stage. Finally, the removal of the photoresist belongs to the recycling stage.

The operations of C\D wafers during the preparation and recycling stages occupy equipment capacity just as product wafers do. However, the use of C\D wafers during the in-use stage can be divided into five parts [3, 4, 5]: (1) product monitoring, (2) equipment monitoring, (3) preventive maintenance, (4) experimentation with engineering lots, and (5) equipment repair in the event of breakdowns. The C\D wafer depletion can temporarily stop the operation of in-use machines and delay the product wafer production.

C\D wafers are often recycled several times (PUR process). A C\D-wafer lot can repeat the same functional test until it reaches its recycling limits (owing to cleanliness or thickness requirements), and such kind of recycling is referred to herein as internal downgrading. Meanwhile, a C\D-wafer lot could also be downgraded to a different functional C\D-wafer lot if it fails to meet pre-defined specifications, called external downgrading. Furthermore, the release of new raw wafers as any kind of C\D wafers is also regarded as external downgrading. Figure 2 displays the usage flow of C\D wafers. Theoretically, managers can directly use new raw wafers as C\D wafers with any function and then discard them immediately after their first use, although this method is obviously not cost-effective.

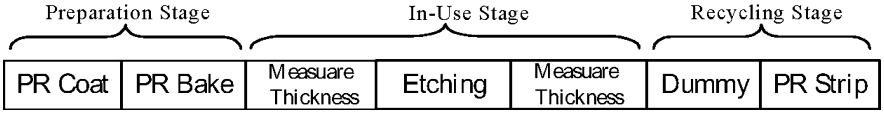


Fig. 1 The PUR process for etching-rate measurement

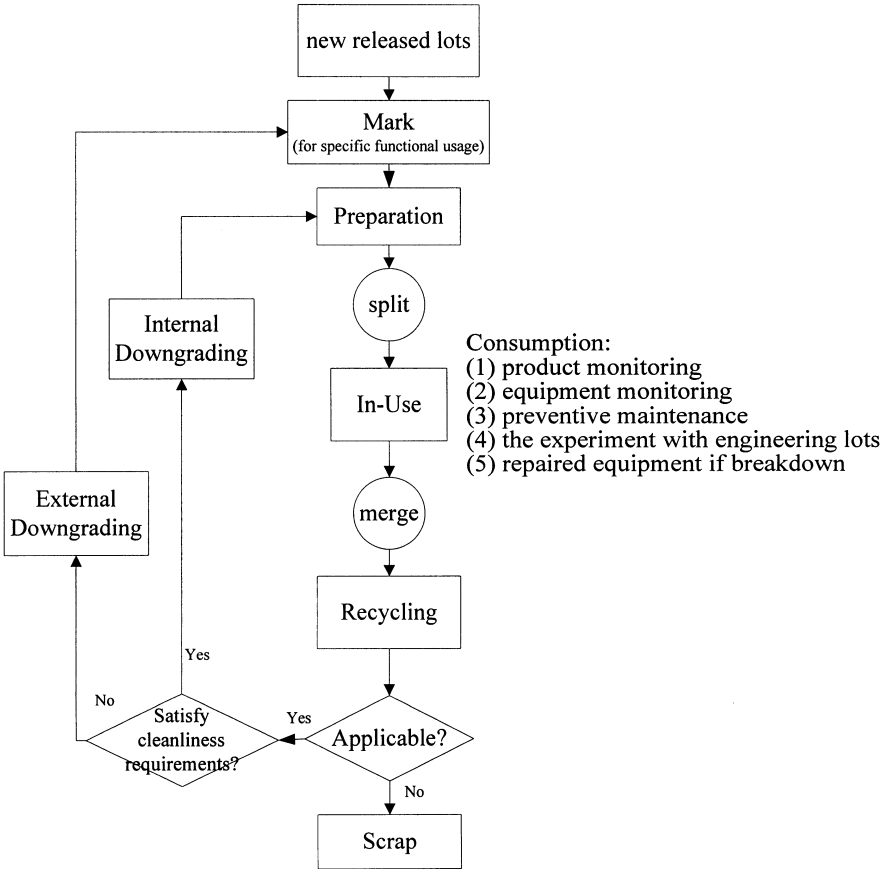


Fig. 2 The usage flow of C\D wafers

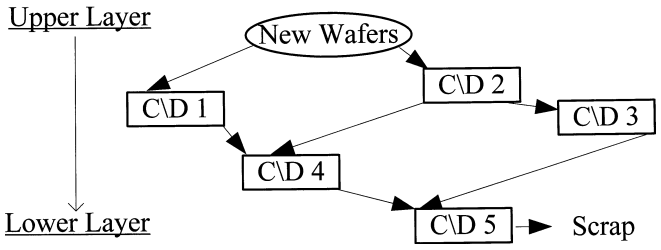


Fig. 3 Simplified downgrading graph

The minimum downgrading unit is generally one C\D-wafer lot at a time.

External downgrading actions are restricted to specific functional C\D wafers due to the process characteristics. C\D wafers can be categorised according to the external downgrading restrictions. This study defines simplified downgrading graphs to express all possible external downgradings, as illustrated in Fig. 3. C\D wafers with different simplified downgrading graphs cannot be mutually downgraded. Furthermore, only the C\D wafers (source C\D wafers) in the upper layers of the simplified downgrading graph can be downgraded to other functional C\D wafers (target C\D wafers) in the lower layers. A path in the simplified downgrading graph must connect both the source and target C\D wafers. For instance, the lot of C\D wafer 1 (C\D 1; source) can be downgraded to C\D wafer 4 (C\D 4; target), or can be downgraded directly to C\D wafer 5 (C\D 5; target) without first being C\D 4. Control wafers are mostly located in the upper layers of the simplified downgrading graph, while dummy wafers are normally located in the lower layers.

Both internal and external downgradings must be considered at every downgrading decision to increase recycled usages of C\D-wafer lots before being scrapped. C\D-wafer lots with more recycled usages imply that they experience more PUR processes than those with less recycled usages, thus prolonging their lives and reducing costs. However, C\D-wafer lots do not need to experience all pre-determined PUR processes, since they can skip the remaining PUR processes and proceed with different functional tests if necessary. The simplified downgrading graph can be transformed into a general downgrading graph to express all pre-determined PUR processes, and this general downgrading graph, illustrated in Fig. 4, can then be used to demonstrate the pull system in the following sections.

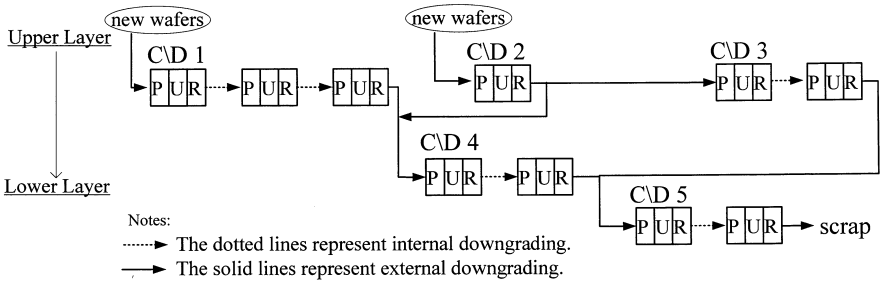
The pull system defines an available buffer before the in-use stage and a downgradeable buffer after the recycling stage for every PUR process. C\D-wafer lots accumulate in the available buffer after completing the preparation stage, and the number of lots is termed the available quantity. Similarly, C\D-wafer lots accumulate in the downgradeable buffer after completing the recycling stage, and the number of lots is termed the downgradeable quantity. The sum of the available quantities belonging to the same functional C\D wafer is called the total available quantity, while the sum of the downgradeable quantities belonging to the same functional C\D wafer is called the total downgradeable quantity. The pull system also specifies individual target stock levels at each available buffer. Downgrading only occurs when the available quantity is below the target stock level. It is assumed that serial type machines follow the first-in-first-out rule (FIFO) and batch type machines comply with the minimum batch size rule (MBS) [6]. Figure 5 displays the material flow inside the first PUR process of any functional C\D-wafer.

3 Inventory control

The pull system adopts the periodic inventory system [7, 8], a time-based inventory system, to increase the recycled usages of C\D-wafer lots. The downgrading quantity is variable and placed at regular decision intervals to raise the stock to the individual target stock level (ITSL). The inventory control of the pull system must determine two parameters: the decision interval and ITSL of each PUR process.

The decision interval affects the cost of the C\D-wafer management. The cost of C\D-wafer management includes WIP level, recycled usages, throughput rate of product wafers and shortages of C\D wafers. The first two items are related to the decision interval, while the rest are related to the ITSL. The optimal decision interval minimises the cost of the recycled usages and the WIP level. However, the cost function of the decision interval is difficult to formulate since the relationship between recycled usages and the decision interval is uncertain, especially when each recycling has a different value. Therefore, this study proposes a heuristic method rather than an optimal one to determine the decision interval. A short decision interval should be adopted herein since conventional JIT theory suggests a small

Fig. 4 General downgrading graph



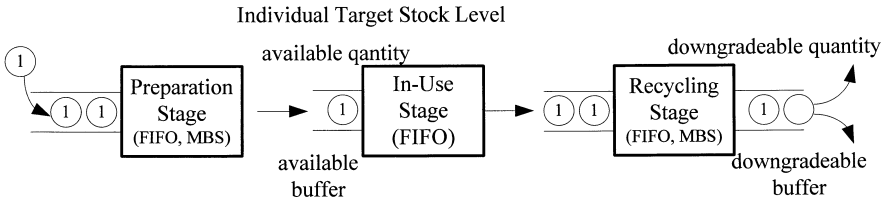


Fig. 5 Material flow inside the first PUR process

Note1: A circle represents a C\D-wafer lot; the figure in the circle represents its recycled usages.
Note2: Product wafer lots are not shown in this illustration.

time period. A small time interval does lead to a lower ITSL value and WIP level. However, the decision interval should not be shortened unconditionally since the replenishment of each C\D wafer at the available buffer only occurs after its preparation time (the flow time through the preparation stage). Meanwhile, a shorter decision interval may result in excessive downgrading quantities. This study adopts the maximum preparation time from all kinds of C\D wafers as the decision interval shown in Eq. 1. This maximum preparation time represents the minimum time required to sufficiently replenish all kinds of C\D wafers at the available buffers.

$$\text{Decision Interval} = Max\{\overline{PT}_i\} \qquad i = 1, ..., k \tag{1}$$

$\overline{PT}_i$: average preparation time of C\D wafer i
k: the number of different types of C\D wafers

The individual target stock level (ITSL) is indirectly determined by the decision interval. The pull system works by examining the available quantity of each PUR process at a decision interval and downgrading the amount which brings the stock up to ITSL. Since ITSL is based on PUR processes, total target stock level (TTSL) for every kind of C\D wafer should be calculated first and based on the usage during the preparation time, the usage during the decision interval, and the safety stock level. TTSL equals the total available quantities $\overline{AB}$ of all available buffers plus the total downgrading quantities $\overline{CD}$, as displayed in Fig. 6. Meanwhile, $\overline{AB}$ includes the safety stock level and C\D-wafer consumption during the preparation time. The total downgrading quantity $\overline{CD}$ must fulfill all consumption until the arrival of the next total downgrading quantity. When preparation time and consumption amount are normally distributed and independent, the TTSL is formulated using Eq. 2 and the safety stock level is calculated using Eq. 3.

$$\begin{aligned} TTSL_i &= \overline{AB} + \overline{CD} \\ &= \text{total available quantity} \\ &\quad + \text{total downgrading quantity} \\ &= \text{total available quantity} + \text{consumption over } DI \\ &= \text{consumption over } PT + \text{safety stock level}_i \\ &\quad + \text{consumption over } DI \\ &= \text{consumption over}(DI + PT) + \text{safety stock level}_i \\ &= DI * \overline{D}_i + \overline{PT}_i * \overline{D}_i + Z * \sqrt{\overline{PT}_i * \sigma_{Di}^2 + \overline{D}_i^2 \sigma_{PTi}^2} \end{aligned} \tag{2}$$

$$\text{Safety stock level}_i = Z * \text{standard deviation of demand during lead time}$$

$$= Z * \sqrt{\overline{PT}_i * \sigma_{Di}^2 + \overline{D}_i^2 \sigma_{PTi}^2} \tag{3}$$

Where
Z the number of standard deviations from the mean corresponding to the selected service level,
$\overline{PT}_i$ average preparation time of C\D-wafer i,

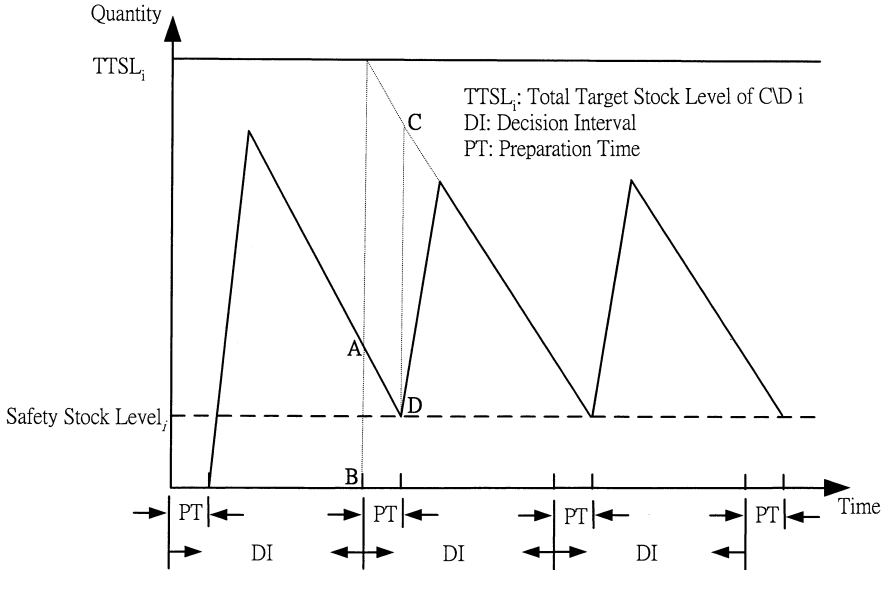


Fig. 6 Variation of total available quantities from the same functional C\D wafer

D_i average consumption of C\D-wafer i,
σ_{Di} standard deviation of consumption distribution of C\D-wafer i,
σ_{PT_I} standard deviation of preparation time distribution of C\D-wafer i.

After calculating $TTSL_i$ of C\D-wafer i, all PUR processes belonging to C\D-wafer i require the same ITSL value at the available buffer to determine the downgrading quantity at regular decision intervals. Therefore, the $TTSL_i$ is divided by the maximum recycled usages of C\D-wafer i to calculate the $ITSL_i$ as shown in Eq. 4. In addition, the ITSL value should be rounded up as the minimum downgrading unit is a single lot.

$$ITSL_i = round\,up(TTSL_i/\text{Max recycling usages of C\D wafer } i) \quad (4)$$

Manufacturing data, including mean consumption rate, standard deviation of consumption, mean preparation time, and standard deviation of the preparation time of each C\D-wafer lot, should be collected before calculating the individual target stock level of each PUR process.

4 Downgrading mechanism

A downgrading mechanism periodically determines which PUR processes are the targets and sources of the downgrading and how many lots targets demand and sources supply. Multiple C\D-wafer targets and sources may happen during the decision interval and the targets with C\D-wafer demand could normally get downgradeable quantities from the nearer upstream sources. Consequently, the periodic downgrading mechanism reduces the number of skipped PUR processes and increases the recycled usages.

4.1 Release and downgrading procedure

Step 1 Calculate the comparative downgrading costs before the first decision.

The cost of each possible downgrading action should be considered to make an economical downgrading decision. However, it is difficult to estimate the cost because different functional C\D wafers have different values. Therefore, the pull mechanism estimates the comparative cost of each downgrading by the distance from the source node (PUR process) to the target node in the general downgrading graph. Although many paths may exist from the source to target C\D wafer in the general downgrading graph, the longest path should be applied to be the comparative downgrading cost in the pull mechanism because cost estimation should be based on the maximum loss [9]. The comparative downgrading cost from C\D wafers in the lower layers to those in the upper layers will be infinite because the downgrading graph belongs to a non-cyclic network. This configuration totally complies with the downgrading principle since only upper-layer C\D wafers could be downgraded to lower-layer ones. Equation 5 shows the calculation of all comparative downgrading costs.

$$c_{ij} = \begin{cases} Max\{d(i,j)\} & \text{if there is a path from } i \text{ to } j. \\ \infty & \text{otherwise} \end{cases} \quad (5)$$

$d(i, j)$ the distance from source node i to target node j
c_{ij} the shipping cost per unit of the downgrading lot from node i to node j

Step 2 Determine downgrading and C\D-wafer release at every decision interval.

According to the discussion in Sect. 3, the heuristic decision interval is set to the maximum preparation time of all functional C\D-wafer lots. The decision interval configuration will affect C\D-wafer recycled usages and the WIP level.

Step 3 Identify source and target C\D wafers and calculate their supply and demand quantities.

Source C\D wafers include new wafers and all downgradeable C\D-wafer lots in the upper-level C\D-wafer buffers. It is assumed that an infinite amount of new raw wafers can be provided if necessary. C\D-wafer buffers will provide the accumulated downgradeable quantity as shown in Eq. 6. The target C\D wafer consists of all kinds of C\D wafers whose available quantity is lower than the target stock level. The target node requires the difference between the target stock level and the available quantity as shown in Eq. 7.

$$A = \{a_i | a_i = DQ_i, a_i > 0\}, \quad |A| = m, \quad i = 1, \ldots, m \quad (6)$$

$$B = \{b_j | b_j = ITSL_j - AQ_j, b_j > 0\}, |B| = n, j = 1, \ldots, n \quad (7)$$

i source C\D wafers
j target C\D wafers
m the number of source C\D wafers
n the number of target C\D wafers
a_i the supply of source C\D wafer i
b_j the demand (downgrading quantity) of target C\D wafer j
A the set of all supply quantities
B the set of all demand quantities
$ITSL_j$ the individual target stock level of C\D-wafer j
DQ_i the downgradeable quantity of C\D wafer i
AQ_j the available quantity of C\D wafer j

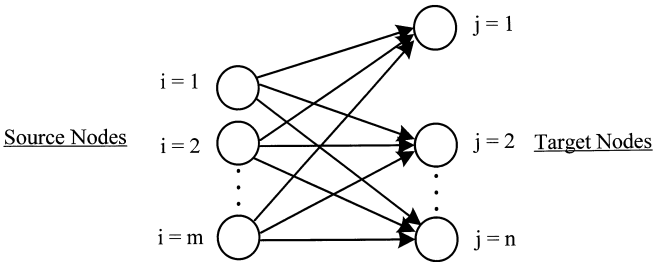


Fig. 7 Depiction of the transportation network

$$\text{Min. } Z = \sum_{i=1}^{m}\sum_{j=1}^{n} c_{ij}x_{ij} \text{ subject to :}$$
$$\sum_{j=1}^{n} x_{ij} \le a_i, \quad i = 1,2,...,m$$
$$\sum_{i=1}^{m} x_{ij} \ge b_j, \quad j = 1,2,...,n \tag{8}$$
$$x_{ij} \ge 0, \quad i = 1,2,...,m;\ j = 1,2,...,n$$

where a_i, b_j, c_{ij} are all nonnegative integers.
x_{ij} the shipping amount from node i to node j
Z the total transportation cost of the transport problem

Step 4 Transform the downgrading problem into a transportation problem and make the downgrading decision.

The downgrading problem of the pull mechanism can be transformed into a transportation problem [10, 11] after Step 1 and Step 3 as depicted in Fig. 7. The source C\D wafers become supply nodes and the target C\D wafers become target nodes. The comparative downgrading cost becomes the shipping cost of the transportation problem. The problem formulated in Eq. 8 consists of m supply nodes and n target nodes. Each supply node i could provide a maximum of a_i units and each target node j requires at least b_j units. Each arc denotes the shipping cost per unit of the downgrading lot c_{ij}. The equation attempts to determine the shipping quantity $x_{ij,}$ which will minimise not only the total transportation cost Z, but also the total number of skipped PUR processes. The transportation problem has a feasible solution if supply is greater than demand, i.e. $\sum_{i=1}^{m} a_i \ge \sum_{j=1}^{n} b_j$. The pull mechanism always has a feasible solution because supply (including new wafers) will be absolutely greater than demand. The pull mechanism's minimum cost solution also creates the most efficient C\D-wafer utilisation. Right after Step 4, the execution goes back to Step 2.

5 Illustrative example

Figure 8 is employed to illustrate a downgrading graph of the illustrative example. Each PUR process is represented by a node. Each downgrading is represented by an arc. This example includes five different functional C\D-wafer types. The first digit of the double-digit figure in the node symbolises the type of C\D-wafer lot, while the second number indicates the recycled usages of the lot. For example, the lot in node 51 has a part number of five and is undergoing its first PUR process. New wafers are the only exception to this system, and use the symbol, node 0. The three numbers outside the node symbolise the individual target stock level (ITSL), available quantity, and downgradeable quantity, respectively. For instance, the three numbers outside node 51 indicate that the ITSL is now configured to three lots, with two lots in the available buffer and one in the downgradeable buffer. Meanwhile, all of these lots are undergoing their first PUR process.

The decision interval and ITSL of each PUR process are first calculated from the simulation data, as shown in Table 1. The decision interval in this example is 1497 minutes, and the ITSL of each PUR process is in 95% service level, as listed in Table 2. Meanwhile, Eqs. 9 and 10 are used to calculate the ITSL in node 51.

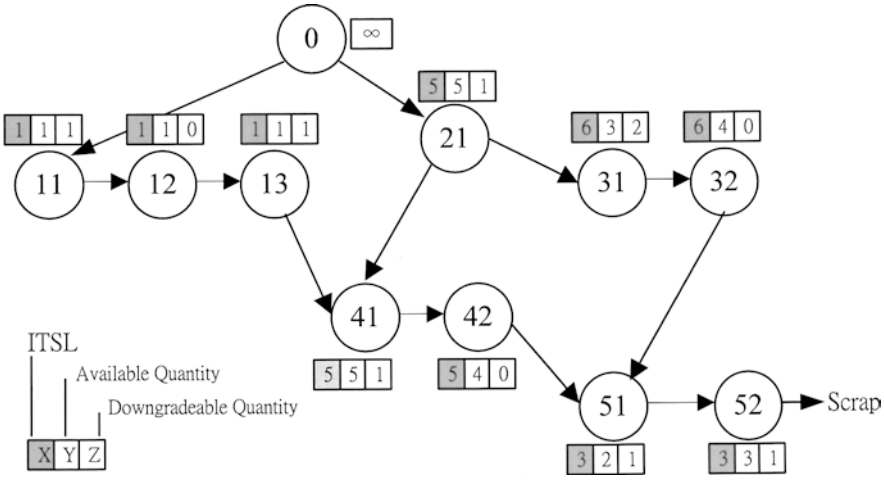


Fig. 8 An example of the downgrading graph

$$\begin{aligned} \textit{Decision Interval} &= \max\{543, 986, 1497, 425, 552\} \\ &= 1497\ \text{Minutes} \end{aligned} \tag{9}$$

$$\begin{aligned} TTSL_5 &= DI * \overline{D_5} + \overline{PT}_5 * \overline{D}_5 + Z * \sqrt{\overline{PT}_5 * \sigma_{D5}^2 + \overline{D}_5^2 \sigma_{PT5}^2} \\ &= 1497 * 0.002355 + 552 * 0.002355 \\ &\quad + 1.64 * \sqrt{552 * 0.000179^2 + 0.002355^2 * 151^2} \\ &= 5.4 \\ ITSL_5 &= \text{round up}\,(5.4/2) = 3\,\text{lots} \end{aligned} \tag{10}$$

The following instance (under the configuration of Fig. 8) demonstrates the decision process of the pull mechanism. First, the shipping costs of all possible downgrading combinations are calculated using the longest length between the corresponding source and target C\D wafers. Consequently, all paths between new wafer 0 and C\D wafer 51 must be identified before calculating the comparative downgrading cost. Three different downgrading paths exist from new wafer 0 to C\D wafer 51, as displayed in Fig. 9. The comparative downgrading cost from C\D wafer 0 to C\D wafer 51 will be six units since the longest path involves six downgradings.

Table 2 Individual target stock level (ITSL) of each node (PUR process)

Node	11	12	13	21	31	32	41	42	51	52
ITSL (lots)	1	1	1	5	6	6	5	5	3	3

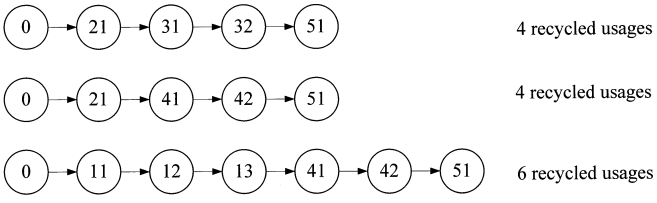


Fig. 9 Possible downgrading paths from C\D wafer 0 to 51

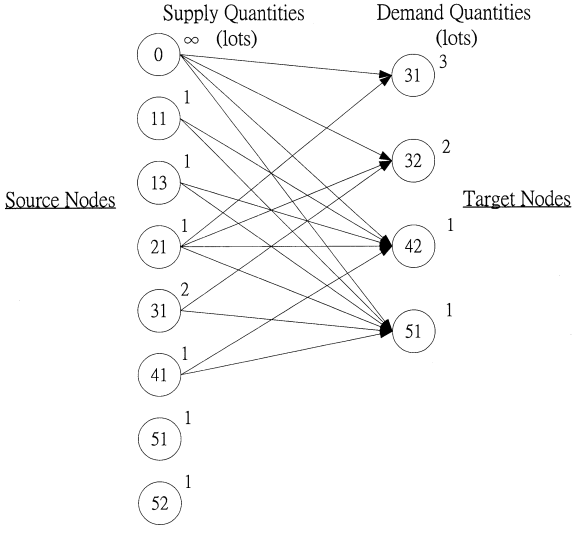


Fig. 10 The relationship among source nodes and target nodes

The mechanism then identifies the source and target C\D wafers and calculates their levels of supply and demand. The target C\D wafers that require replenishment in this example include C\D wafers 31, 32, 42, and 51. The source C\D wafers include C\D wafers 0, 11, 13, 21, 31, 41, 51, and 52. Figure 10 presents the relationship between the source and target nodes. Each arc in the figure represents a possible downgrading. The figure does not include downgradings (arcs) with infinite costs.

The pull mechanism transforms the downgrading problem into a transportation problem below. The solution to the transportation problem is displayed in Table 3. The first column lists all source nodes and the first row lists all target nodes. Both the supply quantity in the last column and the demand quantity in the last row come from manufacturing data in Fig. 8. The shipping costs are calculated and listed in the lower-right corner of each cell. The Ford-Fulkerson algorithm is applied to solve the transportation problem and the shipping quantity x_{ij} is listed in each cell [12]. The figure in each cell represents the number of C\D-wafer lots that will be downgraded from the corresponding source node to the target node. Conversely, the cell without a figure suggests that no downgrading will occur. The downgrading decision comprises two lots of the internal downgrading from C\D wafer 31 to 32 and one lot of the internal downgrading from 41 to 42. External downgradings include one lot from C\D wafer 13 to 51 and one lot from 21 to 31. In addition, two new wafer lots are released to C\D wafer 31 as listed in Table 4.

Table 3 The transformed transportation problem in the pull mechanism

Demand nodes\Supply nodes	31	32	42	51	Supply quantity (lots)
0	2 2	3	5	6 ∞	
11	∞	∞	4	5 1	
13	∞	∞	2	3 1	
21	1 1	2	2	3 1	
31	∞	2 1	∞	2 2	
41	∞	∞	1 1	2 1	
51	∞	∞	∞	∞ 1	
52	∞	∞	∞	∞ 1	
Demand quantity (lots)	3	2	1	1	

Table 4 The release and downgrading decision of the pull mechanism

	Source C\D wafer	Target C\D wafer	Quantity (lots)
Internal downgrading	31	32	2
	41	42	1
External downgrading	13	51	1
	21	31	1
Release new wafers	0	31	2

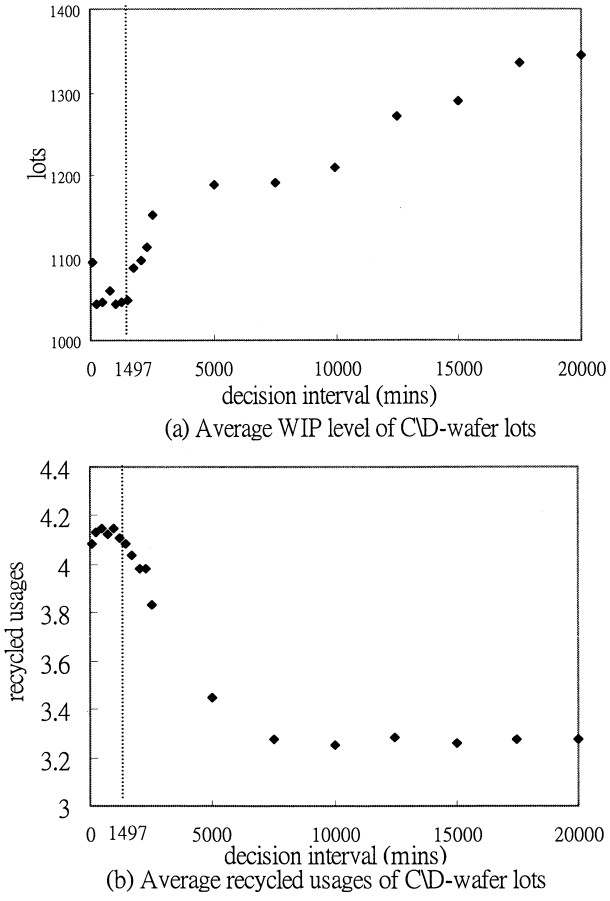


Fig. 11a,b Decision interval vs. **a** Average WIP level. **b** Average recycled usages of C\D-wafer lots in the pull system

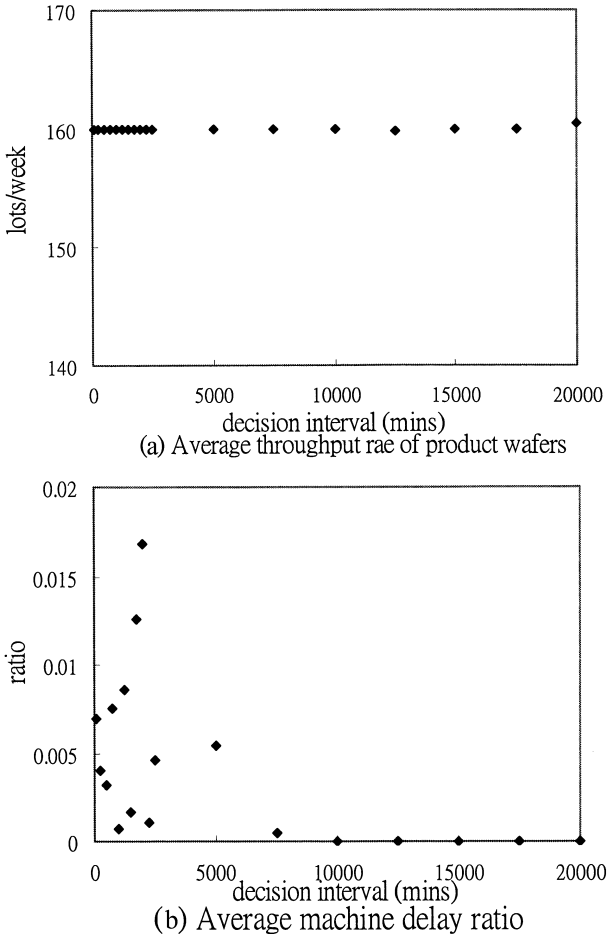


Fig. 12a,b Decision interval vs. **a** Average throughput rate of product wafers. **b** Average machine delay ratio in the pull system

6 Simulation results

To evaluate its performance, the above pull system is applied to a pseudo wafer fab with an assumed downgrading graph as in Fig. 8. Four indices of C\D-wafer management [13] applied here include WIP level, recycled usages of C\D-wafer lots, throughput rate of product-wafer lots, and machine delay ratio. Meanwhile, the manufacturing parameters, shown in the Appendix, are based on those from an actual wafer fabrication factory. The machine groups are assumed to have normally distributed processing times. WIP-to-Bottleneck Control (WB) is adopted as the release rule of the six types of product wafers. FIFO is adopted as the dispatching rule for serial-process machines and MBS is adopted for batch-process machines. The time horizon for each simulation run is 525600 min (one year), and the analysis ignored the data of the first 178560 min (four months) as the warm-up period. The simulation is run ten times for each datum under various random seeds.

Average WIP level and recycled usages of C\D wafers are two direct influences on the cost of C\D-wafer management. The simulation results, displayed in Fig. 11, demonstrate that adopting a longer decision interval increases the WIP level of the C\D wafers and decreases the recycled usages. This simulation result confirms that costs decrease with decision intervals. However, a shorter decision interval increases the WIP level and reduces the recycled usages because of the possibility of excessive downgrading quantities. The decision interval proposed in this example, 1497 min, provides a lower WIP level and more recycled usages than does a longer decision interval.

Additionally, the average throughput rate of product wafers and machine delay ratio are indices of wafer fabrication performance, and are indirectly influenced by the C\D-wafer management system. The average throughput rate of product wafers remains almost constant at 160 lots per week despite ITSL configurations changing with decision interval as shown in Fig. 12. The machine delay ratio is the proportion of machine delay time during the simulation period. The longest delay time occupies just 1.683% of the simulation time given a decision interval of 2000 min, indicating that the ITSL configuration performs well regardless of the decision interval. Additionally, a shorter decision interval may increase demand variation as indicated in Fig. 12.

This section analyses the characteristics of the pull system rather than comparing its performance with that of other systems since the pull system combines inventory control policy, downgrading and the release mechanism. Different systems have unique mechanisms, increasing the difficulty of impartial comparison. Generally, the pull system proposed herein achieves lower WIP level but less recycled usages than the push system [13]. However, determining which system is better is impossible because system performance is influenced by the parameters. The performance of the push system varies with the release interval while that of the pull system varies with the decision interval; although the pull system is less parameter sensitive than the push system. Furthermore, the comprehensive cost function of a C\D-wafer management system is difficult to formulate since it involves the WIP level, recycled usages of C\D wafers, throughput rate of product wafers and machine delay ratio.

7 Conclusion and future research

The purpose of this research is to propose a pull system for C\D wafers with inventory and downgrading management. This pull system differs from other kanban systems, which are based on the fixed single production line, but deals with more complex dynamic systems (job shops) where the process sequence of C\D wafers goes through alternative routes. The time-based inventory control policy is simple and convenient to manage since the stock level does not have to be monitored continuously. The downgrading mechanism applied with transportation problems helps to find proper downgrading paths effectively. The simulation results indicate that this pull system leads to a low WIP level, high recycled usages of C\D wafers, low machine delay ratio but does not decrease the throughput rate of product wafers.

The pull system presented in this study is not necessarily the optimal mechanism. However, for firms attempting to proceed with systematic C\D-wafer management, it is certainly a feasible approach although further studies would also be worthwhile. Optimising the decision interval could be one direction of future research since a shorter decision interval can lead to serious WIP accumulation. Additionally, the evaluation of the downgrading cost can also be considered since the value of functional C\D wafers differs.

Appendix

Pertinent data of the example fab are contained in Tables 5, 6, 7, 8, 9, 10, 11, 12, 13 and 14.

Table 5 Machine data

Machine group	Number of machines	Batch size (lots)	Machine group	Number of machines	Batch size (lots)
0*	1	6	20	2	1
1	1	1	21*	4	6
2	3	1	22*	2	6
3	0	1	23*	3	6
4	3	1	24*	3	6
5	2	1	25	3	1
6	2	1	26	10	1
7	2	1	27*	2	6
8	0	1	28*	2	6
9	2	1	29	2	1
10	1	1	30	0	1
11*	3	6	31*	1	6
12	0	1	32	1	1
13	1	1	33	2	1
14	1	1	34*	2	6
15	1	1	35	0	1
16	6	1	36	0	1
17	2	1	37*	2	6
18	0	1	38	2	1
19	0	1			

*: Batch machines

Table 6 Mean processing time and its variance of each recipe at each machine group (min)

Machine group	Recipe	Mean processing time	Variance of processing time
0	1	104	5.2
1	1	54	2.7
2	1	157	7.8
3	1	99	4.9
4	1	129	6.4
	2	131	6.5
5	1	86	4.3
6	1	121	6
7	1	84	4.2
	2	83	4.15
	3	85	4.25
9	1	50	2.5
	2	49	2.45
	3	48	2.4
10	1	55	2.75
11	1	318	15.9
	2	320	16.15
	3	317	15.85
13	1	57	2.85
14	1	55	2.75
15	1	86	4.3
16	1	158	7.9
	2	156	7.8
17	1	14	0.7
20	1	50	2.5
21	1	460	23
	2	455	22.75
22	1	459	22.95
23	1	459	22.95
	2	460	23
	3	458	22.9
24	1	228	11.4
25	1	84	4.2
	2	80	4
26	1	50	2.5
	2	48	2.4
	3	48	2.4
	4	49	2.45

Table 6 Continued

Machine group	Recipe	Mean processing time	Variance of processing time
27	1	344	17.2
	2	345	17.25
	3	343	17.15
28	1	343	17.15
	2	346	17.3
29	1	104	5.2
31	1	210	10.5
32	1	130	6.5
33	1	87	4.35
34	1	394	19.7
36	1	77	3.85
37	1	460	23
38	1	28	1.4

Table 7 Standard WIP of product wafers in Layer 0

Product	A	B	C	D	E	F
Standard WIP (lots)	2.158	3.164	4.176	5.322	1.037	2.115

Table 8 Data for product A

Sequence	Machine group	Recipe	Stage	Layer	Sequence	Machine group	Recipe	Stage	Layer
1	31	1	0	0	35	26	4	75	15
2	24	1	1	0	36	16	2	61	11
3	20	1	2	0	37	34	1	62	11
4	26	1	3	0	38	28	1	63	11
5	9	1	4	1	39	27	1	64	11
6	17	1	5	1	40	26	2	65	11
7	21	1	6	1	41	7	2	66	12
8	38	1	7	1	42	26	1	67	12
9	17	1	8	1	43	16	1	76	16
10	37	1	9	1	44	2	1	77	16
11	24	1	10	1	45	11	1	78	16
12	20	1	11	1	46	26	2	79	16
13	26	2	12	1	47	5	1	80	17
14	9	1	13	2	48	11	3	81	17
15	26	1	14	2	49	33	1	82	17
16	17	1	15	3	50	26	3	83	17
17	21	2	16	3	51	4	1	84	18
18	38	1	17	3	52	15	1	85	18
19	24	1	18	3	53	32	1	86	18
20	17	1	19	3	54	15	1	87	18
21	22	1	20	3	55	26	2	88	18
22	28	1	21	3	56	5	1	93	20
23	1	1	22	3	57	33	1	94	20
24	27	1	23	3	58	26	1	95	20
25	26	2	24	3	59	4	2	96	21
26	7	1	38	6	60	25	1	97	21
27	11	1	39	6	61	25	2	98	21
28	26	1	40	6	62	26	1	99	21
29	17	1	56	10	63	6	1	100	22
30	34	1	57	10	64	0	1	101	22
31	10	1	58	10	65	14	1	102	22
32	23	3	59	10	66	13	1	103	22
33	26	1	60	10	67	29	1	104	22
34	16	1	74	15					

Table 9 Data for product B

Sequence	Machine group	Recipe	Stage	Layer	Sequence	Machine group	Recipe	Recipe	Layer
1	31	1	0	0	32	34	1	57	10
2	24	1	1	0	33	10	1	58	10
3	20	1	2	0	34	23	3	59	15
4	26	1	3	0	35	26	1	60	15
5	9	1	4	1	36	16	1	74	11
6	17	1	5	1	37	26	4	75	11
7	21	1	6	1	38	16	1	76	11
8	38	1	7	1	39	2	1	77	11
9	17	1	8	1	40	11	1	78	11
10	37	1	9	1	41	26	2	79	12
11	24	1	10	1	42	5	1	80	12
12	20	1	11	1	43	11	3	81	16
13	26	2	12	1	44	33	1	82	16
14	9	1	13	2	45	26	3	83	16
15	26	1	14	2	46	4	1	84	16
16	17	1	33	5	47	15	1	85	17
17	21	2	34	3	48	33	1	86	17
18	38	1	35	3	49	15	1	87	17
19	24	1	36	3	50	26	2	88	17
20	26	1	37	3	51	5	1	93	18
21	17	1	41	3	52	33	1	94	18
22	17	1	42	3	53	26	1	95	18
23	22	1	43	3	54	4	2	96	18
24	28	1	44	3	55	25	1	97	18
25	1	1	45	3	56	25	2	98	20
26	27	1	46	6	57	26	1	99	20
27	26	2	47	6	58	6	1	100	20
28	7	1	53	6	59	0	1	101	21
29	23	1	54	10	60	14	1	102	21
30	26	1	55	10	61	13	1	103	21
31	17	1	56	10	62	29	1	104	21

Table 10 Data for product C

Sequence	Machine group	Recipe	Stage	Layer	Sequence	Machine group	Recipe	Stage	Layer
1	31	1	0	0	29	7	2	66	12
2	24	1	1	0	30	26	1	67	12
3	20	1	2	0	31	17	1	68	13
4	26	1	3	0	32	26	1	69	13
5	9	1	4	1	33	9	3	70	14
6	17	1	5	1	34	10	1	71	14
7	21	1	6	1	35	34	1	72	14
8	38	1	7	1	36	26	1	73	14
9	17	1	8	1	37	16	1	74	15
10	37	1	9	1	38	26	4	75	15
11	24	1	10	1	39	16	1	76	16
12	20	1	11	1	40	2	1	77	16
13	26	2	12	1	41	11	1	78	16
14	9	1	13	2	42	26	2	79	16
15	26	1	14	2	43	5	1	80	17
16	17	1	25	4	44	11	3	81	17
17	21	2	26	4	45	33	1	82	17
18	38	1	27	4	46	26	3	83	17
19	24	1	28	4	47	4	2	92	21
20	28	1	29	4	48	25	1	93	21
21	1	1	30	4	49	25	2	94	21
22	27	3	31	4	50	26	1	95	21
23	26	2	32	4	51	6	1	96	22
24	7	3	48	8	52	0	1	97	22
25	22	1	49	8	53	13	1	98	22
26	28	1	50	8	54	14	1	99	22
27	27	1	51	8	55	29	1	100	22
28	26	2	52	8					

Table 11 Data for product D

Sequence	Machine group	Recipe	Stage	Layer	Sequence	Machine group	Recipe	Stage	Layer
1	31	1	0	0	28	7	1	53	9
2	24	1	1	0	29	23	1	54	9
3	20	1	2	0	30	26	1	55	9
4	26	1	3	0	31	17	1	56	10
5	9	1	4	1	32	34	1	57	10
6	17	1	5	1	33	10	1	58	10
7	21	1	6	1	34	23	3	59	10
8	38	1	7	1	35	26	1	60	10
9	17	1	8	1	36	16	1	74	15
10	37	1	9	1	37	26	4	75	15
11	24	1	10	1	38	16	1	76	16
12	20	1	11	1	39	2	1	77	16
13	26	2	12	1	40	11	1	78	16
14	9	1	13	2	41	26	2	79	16
15	26	1	14	2	42	5	1	80	17
16	17	1	33	5	43	11	3	81	17
17	21	2	34	5	44	33	1	82	17
18	38	1	35	5	45	26	3	83	17
19	24	1	36	5	46	4	2	96	21
20	26	1	37	5	47	25	1	97	21
21	17	1	41	7	48	25	2	98	21
22	17	1	42	7	49	26	1	99	21
23	22	1	43	7	50	6	1	100	22
24	28	1	44	7	51	0	1	101	22
25	1	1	45	7	52	14	1	102	22
26	27	1	46	7	53	13	1	103	22
27	26	2	47	7	54	29	1	104	22

Table 12 Data for product E

Sequence	Machine group	Recipe	Stage	Layer	Sequence	Machine group	Recipe	Stage	Layer
1	31	1	0	0	27	23	1	54	9
2	24	1	1	0	28	26	1	55	9
3	20	1	2	0	29	17	1	56	10
4	26	1	3	0	30	34	1	57	10
5	9	1	4	1	31	10	1	58	10
6	17	1	5	1	32	23	3	59	10
7	21	1	6	1	33	26	1	60	10
8	38	1	7	1	34	16	1	74	15
9	17	1	8	1	35	26	4	75	15
10	37	1	9	1	36	16	1	76	16
11	24	1	10	1	37	2	1	77	16
12	20	1	11	1	38	11	1	78	16
13	26	2	12	1	39	26	2	79	16
14	9	1	13	2	40	5	1	80	17
15	26	1	14	2	41	11	3	81	17
16	17	1	15	3	42	33	1	82	17
17	21	2	16	3	43	26	3	83	17
18	38	1	17	3	44	4	2	96	21
19	24	1	18	3	45	25	1	97	21
20	17	1	19	3	46	25	2	98	21
21	22	1	20	3	47	26	1	99	21
22	28	1	21	3	48	6	1	100	22
23	1	1	22	3	49	0	1	101	22
24	27	1	23	3	50	14	1	102	22
25	26	2	24	3	51	13	1	103	22
26	7	1	53	9	52	29	1	104	22

Table 13 Data for product F

Sequence	Machine group	Recipe	Stage	Layer	Sequence	Machine group	Recipe	Stage	Layer
1	31	1	0	0	26	7	1	53	9
2	24	1	1	0	27	23	1	54	9
3	20	1	2	0	28	26	1	55	9
4	26	1	3	0	29	17	1	56	10
5	9	1	4	1	30	34	1	57	10
6	17	1	5	1	31	10	1	58	10
7	21	1	6	1	32	23	3	59	10
8	38	1	7	1	33	26	1	60	10
9	17	1	8	1	34	16	1	76	16
10	37	1	9	1	35	2	1	77	16
11	24	1	10	1	36	11	1	78	16
12	20	1	11	1	37	26	2	79	16
13	26	2	12	1	38	16	1	89	19
14	9	1	13	2	39	11	1	90	19
15	26	1	14	2	40	33	1	91	19
16	17	1	15	3	41	26	3	92	19
17	21	2	16	3	42	4	2	96	21
18	38	1	17	3	43	25	1	97	21
19	24	1	18	3	44	25	2	98	21
20	17	1	19	3	45	26	1	99	21
21	22	1	20	3	46	6	1	100	22
22	28	1	21	3	47	0	1	101	22
23	1	1	22	3	48	14	1	102	22
24	27	1	23	3	49	13	1	103	22
25	26	2	24	3	50	29	1	104	22

Table 14 Manufacturing data of C\D wafers

Sequence	Machine group	Recipe	Stage	PUR process	Mean processing time (min)	Consumption (pieces of wafers)
C\D 1						
1	27	1	23	Preparation	344	
2	31	1	0	In-use	210	6
3	25	1	97	Recycling	84	
C\D 2						
1	34	1	62	Preparation	394	
2	28	1	63	Preparation	343	
3	9	3	4	In-use	48	1
4	14	1	102	Recycling	55	
C\D 3						
1	22	1	49	Preparation	459	
2	28	1	50	Preparation	343	
3	26	1	55	Preparation	50	
4	7	1	38	In-use	84	4
5	16	2	61	Recycling	156	
C\D 4						
1	11	1	78	Preparation	318	
2	10	1	58	In-use	55	6
3	15	1	87	Recycling	86	
C\D 5						
1	27	3	31	Preparation	343	
2	5	1	80	In-use	86	3
3	38	1	7	Recycling	28	

References

1. Foster B, Meyersdorf D, Padillo J M, Brenner R (1998) Simulation of test wafer consumption in a semiconductor facility. Proceedings IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp 298–302
2. Popovich SB, Chilton SR, Kilgore B (1997) Implementation of a test wafer inventory tracking system to increase efficiency in monitor wafer usage. Proceedings IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp 440–443
3. Chu YF (1998) The inventory management model for control and dummy wafers. Master Thesis, National Chiao Tung University, Hsin-Chu, Taiwan
4. UTEK Semiconductor Corp. (1998) Operation Procedure of UTEK Semiconductor Corporation, UTEK, Taiwan
5. Wang MH (1999) The determination of inventory levels of control wafers in wafer fabrication. Master Thesis, National Chiao Tung University, Hsin-Chu, Taiwan
6. Wu CY (1998) The construction of dispatching procedure for control wafers in diffusion area. Master Thesis, National Chiao Tung University, Hsin-Chu, Taiwan

7. Tersine Richard J (1994) Principles of inventory and materials management, 4th edn. Prentice Hall, MA
8. Waters CDJ (1990) Inventory control and management. Wiley
9. Wilson Robin J, Watkins John J (1990) Graphs: an introductory approach. Wiley, New York
10. Evans James R, Minieka Edward (1992) Optimization algorithms for networks and graphs. Marcel Dekker
11. Phillips Don T, Garcia-Diaz Alberto (1981) Fundamentals of network analysis. Prentice-Hall, MA
12. Syslo Maciej M, Deo Narsingh, Kowalik Janusz S (1983) Discrete optimization algorithms with pascal programs. Prentice-Hall, MA
13. Chen HC (2000) Control and dummy wafers management. Proposal of Ph. D. Thesis, National Chiao Tung University, Hsin-Chu, Taiwan