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H_2 and NH_3 Plasma Passivation on Poly-Si TFTs with Bottom-Sub-Gate Induced Electrical Junctions

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The effects of NH_3 and H_2 plasma passivation on the characteristics of poly-Si thin-film transistors (TFTs) with source/drain extensions induced by a bottom sub-gate were studied. Our results show that although significant improvements in device performance can be obtained by either passivation method, the NH_3-plasma-treatment appears to be more effective in reducing the off-state leakage, subthreshold swing, and in improving mobility compared to H_2 plasma passivation. Furthermore, NH_3 plasma treatment is also found to be more effective in reducing the anomalous subthreshold hump phenomenon observed in nonplasma-treated short-channel devices. Detailed analysis suggests that all these improvements can be explained by the more effective passivation of traps distributed in both the front and back sides of the channel by NH_3 plasma treatment.
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Recently, polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have received lots of attention as replacements for amorphous silicon TFTs in the switching elements of high-performance large-area active-matrix display and sensor systems. With their higher mobility, the peripheral driver circuitry can be integrated on the same substrate, which further improves system performance and reliability.[1,2] However, defects at the grain boundaries as well as inside the grains are known to cause device degradation,[3] resulting in poor device performance including low mobility and high off-state leakage current.[4,5] In order to obtain high-performance poly-Si TFTs, it is essential to reduce the trap density in the poly-Si channel. To this end, hydrogen plasma passivation is a well-known technique.[6,7] The atomic hydrogen can passivate defects in the poly-Si channel, thereby improving device characteristics. In addition, nitrogen-containing plasma treatments in combination with hydrogen (*e.g.*, H_2/N_2 mixture plasma,[8] nitrogen implantation with H_2 plasma,[9] preoxidation NH_3 annealing with H_2 plasma,[10] and NH_3 plasma[11]) have also been shown to further improve the device performance. The additional nitrogen passivation and/or the enhanced hydrogen passivation effects in the presence of nitrogen are presumably responsible for the observed improved characteristics.

Another approach for reducing the off-state leakage current is to use an electrical drain junction that is induced by a sub-gate.[12,13] It has been shown that with proper device structure design and operation conditions, the leakage current can be dramatically reduced without significantly compromising the drive current. Conventionally,[12] a top sub-gate configuration is used. Recently, we have proposed a novel TFT device with bottom sub-gate configuration.[13,14] In previous work we have explored and characterized the fabricated devices and shown that high device performance could be achieved using this structure. In this work, we further explore and compare the effects of plasma treatments in NH_3 or H_2 ambient on device characteristics.

Experimental

Figure 1 shows the cross-sectional and top views of the poly-Si TFT used in this experiment. The fabricated devices feature a top main gate and a fork-shaped bottom sub-gate. The fork-shaped sub-gate has two split branches buried under the poly-Si active layer used for electrically inducing the source and drain extensions. The device's channel length, L, is thus defined by the spacing between the two branches of the sub-gate. The length of the offset channel regions between the implanted source/drain and the main gate is fixed at 1 μm in this study.

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The key process flow for fabricating the poly-Si TFTs with bottom sub-gate was described in detail in our previous work.[13,14] Briefly, a 100 nm n^+-poly-Si layer was deposited on an oxidized silicon substrate by low-pressure chemical vapor deposition (LPCVD). The doped poly-Si film was then patterned to form the fork-shaped bottom sub-gate. Next, a 100 nm nitride layer was deposited by chemical vapor deposition (CVD), followed by the deposition of a thick low-pressure tetraethyl orthosilicate (550 nm) oxide layer. Chemical mechanical polishing (CMP) was then applied to planarize the wafer surface and to expose the nitride layer on top of the sub-gate. It is worthy to note that the nitride layer serves not only as the dielectric separation between the field-plate (*i.e.*, sub-gate) and the active device layer in the final device structure, it also

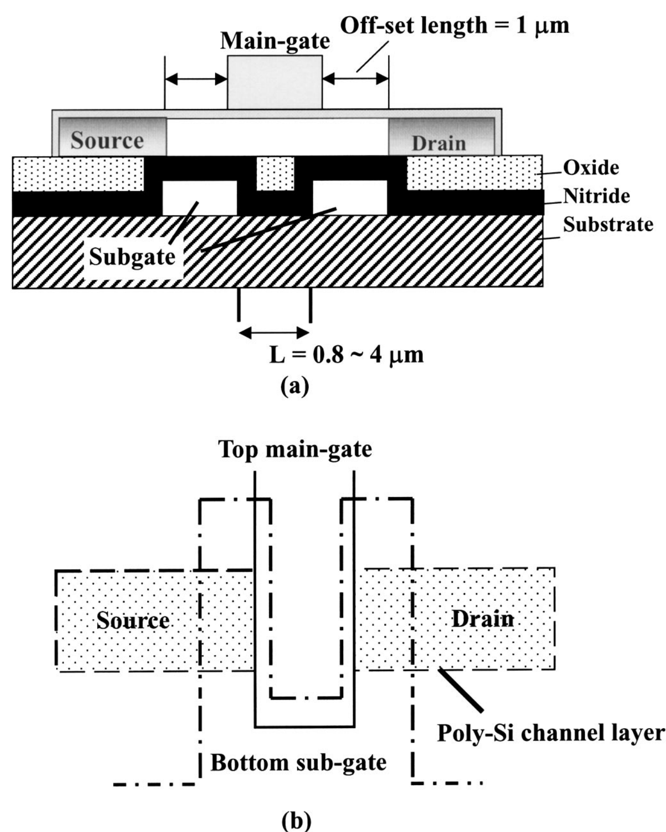

Figure 1. (a) Cross-sectional and (b) top views of a TFT device with bottom sub-gate.

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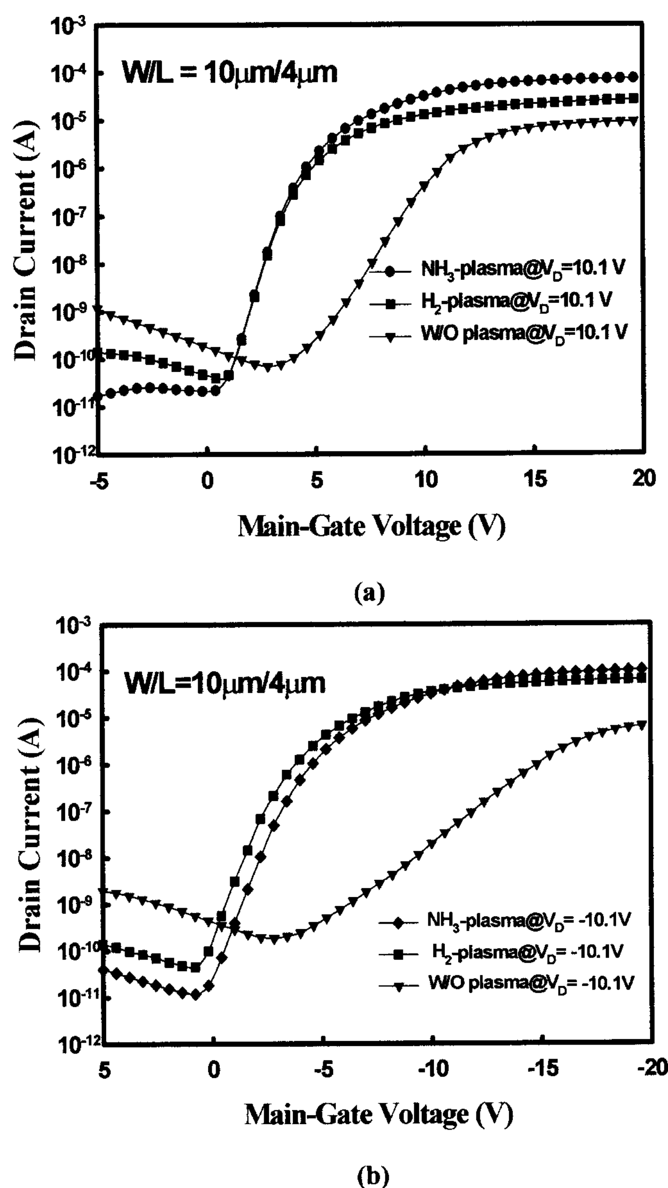

Figure 2. Subthreshold (I_D-V_G) characteristics of (a) n-channel and (b) p-channel TFTs with different plasma treatments. The sub-gate biases of nTFT and pTFT are 40 and −40 V, respectively.

serves as an etch stopper for the CMP process. Afterward, a 50 nm CVD amorphous Si film was deposited at 550°C, which was subsequently converted to polycrystalline phase by solid-phase crystallization (SPC) at 600°C for 24 h, to serve as the active device layer. A 20 nm CVD oxide layer was then deposited to form the gate insulator. An n^+ poly-Si film was deposited and patterned to form the top main-gate. Next, the offset source/drain regions were defined by a photoresist masking step before performing the source/drain ion implantation. For n-channel transistors, As^+ implant with a dosage of 5×10^{15} cm^{-2} at 20 keV was used. Similarly, BF_2^+ implant with a dosage of 5×10^{15} cm^{-2} at 30 keV was used for p-channel transistors. The implanted dopants were subsequently activated in N_2 ambient at 600°C for 12 h. Wafers then followed a standard back-end processing for contact pad formation and metallization. Finally, some devices were split to receive NH_3 or H_2 plasma treatment in a parallel-plate plasma reactor at 250°C for 3 h.

Results and Discussion

Characteristics of long-channel devices.—Figure 2 compares the subthreshold characteristics of devices with and without plasma treatment. The channel length and width of the devices are 4 and 10 μm, respectively. Note that a fixed sub-gate bias of 40 V was chosen in this work because it is large enough for the device performance improvement, while small enough not to degrade the reliability of the dielectric underneath the sub-gate. Tables I and II summarize several important parameters, including subthreshold swing S, threshold voltage V_{th}, trap-state density N_t, off-state leakage current I_{off}, and on/off current ratio, extracted from the results shown in Fig. 2. The threshold voltage is defined at a fixed drain current $I_D = I_{DN} \times W/L$,[15] where I_{DN} is 10 nA. Extraction of trap-state densities is performed using the modified Levinson's method.[16,17] From these results, it can be seen that significant improvements are achieved for both n- and p-channel devices treated by either H_2 or NH_3 plasma, though in the latter case the improvements are much larger. This is further highlighted in Fig. 3 in which the I_D-V_D characteristics of n- and p-channel TFTs are shown (nTFT and pTFT, respectively). Clearly, NH_3-plasma-treated samples show better performance, especially for n-channel devices.

Dependence of channel length.—The effects of channel length on device performance for n- and p-channel devices are shown in Fig. 4 and 5, respectively. From these results, two basic leakage components are identified: (*i*) the off-state leakage current that increases with increasing voltage difference between the gate and drain (V_{GD}) as $L < 2$ μm, and (*ii*) the "hump" that appears in the subthreshold regionas $L < 1.5$ μm. The former component is well characterized in the literature and could be ascribed to the trap-assisted thermionic emission[5] or field emission[18] conduction process. Such leakage process is closely related to the amount of trap density in the channel. Note that due to the bottom sub-gate configuration in the devices, the flow path for such leakage component is from the surface channel to the bottom extension drain junction, as schematically shown in Fig. 6 (path 1). To highlight the importance of the sub-gate bias on this type of leakage, Fig. 7 depicts the off-state leakage for both p- and n-channel devices treated with NH_3 plasma as a function of the sub-gate bias. In the measurements, the main-gate voltages are fixed at −5 and 5 V for n- and p-channel operations, respectively. It can be seen that the leakage is roughly constant in the low-sub-gate bias region, and starts to rise when the

Table I. The values of SS, V_{th}, N_t, I_{off}, and on/off current ratio of the n-channel polysilicon TFTs for various plasma treatments.

Plasma gas	Subthreshold swing (V/dec)	V_{th} (V)	N_t ($\times 10^{11}$ cm^{-2})	I_{off} (A) V_D = 10.1 V	I_{on}/I_{off} V_D = 10.1 V
No plasma treatment	1.62	13	22.1	3.78×10^{-11}	1.1×10^5
H_2-plasma treatment	0.72	4	9.59	3.77×10^{-11}	7.1×10^5
NH_3-plasma treatment	0.64	3.4	7.63	1.7×10^{-11}	4.4×10^6

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Table II. The values of SS, V_{th}, N_t, I_{off}, and on/off current ratio of the p-channel polysilicon TFTs for various plasma treatments.

Plasma gas	Subthreshold swing (V/dec)	V_{th} (V)	N_t ($\times 10^{11}$ cm^{-2})	I_{off} (A) $V_D = -10.1$ V	I_{on}/I_{off} $V_D = -10.1$ V
No plasma treatment	3.35	−11.2	19.2	1.84×10^{-10}	3.5×10^4
H_2-plasma treatment	0.75	−5	8.28	4.28×10^{-11}	1.5×10^6
NH_3-plasma treatment	0.71	−3.4	7.03	1.17×10^{-11}	8.8×10^6

sub-gate voltage exceeds a threshold, *e.g.*, around 15 V for nTFT and −20 V for pTFT, corresponding to the formation of electrical drain extension in the offset region.

At a fixed channel length, the leakage for H_2-plasma-treated devices is higher than the NH_3-plasma-treated ones, as can be seen in Fig. 4 and 5. This again indicates that NH_3 plasma is more effective in passivating the defects in the poly-Si channel. This is further confirmed with the results shown in Fig. 8, in which the extracted effective trap-state density (N_t) using the modified Levinson's method[17] is plotted as a function of channel length. Note that these results are for the unpassivated defects located at or near the front-side interface in which an inversion layer formation is taking place. It is observed that the N_t values for NH_3-plasma-treated devices are lower than H_2-plasma-treated counterparts. Moreover, there is a re-

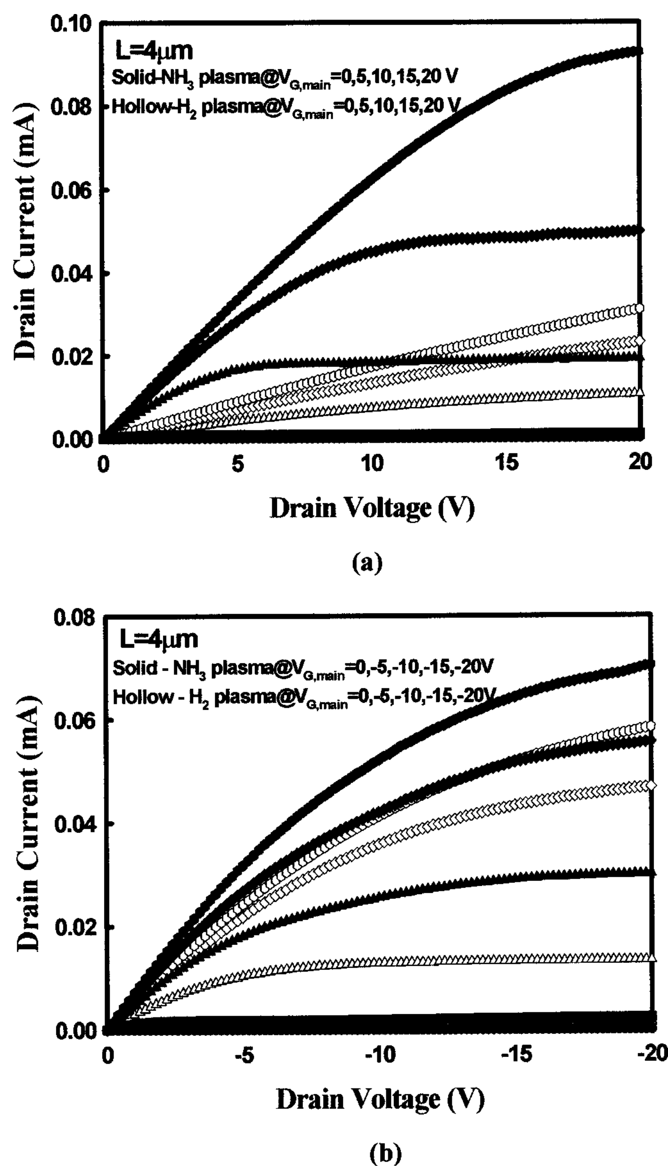

Figure 3. Output (I_D-V_D) characteristics of (a) n-channel and (b) p-channel TFTs with different plasma treatments. The sub-gate biases of nTFT and pTFT are 40 and −40 V, respectively.

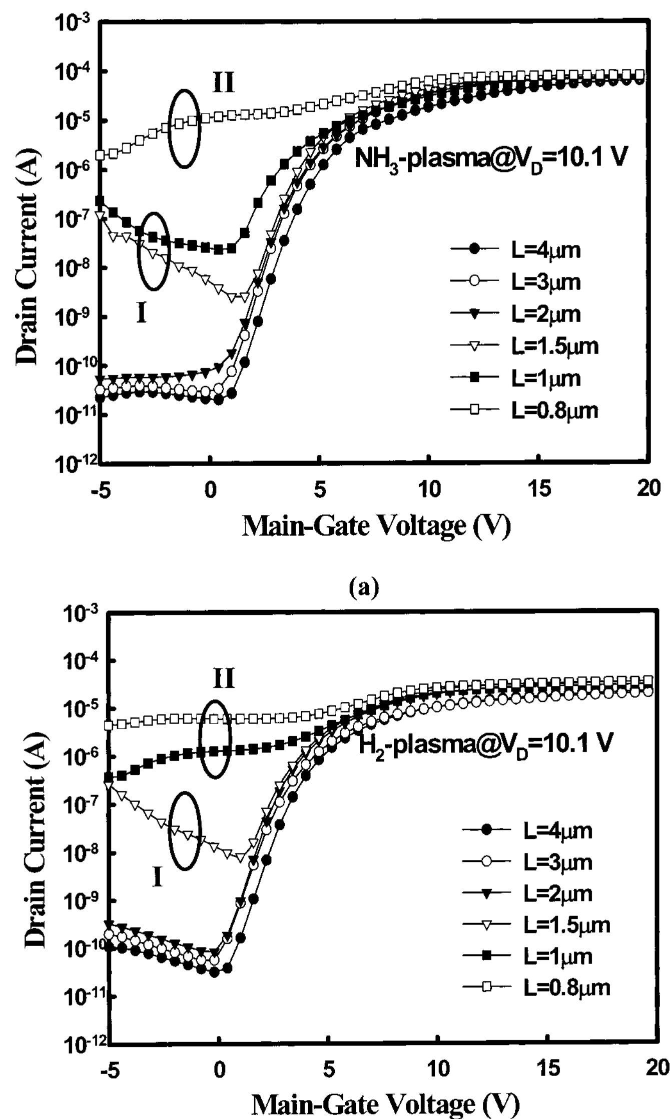

Figure 4. Subthreshold characteristics of n-channel TFT devices with various channel lengths at $V_D = 10.1$ V after (a) NH_3 plasma treatment and (b) H_2 plasma treatment. The sub-gate bias is 40 V.

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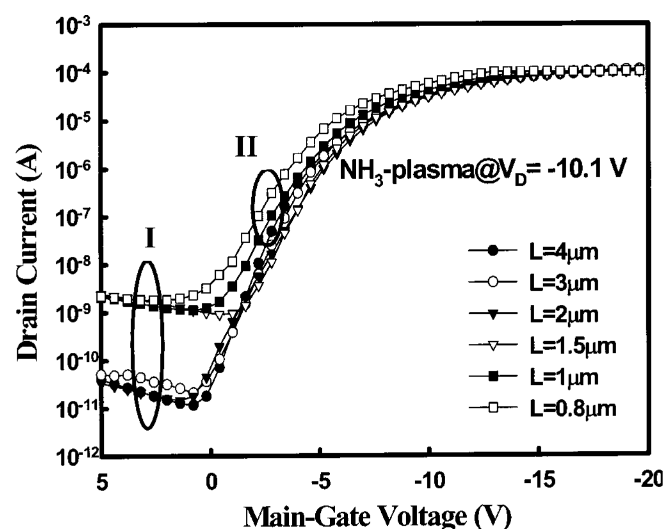


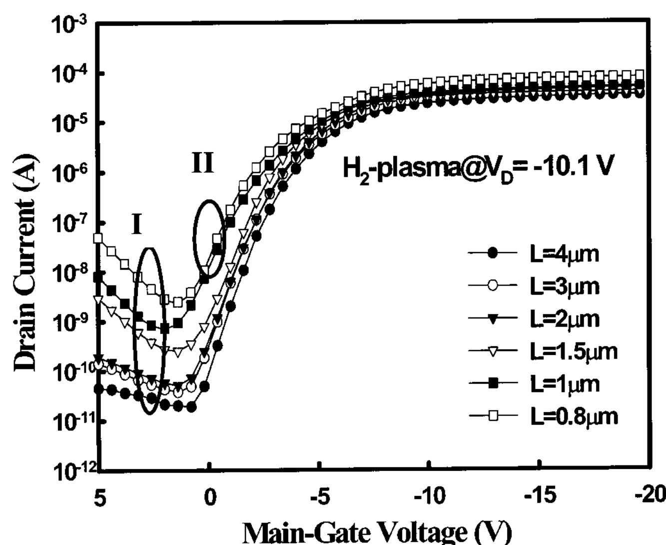


Figure 5. Subthreshold characteristics of p-channel TFT devices with various channel lengths at $V_D = -10.1$ V after (a) NH_3 plasma treatment and (b) H_2 plasma treatment. The sub-gate bias is -40 V.

duction in N_t for devices having a shorter channel. This trend is reasonable because the passivation of defects in the channel is related to the diffusion of passivating species from the edge of the channel. Devices with a shorter length may have more defects passivated in the middle of the channel simply because of a shorter diffusion path.[19] Nevertheless, the off-state leakage becomes significant as $L < 2$ μm because of the dramatic increase in field strength.

The appearance of a hump in the subthreshold region as $L < 1.5$ μm has been reported in our previous report.[14] The leakage path is believed to flow through the back-side surface of the channel layer, as illustrated in Fig. 6 (path 2). Some defects near the bottom interface generated during some processing steps (*e.g.*, CMP) are believed to be responsible for such leakage. Such phenomenon also leads to the anomalous current increase in the output characteristics of short-channel devices, as shown in Fig. 9. By comparing the device characteristics, the hump is less pronounced in NH_3-plasma-treated samples, implying that the NH_3 plasma is also more effective in reducing the active defect density along the back-side surface of the channel layer.

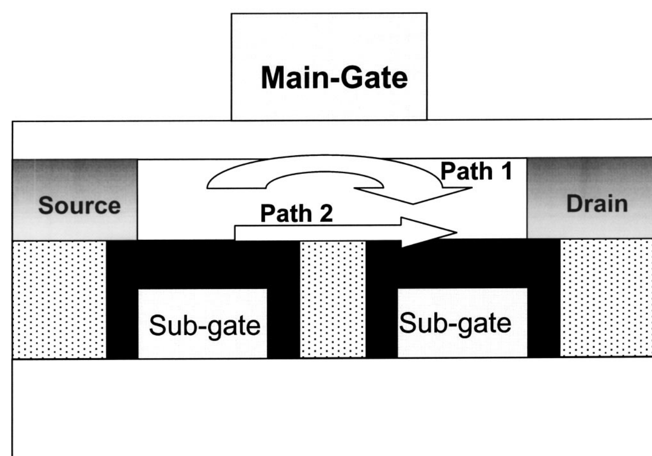
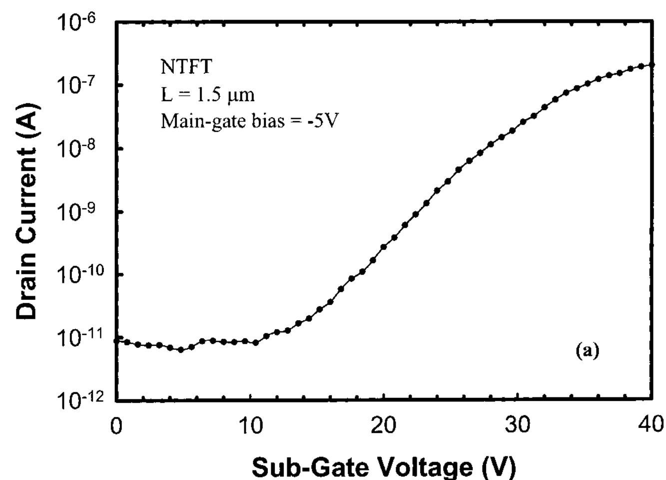


Figure 6. Illustration of the leakage path along the top (path 1) and bottom (path 2) interfaces of the poly-Si active layer.

From these observations, it is clear that NH_3 plasma is more effective in passivating trap state and improving device characteristics. This may be due to the appearance of nitrogen species in the NH_3 plasma that may also help passivate the defects. According to a previous report,[11] the use of NH_3 plasma treatment would result in the nitrogen pileup at the SiO_2/poly-Si interface and the formation



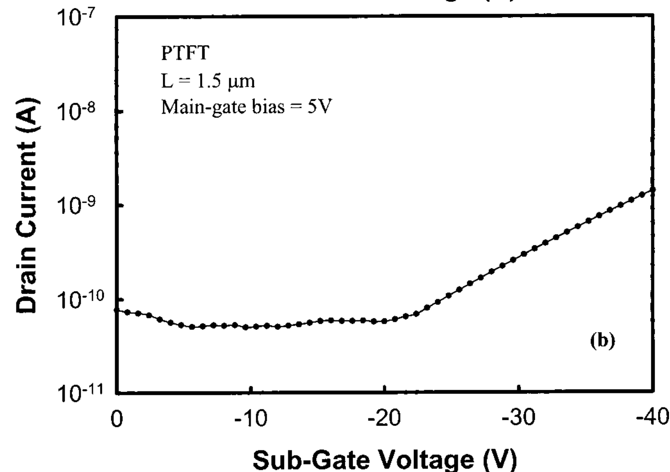


Figure 7. Off-state drain current as a function of sub-gate bias for (a) n- and (b) p-channel TFTs with NH_3-plasma treatment.

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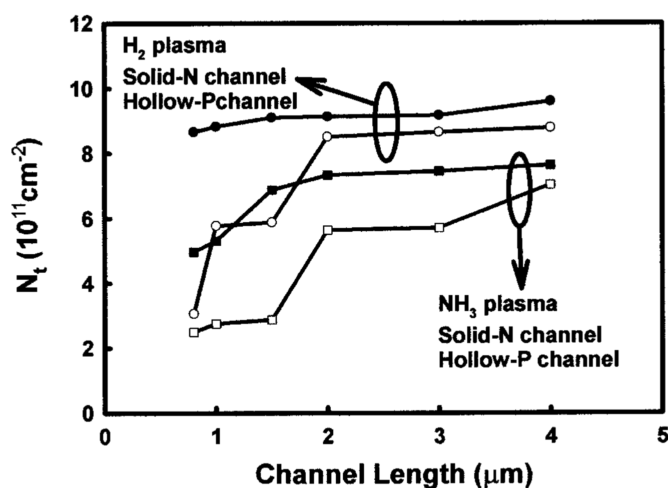
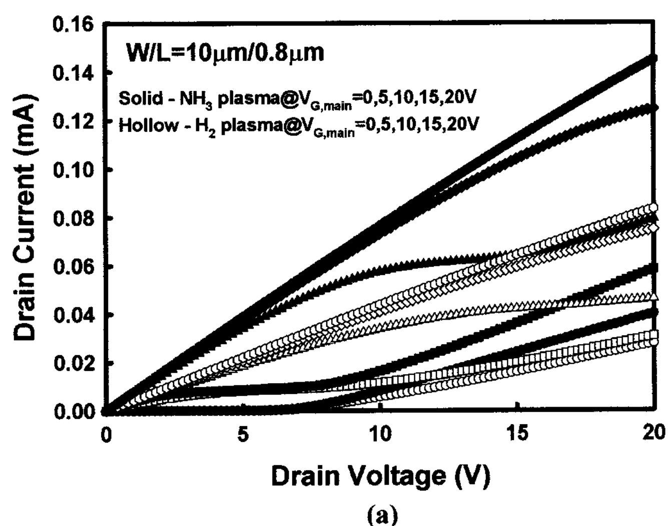


Figure 8. Trap-state density *vs.* gate length for n- and p-channel TFTs with H_2- and NH_3-plasma treatments.



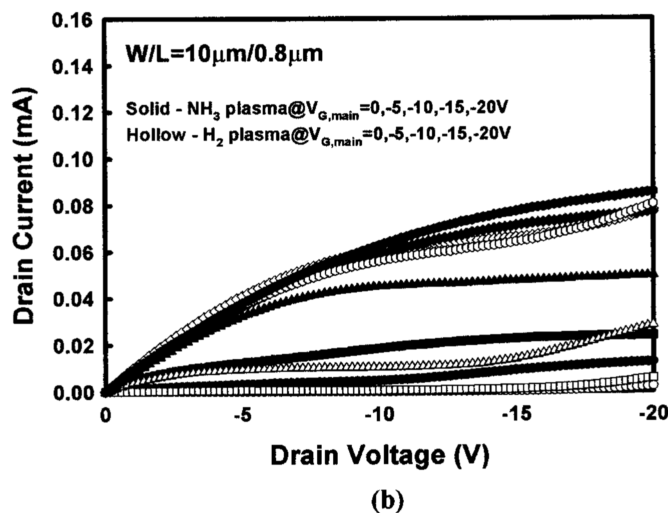
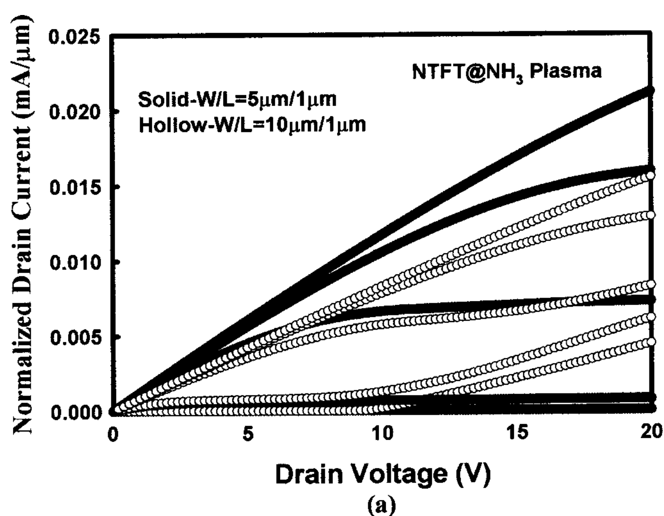


Figure 9. Comparison of output characteristics for H_2- and NH_3-plasma passivated (a) n-channel and (b) p-channel devices with $L = 0.8\ \mu m$. The sub-gate biases of nTFT and pTFT are 40 and −40 V, respectively.



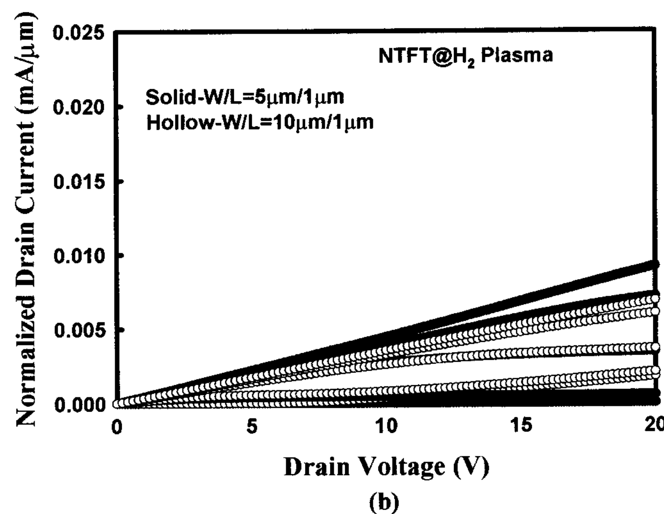


Figure 10. Output characteristics of nTFT devices with various channel widths after (a) NH_3 and (b) H_2 plasma treatment. The sub-gate bias is 40 V.

of strong Si-N bonds, which tends to terminate the dangling bonds in the grains and at the grain boundaries in the poly-Si channel. In our case, these events could occur at or near both top and bottom interfaces, and thus result in the reduction of off-state leakage.

Dependence of channel width.—In order to understand the cause of hump phenomenon in more detail, transistors having same channel length (1 μm) but different channel width were characterized and compared. The effects of channel width on device output characteristics for n- and p-channel devices are shown in Fig. 10 and 11, respectively. Note that the current has been normalized to the channel width. In these figures we can see that significant increase in output current could be realized as channel width is reduced. Meanwhile, the aforementioned anomalous phenomenon in current-voltage characteristics becomes less pronounced and eventually disappears as channel width is reduced. The improvement in device performance could be correlated with the diffusion path of the passivation species, as schematically shown in Fig. 12. To more clearly illustrate the situation, the top gate is deliberately not shown in the figure. Because the passivation species enter the device region from the edges of the channel, defect passivation takes place initially at the edges of the channel and then gradually extends to the central region away from the channel edges. For devices with a wider channel, the defects located at the central region may remain unpassivated after the plasma treatment. The unpassivated defects at the bottom central channel interface are believed to be responsible for

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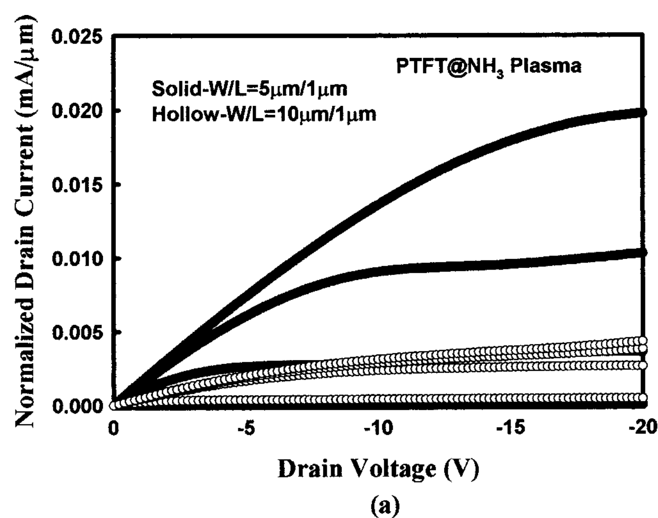

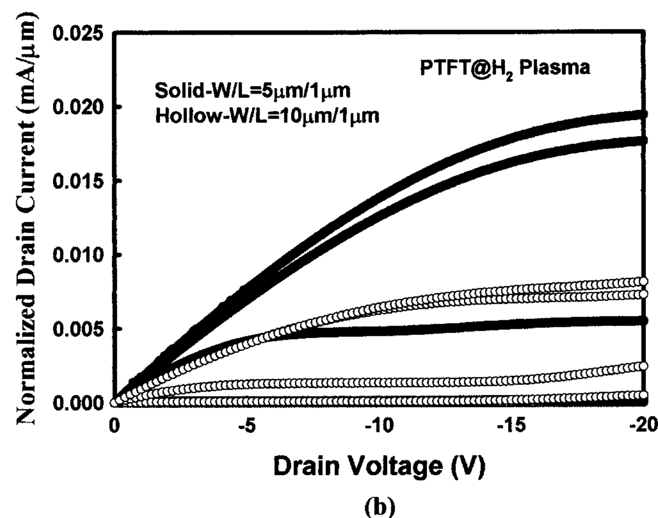

Figure 11. Output characteristics of pTFT devices with various channel widths after (a) NH_3 and (b) H_2 plasma treatment. The sub-gate bias is -40 V.

the hump phenomenon observed in short-channel devices. When the width is narrow enough (*e.g.*, $\leqslant 5\ \mu m$), the passivation process is complete (*i.e.*, even the central channel region has become fully passivated) after the plasma treatment, so the leakage could be effectively suppressed.

Conclusions

In this work, TFT devices with electrical source/drain extensions induced by a bottom sub-gate after treatment in H_2 or NH_3 plasma were characterized. NH_3 plasma was found to be more effective than H_2 plasma for passivating defects in the poly-Si channel, thus resulting in lower off-state current, steeper subthreshold slope, and lower threshold voltage. The hump phenomenon observed in short-channel TFTs indicates the existence of an additional leakage path formed on the bottom interface of the channel layer. Our results indicate that NH_3 plasma passivation is also more effective in suppressing such phenomenon. Moreover, the effects of channel width on the characteristics of both n- and p-type hydrogenated devices were investigated. It is shown that the hump in current-voltage characteristics could be effectively suppressed for devices with narrow channel width.

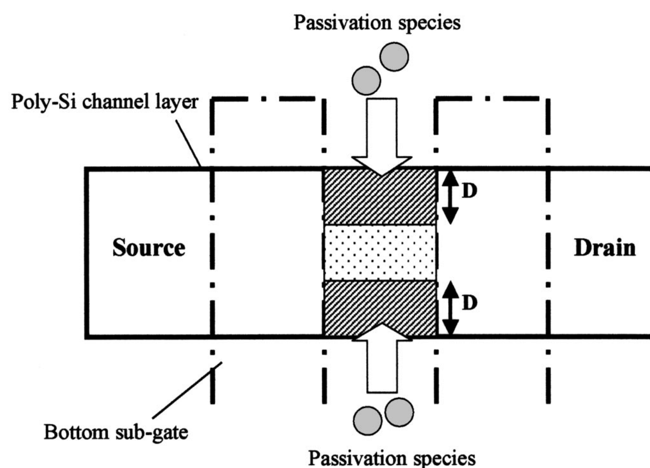

Figure 12. Illustration of the diffusion process for passivation species during plasma treatment.

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