A 0.5 V 4.85 Mbps Dual-Mode Baseband Transceiver With Extended Frequency Calibration for Biotelemetry Applications

Tsan-Wen Chen, *Student Member, IEEE*, Jui-Yuan Yu, Chien-Ying Yu, and Chen-Yi Lee, *Member, IEEE*

***Abstract*—This work provides a dual-mode baseband transceiver chipset for wireless body area network (WBAN) system. The modulation schemes include multi-tone code division multiple access (MT-CDMA) and orthogonal frequency division multiplexing (OFDM) to meet multi-user coexistence (up to 8) and high data rate purposes. Based on the analysis of the WBAN operation behavior, several methods including higher data rate, optimal storage determination, and low power implementation techniques are proposed to reduce the transmission energy. To achieve tiny area integration, an embedded phase frequency tunable clock generator and frequency error pre-calibration scheme are provided to extend the frequency mismatch tolerance to 100 ppm (2.5x of state-of-the-art systems). This chipset is manufactured in 90 nm standard CMOS process. Working at supply voltage of 0.5 V, this chipset is able to provide maximum date rate of 4.85 Mbps with modulator power consumption of 5.52 μW.**

***Index Terms*—Baseband, power domain, power gating, WBAN, voltage scaling.**

I. Introduction

UBIQUITOUS healthcare extends medical services from the closed in-hospital systems to any open roaming spaces. Wireless body area network (WBAN) is an emerging technology which is specifically designed for body signal collection and monitoring to provide reliable physical information. A typical WBAN consists of a multiple of wireless sensor nodes (WSNs) and a central processing node (CPN) as shown in Fig. 1(a). These WSNs are capable of sensing and filtering the body signals, storing the information, and transmitting the data wirelessly to a CPN for further processing and other applications. In order to achieve long duration monitoring for biotelemetry applications, the WBAN system, especially the WSN, is required to provide reliable signal transmission, ultra-low power operation, and highly integrated tiny area for comfortable purposes.

There are several candidate systems for WBAN, such as Bluetooth and ZigBee [2], [3] which have been developed and already integrated in lots of portable devices. However, both of them are designed for widespread applications such as entertainments, sports, and surveillance. The power consumption cannot satisfy the requirements for continuous healthcare monitoring applications which often demand more than 24 hours (even several days) or longer. Therefore, another specific design for low power solution is necessary for biotelemetry applications.

State-of-the-art platforms [4], [5] achieve highly integrated SoC designs with mature FSK wireless scheme. Alternative RF front-end designs [6]–[8] focus on a pulse-based radio ultra wideband (UWB) transmission. All of these approaches provide low data rate transmission with simple modulation to achieve low power target. In order to achieve low power purpose, however, all of these solutions only provide the point-to-point transceiver design without considering the interference from other users in WBAN. In fact, low-data-rate transmission requires longer active duration, dissipating higher overall energy. Besides, the simple modulation also suffers network difficulties from multi-user (or sensor network) environments, and it has no flexibilities to enhance data transmission quality.

This work, considering the WBAN behavior, provides the transmission energy analysis and power reduction strategies. The baseband modulations include MT-CDMA [1] and OFDM for both reliable transmission in multi-user (or sensor network) environment and high data rate requirements. The energy analysis also shows that the power of the storage unit (SU) is related to the transmission power. The methods to determine the storage type and the size are also discussed to minimize transmission energy. In order to extend the battery life, the supply voltage is scaled to 0.5 V to reduce the power consumption of the transceiver and its storage circuits. The leakage power is further reduced with power gating scheme [1] when the system is idle. Therefore, the proposed design provides both reliable data transmission and power reduction from the system operation level point of view.

Considering the tiny area integration in WSN, the bottleneck is a quartz crystal that provides a stable clock signal to the whole device, but it cannot be integrated with standard CMOS designs due to heterogeneous manufacturing process. As a result, a pre-calibration scheme is proposed to extend the baseband frequency tolerance such that a less accurate clock source is allowed. This enables a CMOS clock source that is implemented in standard CMOS [9], [10] to be integrated in a WSN, instead of an external crystal, resulting in a tiny area system integration.

This paper is organized as follows. In Section II, an introduction for the proposed WBAN system operation is given. Based on the system operation model, a power reduction strategy is

Manuscript received February 06, 2009; revised April 24, 2009. Current version published October 23, 2009. This paper was approved by Guest Editors Hoi-Jun Yoo and SeongHwan Cho. This work was supported by MOEA of Taiwan under Grant 97-EC-17-A-03-S1-0005. The original work was supported by NSC and MOE ATU programs.

The authors are with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 30010, Taiwan (e-mail: goodidea@si2lab.org; jyyu@si2lab.org; cyyu@si2lab.org; cylee@si2lab.org).

Digital Object Identifier 10.1109/JSSC.2009.2028940

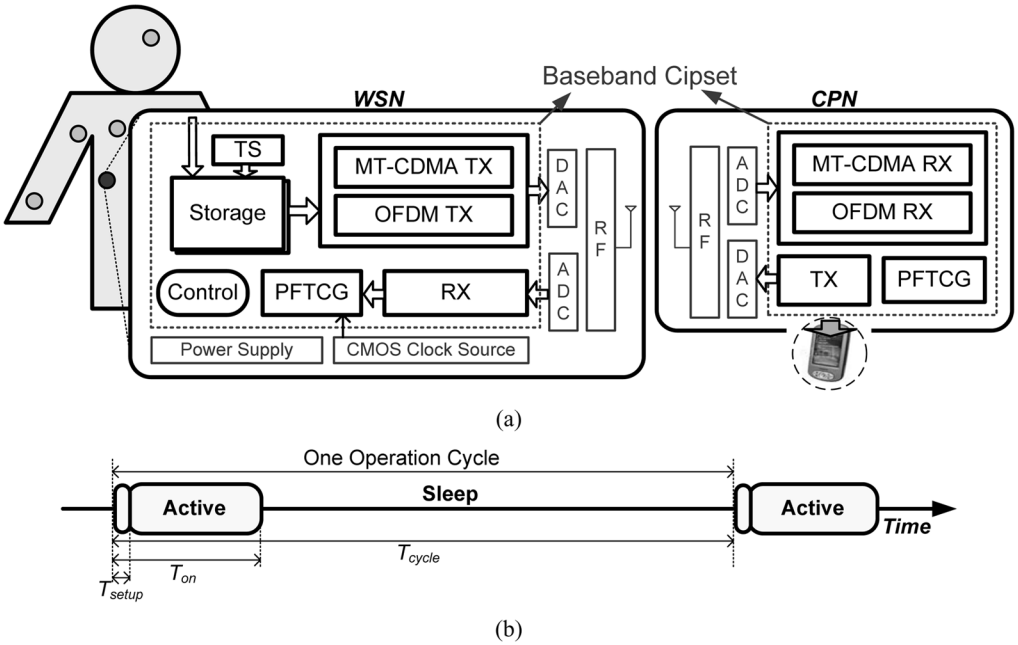

Fig. 1. Block diagram of WBAN system (a) and behavior time line (b).

discussed in Section III, including storage space determination. In order to include an embedded CMOS clock source for tiny area integration, Section IV presents the proposed pre-calibration scheme. Section V describes the low power chipset circuits design and implementation details. Then the simulation and experimental results are presented in Section VI followed by the conclusion in Section VII.

II. Proposed WBAN System Operation

The WBAN system block diagram is shown in Fig. 1(a), including a WSN and a CPN that are attached on human body skin and integrated in a portable device, respectively. The proposed baseband transceiver chipset contains a temperature sensor (TS), modulator, demodulator, phase and frequency tunable clock generator, and the SU.

In the WSN, the body signal from the integrated temperature sensor or other external readout sensors are accumulated in the SU. The clocking speed and bit-length resolution of a SU that connects to a readout sensor is based on the specification of an electrocardiogram (ECG) signal that requires almost the highest sampling rate and longest bit-length to represent its waveform among a human body. An analog to digital converter (ADC) with 610 Hz sampling rate and 16-bit resolution is used to sample body signals in this work (9.76 kbps throughput from sensor). When the SU is full, either of OFDM or MT-CDMA modulation scheme can be used to transmit data.

These dual-mode modulation parameters are summarized in Table I. The OFDM mode provides high data rate that can improve the transmission power efficiency according to a shorter active duration. Besides, OFDM mode can be applied to extend applications which require Mbps-level data rate such as video data transmission (endoscope capsule). However, OFDM only can be used in point-to-point transmission. The MT-CDMA modulation enables more than a single WSN operating at the same time in the sensor network [1]. With the same required SNR as OFDM mode to achieve the target transmission quality (11.2 dB for frame error rate $(\mathrm{FER}) = 1\%$ in AWGN channel), MT-CDMA provides the multiple access feature according to the coding diversity, however, the data rate is limited due to the overhead of spreading codes. This work provides dual-mode modulation that allows user to switch due to user numbers in the network and operation requirements for reliable and low power wireless transmission.

TABLE I
Dual-Mode Modulation Parameters

Modulation	OFDM	MT-CDMA
Signal bandwidth	5MHz	5MHz
FFT Size	64	16
Mapping	QPSK	QPSK
Conjugate symmetric	Yes	Yes
GI length	1/32 OFDM symbol	1/8 OFDM symbol
Spreading code length	N/A	31
Data rate	4.85Mbps	143kbps

The network information such as user numbers and the distance among users in the network are assumed to be detected in CPN by other wide range network services in the portable device. Then the modulator in the CPN broadcasts the down-link preamble to all WSNs for both network information transmission and synchronization before the up-link operation. Since no coexistence issue exists during the broadcast, the OFDM modulation is used for down-link transmission.

The proposed system operates in 1397.5 MHz radio band and occupies 5 MHz bandwidth. Instead of an external crystal, the clock source in WSN is provided by a CMOS clock source for tiny area integration purpose. Due to less accurate frequency provided by CMOS clock source, a digital signal processing (DSP) calibration method in the transmitter block and a phase

frequency tunable clock generator (PFTCG) design are also integrated in the WSN. From the down-link transmission, the receiver in the WSNs can get the mismatch information, and WSN can adjust the PFTCG and transmission block before data transmission for better system performance.

III. Power Reduction Strategy and Analysis

A. Transmission Energy Analysis

Comparing to the sensor sampling speed, the baseband processing rate is much higher, so the WSN takes much longer time accumulating the body signal. The behavior time line is shown in Fig. 1(b), where the system stays in sleep phase for most of time and is activated in burst mode for data transmission. In order to design a low power WBAN system, it is necessary to analyze the relationship between the transmission energy and system design parameters based on the system operation behavior. For an in-depth analysis, the following denotes the notations which are used in the formulation:

- f_s : sampling rate of the sensor (also the operating rate of the storage);
- f_d : transmission data rate;
- T_{cycle} : the duration to fulfill the SU;
- T_{on} : the system active duration;
- T_{setup} : the setup time of the circuits from sleep to active;
- T_p : the duration of the preamble transmission;
- P_{on} : system dynamic power (except SU);
- P_{off} : system leakage power (except SU);
- P_{storage} : SU power.

Assuming that the SU can accumulate M samples and each sample contains N bits, so the duration to fill the storage can be computed by $T_{\text{cycle}} = M/f_s$. When the SU is full, the system from sleeping to active needs the setup time denoted as T_{setup}. Then the transmitter begins to transmit the data in the SU. The transmitter needs to transmit the preamble in advance for synchronization before the data transmission, and the duration is denoted as T_p. According to the data rate f_d and a total of $N \times M$ bits data in the SU, the duration to transmit data is $N \times M/f_d$. Therefore, the active duration can be computed as $T_{\text{on}} = T_{\text{setup}} + T_p + N \times M/f_d$.

With the behavior time line in Fig. 1(b) and the notations described above, the transmission energy per sample is defined as

$$\begin{aligned} E_{\text{sample}} &= \frac{P_{\text{on}}T_{\text{on}} + (P_{\text{off}} + P_{\text{storage}})T_{\text{cycle}}}{M} \\ &= \frac{P_{\text{on}}(T_{\text{setup}} + T_p + N \times M/f_d) + (P_{\text{off}} + P_{\text{storage}})(M/f_s)}{M} \\ &= \frac{P_{\text{on}}(T_{\text{setup}} + T_p)}{M} + \frac{N \times P_{\text{on}}}{f_d} + \frac{P_{\text{off}} + P_{\text{storage}}}{f_s}. \end{aligned} \quad (1)$$

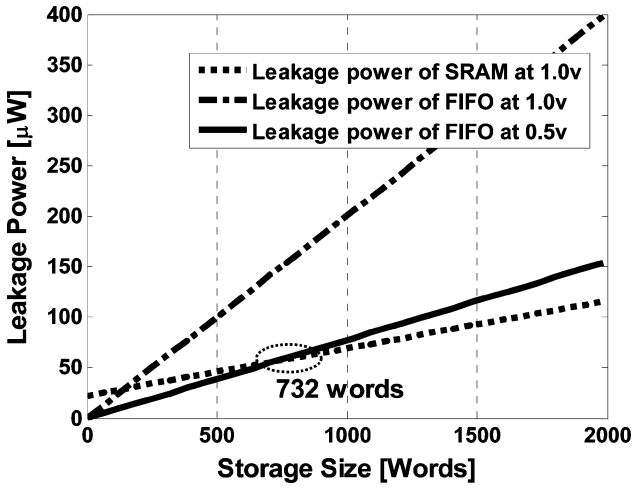

Fig. 2. Leakage power comparison between FIFO and SRAM with different storage size.

From (1), with the fixed sampling rate of the sensor, the transmission energy can be reduced by: (a) increasing the data rate f_d; (b) trading off the storage power and the size; (c) reducing the dynamic system power in active phase; (d) reducing the leakage power of the system. Therefore, the OFDM mode with high data rate mentioned before can reduce the transmission energy due to the strategy (a). Both active and leakage power can be reduced by several chipset implementation techniques which are discussed in Section V.

B. Storage Choice and Size Determination

Normally, both static random access memory (SRAM) and register-based first-in-first-out (FIFO) design are the candidates to store data. A comparison between these two candidates shows that SRAM costs less area and power consumption for large size SU requirement, but it suffers for small size SU due to the overhead from the sense amplifier. The register-based FIFO design has less static power when the SU size is small, and it also has the flexibility to scale the supply voltage to reduce the power consumption. Due to the low operation speed of the SU, the most power consumption comes from the leakage current. Fig. 2 shows the leakage power comparison between the register-based FIFO and SRAM with 90 nm standard CMOS process. It also includes the FIFO leakage power information under both 1.0 V and 0.5 V supply voltages, but the SRAM can only operate at 1.0 V due to the bias voltage for analog circuits such as the sense amplifier. Comparing to SRAM, FIFO with 1.0 V supply voltage performs better only when the SU size is less than 146 words, and the FIFO under 0.5 V has less leakage power when the SU size is less than 732 words. The SU size also affects the SU power and system transmission energy. Following introduces a simple design procedure to find the SU size.

From the simulation results, the approximate leakage power is expressed as follows:

$$P_{\text{FIFO\_0.5 V}}(\mu\,\text{W}) = 0.0775M \quad (2)$$

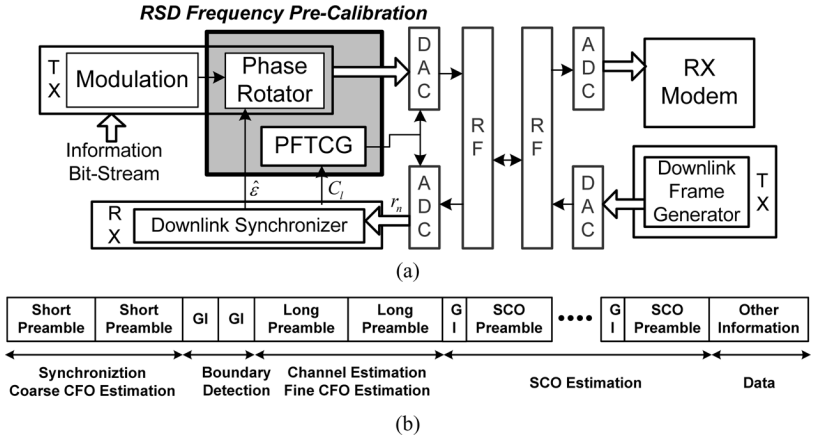

Fig. 3. The transmission block diagram with RSD frequency pre-calibration (a) and the down-link frame format (b).

$$P_{\mathrm{FIFO\_1.0\ V}}(\mu\,\mathrm{W}) = 0.20036M \tag{3}$$

$$P_{\mathrm{SRAM}}(\mu\,\mathrm{W}) = 22.414 + 0.0469M. \tag{4}$$

In the beginning, we assume the FIFO is used as the storage with 0.5 V supply to find the optimal SU size, and then SRAM can be used to derive the following equations if the optimal size is larger than 732. To formulate the optimization problem, we apply (2) to the SU power in (1):

$$E_{\mathrm{sample}} = \frac{P_{\mathrm{on}}(T_{\mathrm{setup}} + T_p)}{M} + \frac{0.0775}{f_s}M + \frac{N \times P_{\mathrm{on}}}{f_d} + \frac{P_{\mathrm{off}}}{f_s}. \tag{5}$$

Using the transmission energy per sample as the objective function, and the optimal SU size M can be computed by solving (6):

$$\min_{M}\ E_{\mathrm{sample}} \tag{6}$$

Then we examine if M is larger than or near 732 implying the SRAM may be a better choice. As a result, we put the SRAM power approximation (4) into (1) and repeat the same computation. By this procedure, a suitable SU and size can both be determined.

IV. Tiny Area Integration

In order to achieve long duration monitoring, tiny area for the sensor node is required. However, the system in the WSN requires an accurate clock source that is usually provided by an external quartz crystal, and that is hard to be integrated within a single die due to different fabrication processes. The crystal occupies large area in board level system integration, and that is a bottleneck to meet tiny area requirement in WSN. In these years, several clock source designs with CMOS process have been proposed to provide the clock signal without external crystals [9], [10]. By using these clock source designs, overall system can be integrated in a chip such that tiny area integration can be achieved.

However, these clock sources are less accurate and cause larger frequency mismatch such as the carrier frequency offset (CFO) and the sampling clock offset (SCO). Therefore, this work proposes a rotator-and-synthesizer driven (RSD) pre-calibration scheme to extend the baseband frequency mismatch tolerance.

A. RSD Based Pre-Calibration Scheme

For both OFDM and MT-CDMA modes, the up-link symbols are proposed to be pre-calibrated with the CFO and SCO via the RSD frequency pre-calibration shown in Fig. 3(a), where the frequency information is from the down-link synchronizer [11]. The down-link synchronizer estimates CFO and SCO from the down-link frame whose format is described in Fig. 3(b). The phase rotator rotates the data by the estimated CFO value before transmission. Because it is hard to achieve fine tuning in the radio frequency synthesizer, the phase rotator tries to calibrate the CFO by multiplying an exponential term $e^{-j2\pi\hat{\varepsilon}n}$ where $\hat{\varepsilon}$ is the estimated CFO and n is the time index. There are several existing SCO algorithms to compensate the SCO effect [12], [13], however, they are not suitable when the frame length is long or the error is large. In the RSD design, a PFTCG is proposed to calibrate the inaccurate sampling clock from the estimated SCO value. The benefits of providing phase tuning capability have been discussed in [1] (for power reduction). This PFTCG is used to adjust the generated clock phase and frequency automatically for better system performance and reduced power consumption. With the proposed RSD design in the transmitter, the frequency mismatch effects can be reduced to meet transmission requirements.

B. Mismatch Estimation Method

CFO refers to the difference in carrier frequency at transmitter and receiver resulting in the extra phase rotation on the demodulated signal. Therefore, the CFO value between the WSN and CPN is estimated by the expression

$$\begin{aligned} z &= \sum_{n=0}^{L-1} r_{n+L} \cdot (r_n)^* = \sum_{n=0}^{L-1} r_n e^{j2\pi\varepsilon} \cdot (r_n)^* \\ &= e^{j2\pi\varepsilon} \sum_{n=0}^{L-1} |r_n|^2 \end{aligned} \tag{7}$$

where r_n represents the periodic transmitted short preamble or long preamble, L is the length of the preamble, and z is the inner

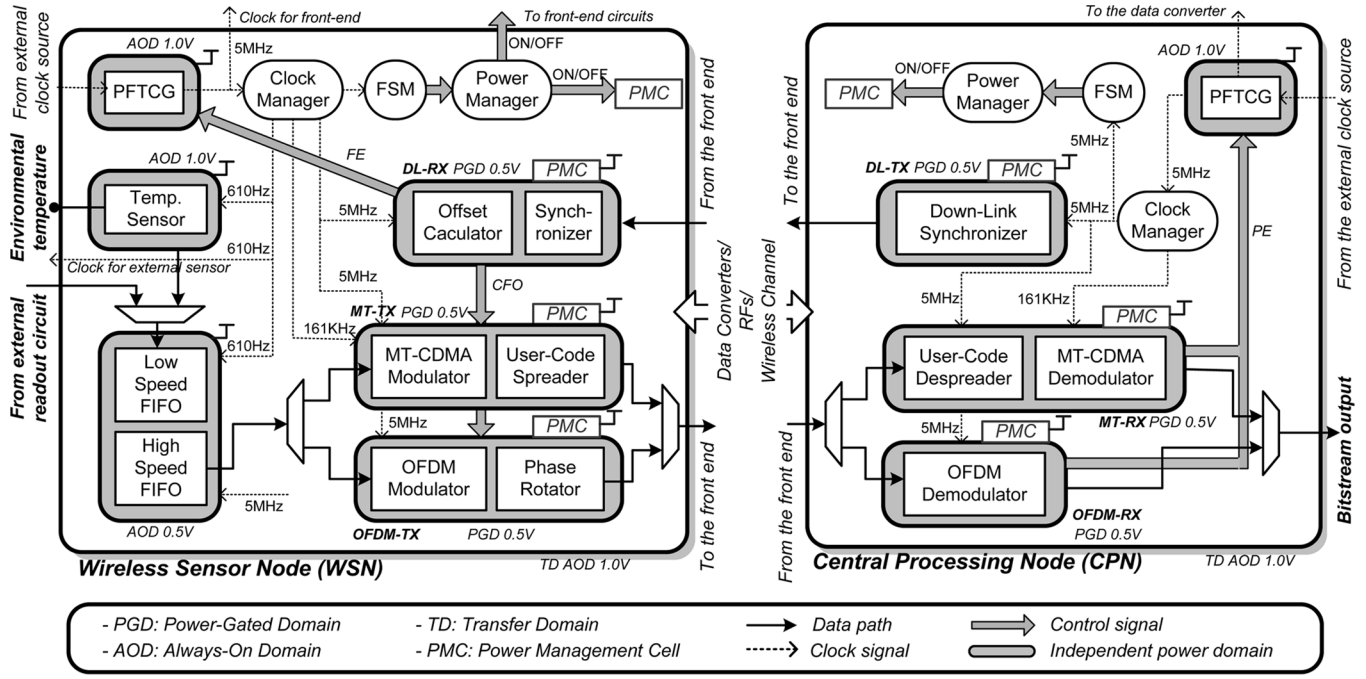

Fig. 4. The transceiver chipset architecture with power domain planning.

product of consecutive two preambles. The ε is the added CFO value, and the estimated CFO is computed via

$$\hat{\varepsilon} = (1/2\pi)\tan^{-1}(z). \tag{8}$$

The remaining received and ready-for-transmitted data will be compensated by the summation of two estimated values from short preamble and long preamble respectively.

The SCO value is estimated by the pilot information in preambles. These preambles after channel equalization and CFO compensation are transformed to frequency domain to perform SCO estimation. SCO results in extra phase rotation in frequency domain, where the behavior of the clock offset can be modeled as

$$\theta_{l,k} = C_{l,0} + C_{l,1}k. \tag{9}$$

Here k is the index of the subcarrier, and $\theta_{l,k}$ is the phase rotation of the data at k_{th} carrier in l_{th} preamble. The coefficient $C_{l,0}$ means the remaining CFO value after compensation. The slope $C_{l,1}$ is used to estimate SCO. The SCO effect on these pilots can be described as the following matrix form

$$\mathrm{K}C_l = \theta_l \tag{10}$$

where

$$K = \begin{bmatrix} 1 & k_1 \\ 1 & k_2 \\ \vdots & \vdots \\ \vdots & \vdots \\ 1 & k_m \end{bmatrix}, C_l = \begin{bmatrix} C_{l,0} \\ C_{l,1} \end{bmatrix}, \text{and } \theta_l = \begin{bmatrix} \theta_{l,k_1} \\ \theta_{l,k_2} \\ \vdots \\ \vdots \\ \theta_{l,k_m} \end{bmatrix}.$$

So the sampling clock offset C_l can be obtained by the least square algorithm:

$$C_l = (K^T K)^{-1} K^T \theta_l. \tag{11}$$

According to the estimated value in (11), the PFTCG is able to alter its generated frequency to reduce the sampling rate mismatch.

V. Chipset Design and Implementation

The detail chip architecture is shown in Fig. 4, including all functional blocks, controllers, clock signals, and data paths. The PFTCG receives the clock from clock source and then generates a 5 MHz clock signal to the clock manager. The PFTCG is able to adjust both phase and frequency for better performance from received information. The clock manager can synthesize different clock frequencies from the PFTCG output, such as 610 Hz for the sensor sampling and the storage, 161 KHz for MT-CDMA spreading codes, and 5 MHz clock for other signal processing blocks and the external front-end circuits.

The finite state machine (FSM) controls the chipset behavior, and the power manager controls specific functional blocks active or idle timing. The power manager outputs the TURN-ON (OFF) information to the front-end circuits and the power management cells (PMC) respectively.

To achieve optimal power distribution and management, the chipset is partitioned into 12 independent power domains with self power supply (including the transfer domains (TD)). As shown in Fig. 4, each block with bold line denotes an independent power domain.

A. Optimal Storage Design

In order to decide the SU type and size, the WBAN system active power should be estimated first, and then the SU size can be computed by (2)–(6). In this work, the power budget of the total system active power P_{on} is assumed to be 12 mW (including the data converter, synthesizers, power amplifier with 10% efficiency and proposed baseband chipset) when transmission output 0 dBm. Besides, 99.9% leakage power is assumed

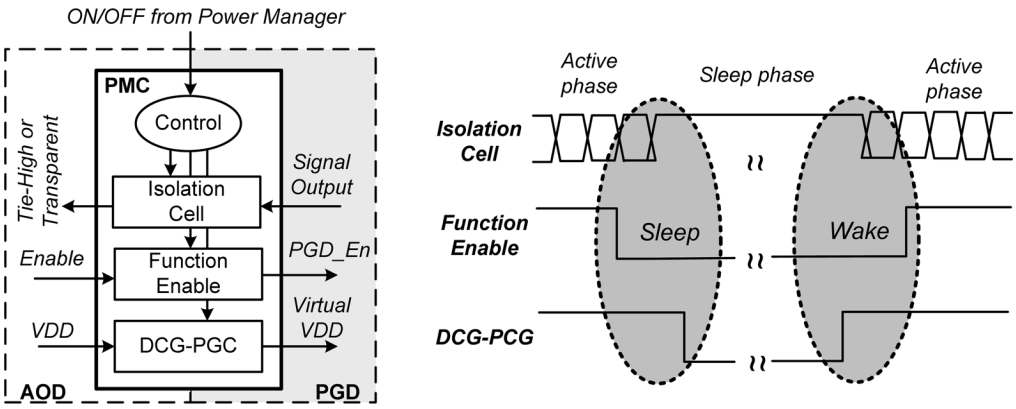

Fig. 5. Power management cell (PMC) and output of the PMC.

to be saved when the system is in sleep phase by applying the power gating scheme [1]. With SU operation rate $f_s = 610$ Hz, the system setup time T_{setup} is limited to one SU operation cycle ($1/610$ s). Assume the WSN only transmits one frame in the active duration to transmit all data in the SU. The frame preamble length in the proposed system is 356 samples with the processing speed 5 MHz, so the duration to transmit the preamble T_p is 71.2 μs for both modes. With these assumptions, it is found that $M = 402$ results in minimal transmission energy per sample by solving (6) for both modes. Because the size value is less than 732, it implies the FIFO is the better choice than SRAM in the proposed WBAN system. Among 2^n number close to 402, the FIFO is designed with size 512 words.

The SU includes a low speed and a high speed FIFO. The low speed FIFO accumulates signal from the sensor and dumps all data to the high speed FIFO when the low speed FIFO is full. Then the high speed FIFO uses 5 MHz clock to interface with the modulators. Therefore, when the modulator is turned on, the low speed FIFO can still receive body signal at the same time.

B. Voltage Scaling

Considering the short active duration property in WBAN system, the chipset stays in the sleep phase for most of time, so reducing the leakage power is an important issue. A high threshold voltage (HVT) device can provide smaller leakage power than regular threshold voltage (RVT) device. However, the dynamic power of the design with HVT process is much higher than RVT process, and the supply voltage for the HVT device cannot be reduced due to the limitation of the device property. In this work, our proposed WBAN chipset globally uses RVT process with voltage scaling such that both dynamic power and leakage power can be reduced. According to the leakage issue when using RVT process, a power gating scheme is proposed to save the leakage power in sleep phase.

In order to apply the voltage scaling scheme in the standard cell based design procedure, the cell behavior and timing information under 0.5 V supply voltage are simulated and recalibrated, then the cell library after picking out the cells which can work normally is reconstructed. With the reconstructed 0.5 V cell library, the proposed WBAN chipset can be implemented by exploiting standard cell-based design procedure.

TABLE II
DL-TX POWER WITH DIFFERENT PROCESS AND SUPPLY VOLTAGE

Voltage (Volt)	RVT		HVT	
	Dynamic	Leakage	Dynamic	Leakage
1.0	3.312μW	2.760μW	6.632μW	0.431μW
0.72	1.874μW	1.802μW	N/A	N/A
0.5	1.092μW	1.020μW	N/A	N/A

From Table II, the down-link transmitter (DL-TX) is used as an example to show the simulated power consumption comparison between RVT and HVT process with different supply voltages. With the RVT process, 65.22% transmitter power can be reduced by scaling the supply voltage from 1.0 V to 0.5 V. Comparing to HVT process with 1.0 V, about 70.11% power consumption is reduced when using RVT process at 0.5 V supply voltage. However, when the transmitter is in sleep phase, power consumption is only caused by the leakage current, and the leakage power in RVT is larger than HVT even when supply voltage is scaled to 0.5 V. To further reduce dynamic and leakage power consumption, the RVT with 0.5 V supply voltage is still selected for the proposed WBAN design, and the power gating scheme is added to save the leakage power in sleep phase such that the drawback of RVT process can be solved. In this chipset, the supply voltage of power domains is 0.5 V for the modulators, demodulators, and the FIFO. The PFTCG and the temperature sensor are still using 1.0 V for accurate results. Besides, the transfer domain (TD) also uses 1.0 V to interface with IO pads.

C. Power Gating

The ON/OFF behavior of the power-gated domains (PGD) is controlled by the PMC. As shown in Fig. 5, the PMC includes the isolation cells, function enable control, and the distributed-coarse-grain power gating cells (DCG-PCG) [1]. After receiving the ON/OFF signal from power manager, PMC will generate control sequence in order for the cells to interface between always-on domains (AOD) and PGD.

When the sleep command is received, the isolation cells tie-high the signal outputs of the function blocks in PGD to avoid the interference from unknown signals. Then the DCG-PGC gates the power supply which has the best performance to minimize the leakage current. When the state is from sleep to active,

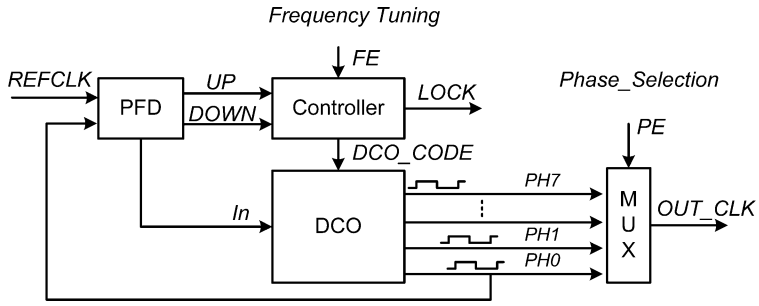

Fig. 6. The proposed PFTCG architecture.

the DCG-PCG turns on the supply voltage first, and then the isolation cells bypass the function block outputs from PGD to AOD. After the virtual supply is activated, the blocks in PGD are able to work normally, and then the function enable command in AOD can be bypassed to the blocks in PGD.

In this chipset, the power gating scheme is applied to the major signal processing blocks, including the modulators and demodulators, to save leakage power.

D. Phase Frequency Tunable Clock Generator

The phase-frequency tunable clock generator (PFTCG) is designed for performance improvement and power reduction in WSN and CPN respectively. As shown in Fig. 6, there are four major blocks, namely phase-frequency detector (PFD), controller, digitally-controlled oscillator (DCO) and phase selection multiplexer. The PFD and DCO are used for 5 MHz clock generation. In the beginning of clock generation and locking loop, the PFD generates an UP or DOWN command to modify the delay in the tracking loop. When this loop achieves the lock-in state, the resulting clock frequency corresponds to the desired 5 MHz clock, which is regarded as the coarse tuning loop.

The DCO further generates eight phases as the lock state is reached. It is designed with 8 delay buffers, and each buffer provides $T_{\mathrm{REFCLK}}/8$ delay time, resulting in 8 clock signals with equally-spaced $T_{\mathrm{REFCLK}}/8$ between Cycle_X and $\mathrm{Cycle}\_(X+1)$. Then one of these 8 sources is selected via the phase-selection. The correct frequency is generated by the closed loop of PFD, controller, and the phase_0 (PH0) in the DCO. This guarantees the resulted clocks keep the same delay spacing $T_{\mathrm{REFCLK}}/8$ when the process-voltage-temperature (PVT) condition changes.

The PFTCG allows both WSN and CPN to slightly change the generated clock frequency and phase by sending a command frequency-error (FE) and phase-error (PE) to the controller and multiplexer, respectively. This frequency fine-tuning capability is to reduce the sampling clock offset between the WSN and CPN for better performance, and the phase-selection capability enables the CPN to sample incoming signals at better instances without increasing sampling frequency [14].

VI. Simulation and Experimental Results

In the simulation results, the relationship among system power, maximal user number tolerance, data rate, and supply voltage are discussed. Besides, the system platform with frequency mismatch model is constructed to verify proposed our RSD pre-calibration scheme. For the experiment, the proposed baseband transceiver chipset is fabricated in 90 nm 1 P9M standard CMOS process. The measurement instruments include a LeCroy LC584A and a current-meter with resolution of 100 pA.

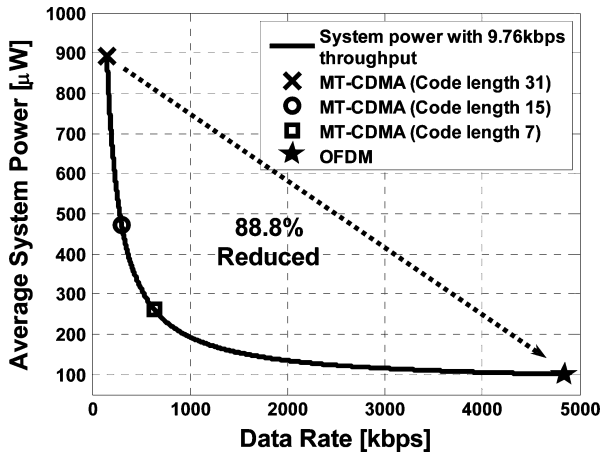

Fig. 7. Average system power with different transmission data rate.

A. System Power and Coexistence Tolerance

With the assumed system information and computed optimal FIFO size $M = 512$ mentioned in the previous section, we apply these values into (5) to get the relationship between the average system transmission energy and data rate. Then the average system transmission power can be computed by multiplying the transmission energy per sample and sample duration ($1/610$ s). Total power consumption can be reduced by enhancing data rate because the system active duration T_{on} is reduced as shown in Fig. 7.

In our proposed chipset, the active duty cycle of OFDM mode and MT-CDMA mode (spreading code length 31) is 0.41% and 7.51% respectively, and OFDM achieves 88.8% power reduction due to much shorter active duration. With the same parameters listed in Table I, the data rate of MT-CDMA mode with spreading code length 15, 9 are also computed and denoted in the figure for reference.

Fig. 8 shows the maximum user number tolerance when OFDM mode and MT-CDMA mode with different code lengths. From the simulation, OFDM mode requires 11.2 dB to

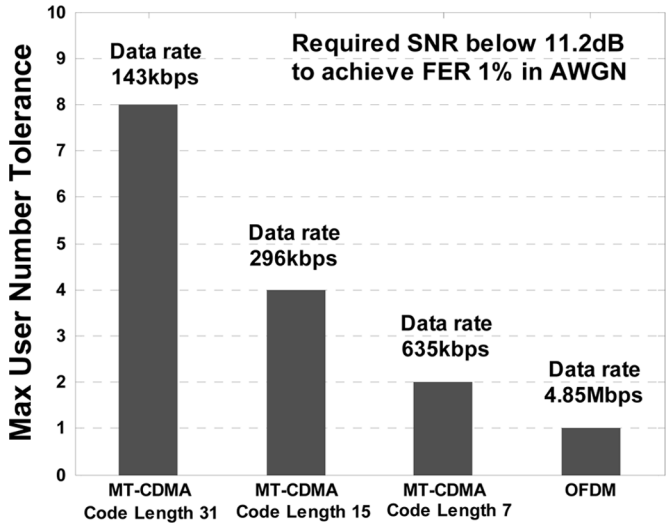

Fig. 8. Maximum user number tolerance in different operation conditions.

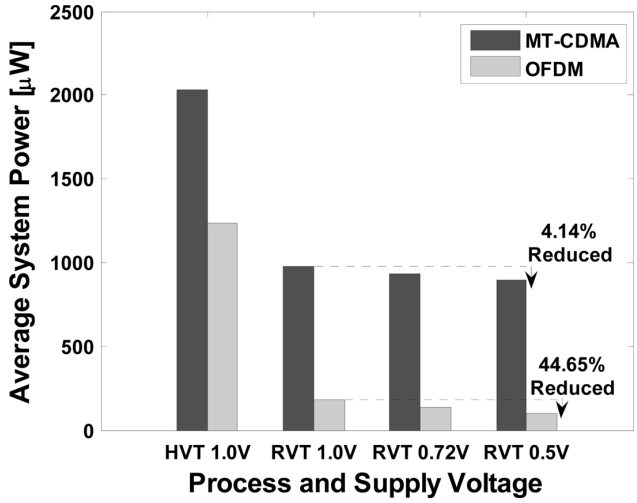

Fig. 9. Average system power with different processes and baseband supply voltages.

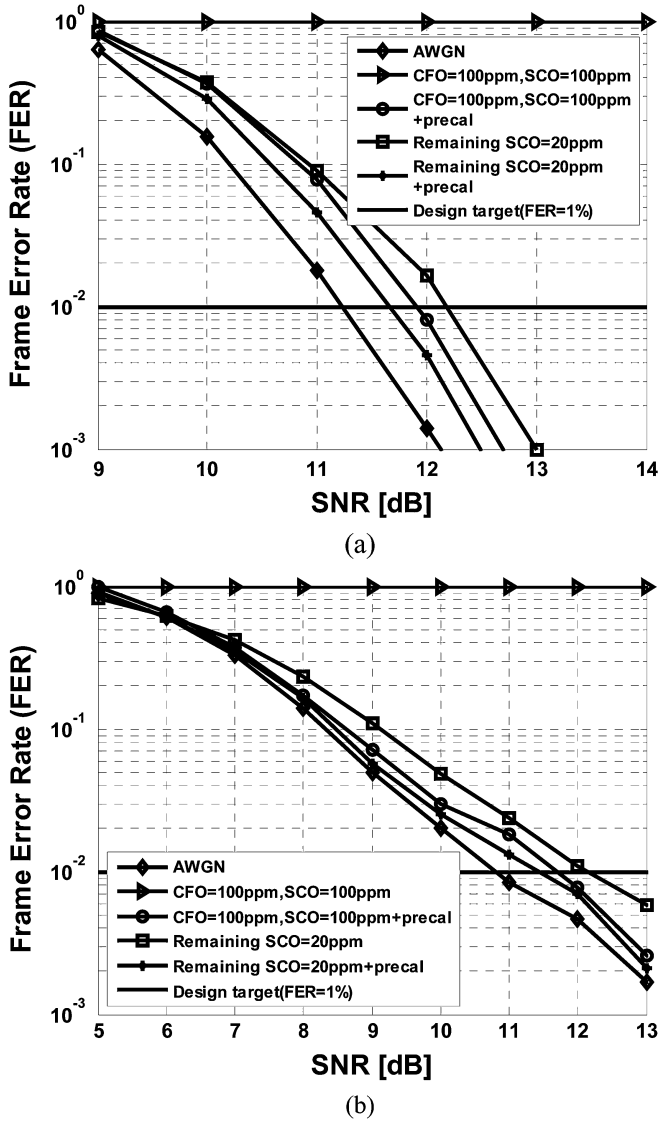

Fig. 10. System performance with RSD frequency pre-calibration. (a) OFDM mode. (b) MT-CDMA mode (8 users coexist with the same received signal power in the CPN).

achieve the target FER 1% with single user in AWGN channel. With the same SNR to keep FER, MT-CDMA improves the coexistence tolerance when increasing the spreading code length. In the proposed chipset, MT-CDMA with code length 31 enables 8 users operating at the same time with the same distance among all users and the CPN. Therefore, both OFDM and MT-CDMA have a trade-off between average system power consumption and maximum user tolerance, and the proposed chipset provides both modes to meet different requirements.

B. System Power versus Process and Voltage Scaling

Among different supply voltages and processes, Fig. 9 shows the average system transmission power comparison when using the MT-CDMA and OFDM mode. Different processes and supply voltages result in different dynamic and leakage power of the baseband transceiver and the FIFO module.

The system power with HVT process is the highest in both modes due to the significant dynamic power of baseband chipset. When using the MT-CDMA mode with RVT process, the active power of front-end circuits in $P_{\rm on}$ with large active duty cycle dominates overall average system power. Applying voltage scaling scheme in the proposed baseband chipset can save 4.14% system power from the reduced baseband transceiver power and always-on storage power $P_{\rm storage}$. According to shorter active duration of OFDM mode, the percentage of $P_{\rm on}$ in average transmission power is reduced, and the power reduction on $P_{\rm storage}$ by voltage scaling becomes more significant to overall average system power. Comparing to RVT process with 1.0 V supply voltage, the proposed chipset using 0.5 V can further reduce 44.65% average system transmission power when using the OFDM mode.

C. System Performance With Frequency Mismatch

Fig. 10(a) and (b) show the system FER performance under AWGN and frequency mismatch channel when using OFDM and MT-CDMA modes respectively. For each curve, 10000 frames with 12000 symbol length are simulated. For the OFDM

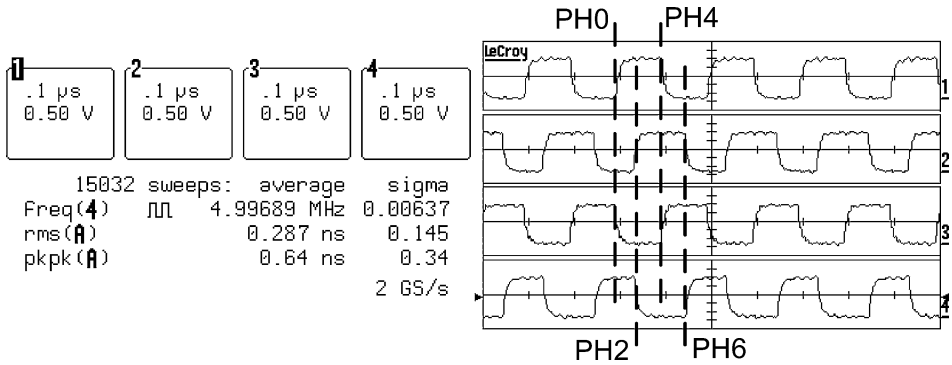

Fig. 11. Clock output from PFTCG.

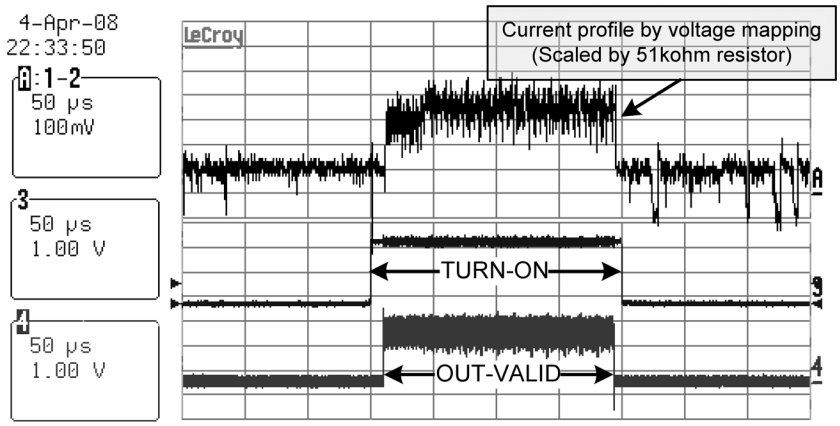

Fig. 12. Current profile between sleep and active.

mode in only AWGN channel, the FER achieves 1% when SNR equals 11.2 dB as shown in Fig. 10(a). Fig. 10(b) shows the FER of MT-CDMA mode when 8 users coexist. Assuming the received signal power from 8 users is the same, 1% FER can still be maintained with required SNR 10.8 dB that implies the robust transmission in multi-user environment for MT-CDMA mode.

These figures also show the frequency error tolerance is extended to 100 ppm in both modes. In order to simulate the frequency mismatch effects, CFO and SCO models are also added between the CPN and WSN. For non-pre-calibrated case, the FER performance in both modes becomes saturated when frequency errors are over 100 ppm. By applying the proposed RSD pre-calibration scheme, the remaining frequency error after pre-calibration is less than 20 ppm which can easily be solved by using the existing algorithms [12], [13] in the receiver. Therefore, the performance can be converged to only 0.5–1 dB SNR loss when FER is equal to 1% which is better than the original system FER with frequency error of 20 ppm in both modes. Therefore, the frequency tolerance of our proposed system with RSD pre-calibration is 100 ppm which is 2.5 times of existing systems [11]. And this enables using an embedded CMOS clock source to provide the clock signal instead of an external crystal.

The generated clock frequency and phase number are 5 MHz and 8 phases, respectively. Fig. 11 shows four generated phases (PH0, PH2, PH4, PH6). This multi-phase clock generation provides better system performance and reduced power in data converter circuits as discussed in [14]. The output frequency can be fine-tuned by the information from the down-link receiver to reduce the sampling clock offset effects. The measured RMS and peak-to-peak jitter is 145 ps and 340 ps, respectively, which are allowed for our proposed chipset at 5 MHz operation speed. The power consumption is 145.8 μW at 5 MHz frequency and 1 V supply voltage.

D. Chipset Measurement Results

In order to verify the switching behavior between sleep phase and active phase, the DL-TX building block is used for the illustration of the current profile. This building block is the modulator in CPN and belongs to the PGD with 0.5 V. This current profile is generated by concatenating a resistor (51 k ohm) in the way of core power path for clear instrument observation, and the voltage between this resistor's two sides is shown in Fig. 12. As the TURN-ON command is given, the DL-TX domain is turned on, and more current is drawn (current $=$ (measured voltage)/51 kΩ) that corresponds to μW-level power consumption. Besides, the OUT-VALID signal is from low to high which represents the functional block in this domain can work normally under 0.5 V supply voltage.

The shmoo plot of our proposed chipset in Fig. 13 shows that higher frequency operation is achievable as supply voltage increases. The target specification of this chipset is to operate at 5 MHz with 0.5 V supply voltage.

The micro photo of this chipset is shown in Fig. 14 with power domain partitions separated by bold lines. The building blocks in this chipset are tended to be designed with individual groups

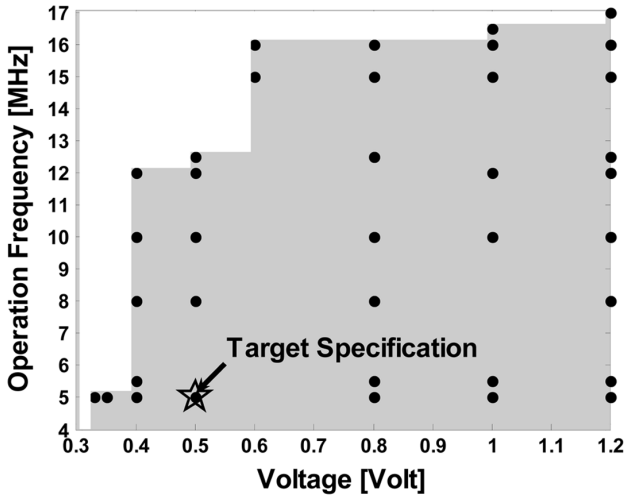

Fig. 13. Shmoo plot of proposed chipset operation.

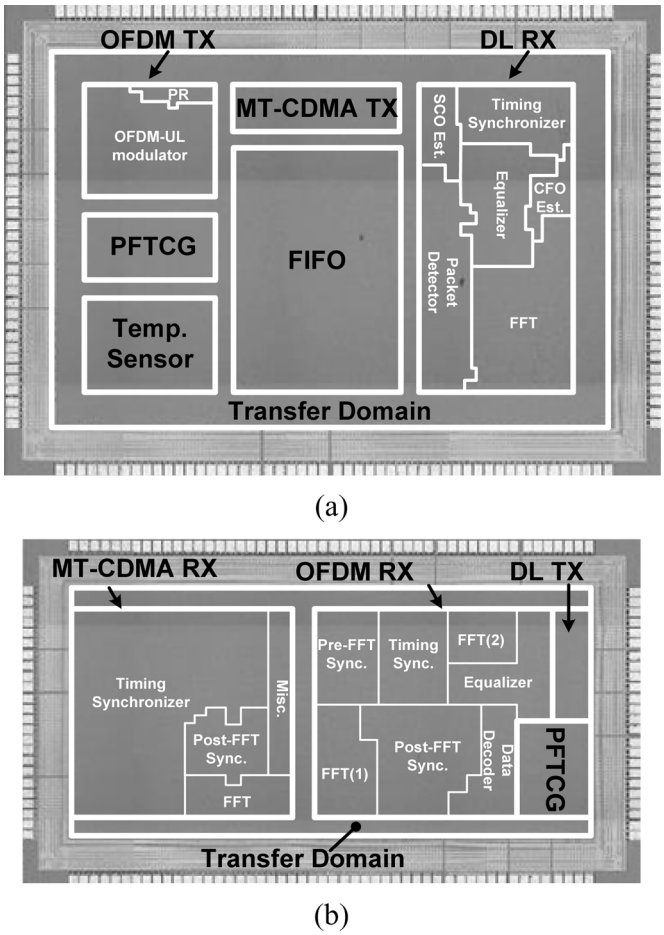

Fig. 14. Micro photo of the chipset (a) WSN and (b) CPN.

of power pads. This enables the power consumption in some of the blocks measured separately. Table III shows the measured core power consumption in corresponding power domain. The measured power of DL-TX is larger compared to the simulation results in Table II. This is because the extra cells to interface between AOD and PGD are ignored in the simulation level. The baseband transmission power is reduced from previous proposal

TABLE III
CHIP CORE POWER IN WSN AND CPN CHIPSET

WSN		CPN	
Total Modulator	5.52μW	DL-TX	3.94μW
		OFDM-RX	520μW
		MT-RX	490μW
FIFO	102.5μW	N/A	N/A
TS	187μW	N/A	N/A
PFTCG	145.8μW	PFTCG	145.8μW

TABLE IV
CHIP SUMMARY

Technology	Standard 90nm SPHVT/SPRVT CMOS
Core Supply Voltage	Globally 0.5V
Max Data Rate	4.85Mbps (OFDM) 143kbps (MT-CDMA)
Storage	Register-based FIFO (512 words)
PFTCG	8 Phases Generations RMS Jitter 145ps
Die Size	WSN: 2191μm x 3030 μm CPN: 1980 μm x 2980 μm

21 μW [1] to this work 5.52 μW (average), resulting in 73.7% efficiency improvement in baseband circuit processing. Finally, the chip summary is shown in Table IV.

VII. CONCLUSION

This paper presents a dual-mode baseband transceiver chipset design based on transmission energy analysis and data storage behavior. The baseband chipset using OFDM mode can provide high data rate to reduce the transmission energy due to shorter active duration, and MT-CDMA mode can allow multiple sensor nodes coexistence. Besides, a register-based FIFO with optimal size is designed for minimal transmission energy.

To achieve tiny area integration, a pre-calibration scheme and an embedded clock generator with frequency and phase tuning capability are provided to extend the frequency tolerance. The supply voltage of this chipset is globally scaled to 0.5 V with dedicated power-domain partitions and the power gating scheme is applied to sleep phase. The WBAN design with our proposed chipset can operate with μW-level system power consumption. As a result, a low power with tiny area, WBAN system can be achieved for biotelemetry applications.

ACKNOWLEDGMENT

The authors would like to thank UMC for the University Shuttle Program for fabricating the test chip and CIC for EDA tool supports.

REFERENCES

[1] J.-Y. Yu, C.-C. Chung, W.-C. Liao, and C.-Y. Lee, "A sub-mW multi-tone CDMA baseband transceiver chipset for wireless body area network applications," *IEEE ISSCC Dig. Tech. Papers*, pp. 364–365, Feb. 2007.

[2] *Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Wireless Personal Area Networks (WPANs)*, IEEE Standard 802.15.1, 2005.
[3] *Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs)*, IEEE Standard 802.15.4, 2003.
[4] A. C.-W. Wong, D. McDonagh, G. Kathiresan, O. C. Omeni, O. El-Jamaly, T. C.-K. Chan, P. Paddan, and A. J. Burdett, "A 1 V, micropower system-on-chip for vital-sign monitoring in wireless body sensor networks," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 138–139.
[5] A. C. W. Wong, G. Kathiresan, C. K. T. Chan, O. Eljamaly, and A. J. Burdett, "A 1 V wireless transceiver for an ultra low power SoC for biotelemetry applications," in *Proc. ESSCIRC*, Sep. 2007, pp. 127–130.
[6] J. Rychaert *et al.*, "Ultra-wideband transmitter for low-power wireless body area networks: Design and evaluation," *IEEE Trans. Circuits Syst. I*, vol. 52, no. 12, pp. 2515–2525, Dec. 2005.
[7] M. Demirkan and R. R. Spencer, "A pulse-based ultra-wideband transmitter in 90-nm CMOS for WPANs," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2020–2028, Dec. 2008.
[8] D. Guermandi, S. Gambini, and J. Rabaey, "A 1 V 250 Kpps 90 nm CMOS pulse based transceiver for CM-range wireless communication," in *Proc. ESSCIRC*, Sep. 2007, pp. 135–138.
[9] K. Sundaresan, P. E. Allen, and F. Ayazi, "Process and temperature compensation in a 7-MHz CMOS clock oscillator," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 433–442, Feb. 2006.
[10] C.-Y. Yu, J.-Y. Yu, and C.-Y. Lee, "An ecrystal oscillator with self-calibration capability," in *Proc. IEEE ISCAS*, May 2009, pp. 237–240.
[11] H.-H. Ma, J.-Y. Yu, T.-W. Chen, C.-Y. Yu, and C.-Y. Lee, "An OFDMA scheme wireless body area network with frequency pre-calibration," in *Proc. 2008 IEEE VLSI-DAT*, Apr. 2008, pp. 192–195.
[12] P. H. Moose, "A technique for orthogonal frequency division multiplexing frequency offset correction," *IEEE Trans. Commun.*, vol. 41, no. 10, pp. 1590–1598, Oct. 1994.
[13] S. A. Fechtel, "OFDM carrier and sampling frequency synchronization and its performance on stationary and mobile channels," *IEEE Trans. Consumer Electron.*, vol. 5, pp. 2777–2782, 1998.
[14] J.-Y. Yu, C.-C. Chung, and C.-Y. Lee, "A symbol-rate timing synchronization method for low power wireless OFDM systems," *IEEE Trans. Circuits Syst. II*, vol. 55, no. 9, pp. 922–926, Sep. 2008.

Tsan-Wen Chen was born in Taipei City, Taiwan, in 1984. He received the B.S. degree in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 2006. He is currently working toward the Ph.D. degree in electronics engineering in the same department.

His research interests include blind equalization algorithm, VLSI architecture, low-power SoC, and wireless communication systems, especially in OFDM-based baseband transceiver for low-power WBAN system.

Jui-Yuan Yu was born in Taipei City, Taiwan, in 1979. He received the B.S. and Ph.D. degrees in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 2002 and 2008, respectively.

He is currently serving as a postdoctoral researcher in the same university. His research interests include VLSI architecture, low-power SoC, and wireless communication systems, especially in OFDM-based baseband transceiver for high-speed WLAN, ultra-wideband (UWB) systems, and low-power WBAN systems.

Chien-Ying Yu was born in Hsinchu City, Taiwan, in 1984. He received the B.S. degree in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 2006. He is currently working toward the Ph.D. degree in electronics engineering in the same department.

His research interests include VLSI architecture, low-power SoC, and wireless communication systems, especially in OFDM-based baseband transceiver for low-power WBAN systems and on-chip oscillator design.

Chen-Yi Lee (M'01) received the B.S. degree from National Chiao Tung University, Hsinchu, Taiwan, in 1982, and the M.S. and Ph.D. degrees from Katholieke University Leuven (KUL), Belgium, in 1986 and 1990, respectively, all in electrical engineering.

From 1986 to 1990, he was with IMEC/VSDM, working in the area of architecture synthesis for DSP. In February 1991, he joined the faculty of the Electronics Engineering Department, National Chiao Tung University, Hsinchu, Taiwan, where he is currently a Professor and Dean of Research and Development Office. His research interests mainly include VLSI algorithms and architectures for high-throughput DSP applications. He is also active in various aspects of high-speed networking, system-on-chip design technology, very low power designs, and multimedia signal processing. In these areas, he has published more than 150 papers and holds decades of patents.

Dr. Lee served as the Director of Chip Implementation Center (CIC), an organization for IC design promotion in Taiwan (2000–2003), and the microelectronics program coordinator of Engineering Division under National Science Council of Taiwan (2003–2005). He was the former IEEE CAS Taipei Chapter Chair.