*Journal of The Electrochemical Society*, 150 (12) G730-G734 (2003) 0013-4651/2003/150(12)/G730/5/\$7.00 © The Electrochemical Society, Inc.



**High Reliability Ultrathin Interpolyoxynitride Dielectrics** Prepared by N<sub>2</sub>O Plasma Annealing

**Jer Chyi Wang,<sup>a</sup> Jam Wem Lee,<sup>b</sup> Liang Tai Kuo,<sup>a</sup> Tan Fu Lei,<sup>a,z</sup>** and Chung Len Lee<sup>a</sup>

*a Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan b National Nano Device Laboratories, Hsinchu 300, Taiwan*

This work addresses the preparation of ultrathin (effective oxide thickness, 42 Å) interpoly-oxynitride (SiO<sub>x</sub>N<sub>y</sub>) films by annealing thin nitride films with high density  $N_2O$  plasma and  $N_2O$  rapid thermal annealing. The proposed oxynitride dielectrics formed using N<sub>2</sub>O plasma annealing exhibited low gate leakage current, high breakdown electric field, long ten-year lifetime, and large effective barrier height. These superior properties can be attributed to the high concentration of oxygen incorporated in the poly-II/nitride interface and a reduction of the trap density of the interpoly-oxynitride films. The dielectric is a suitable substitute for the inter-polyoxide of electrically-erasable programmable read only memory.  $\odot$  2003 The Electrochemical Society. [DOI: 10.1149/1.1619993] All rights reserved.

Manuscript received July 15, 2002. Available electronically October 9, 2003.

Deep submicrometer electrically-erasable programmable read only memory (EEPROM) requires a thin polyoxide with a low leakage current, a high breakdown field  $(E_{bd})$ , a large charge to breakdown (*Q*bd), and a low electron trapping rate to ensure good data retention and endurance characteristics.<sup>1-4</sup> Oxide/nitride/oxide (ONO) multilayered films have been extensively investigated and frequently used as the dielectric layer in the flash memory devices and other applications.<sup>5-7</sup> However, the scaling down of the interpoly dielectrics is critical for next generation nonvolatile memories with a small cell size and low programming voltage. Recently, many studies<sup>8-11</sup> were successfully employed tetra-ethyl-ortho-silicate (TEOS) vapor deposited polyoxide with rapid-thermal-annealing  $(RTA)$  with  $N_2O^{10}$  or  $NH_3$  pretreatment,<sup>11</sup> increasing reliability by making the interface smoother after oxidation. Unfortunately, the quality of thermally oxidized and TEOS vapor-deposited polyoxide is strongly related to the surface roughness and doping concentration of poly I. This relationship raises issues of reliability and scaling limits of the interpoly oxide.<sup>12</sup>

Oxynitride films have attracted much attention as gate and tunnel dielectrics for submicrometer devices due to their superior properties and better reliability than the conventional silicon dioxide films.<sup>13,14</sup> A previous study<sup>15</sup> of nitrided oxides demonstrated advanced properties owing to the presence of nitrogen at the interface. Moreover, the fact that oxynitride has a higher dielectric constant than the silicon dioxide presents many opportunities to decrease the equivalent oxide thickness (EOT). Not only metal oxide semiconductor field effect transistors but also electrically erasable and programmable read only memory (EEPROMs) depend on scaling of the thickness of the oxide to exhibit a large driving capability and charge storage. This work proposes, for the first time, an ultrathin interpoly-oxynitride (EOT =  $42 \text{ Å}$ ) deposited by low pressure chemical vapor deposition (LPCVD) with high density  $N<sub>2</sub>O$  plasma annealing. The fabricated interpoly-oxynitride has a very long tenyear lifetime, a low electron trapping rate, a high breakdown electric field, and a high barrier height. The interpoly-oxynitride, when used in EEPROM applications, can improve performance and reliability.

### **Experimental**

The  $n^+$ -polysilicon/polyoxide/n<sup>+</sup>-polysilicon capacitors were fabricated on p-type silicon (100) wafers. First, silicon wafers were thermally oxidized at 900°C to form a 20 nm thick isolation oxide. Then a 300 nm polysilicon layer (poly-I) was deposited in an LPCVD system using  $SiH<sub>4</sub>$  gas at 620 $^{\circ}$ C and subsequently doped with POCl<sub>3</sub> at  $850^{\circ}$ C for 40 min and drive-in for 20 min, resulting in a sheet resistance of 30-40 $\Omega/\square$ . After the stripping off of p-glass and standard RCA cleaning, the  $Si<sub>3</sub>N<sub>4</sub>$  films, 40 Å and 50 Å thick, were deposited in an LPCVD system at 650°C followed with a  $N_2O$ -plasma annealing (PLA) at 50 W for 5 min and  $N_2O$ -RTA annealing at 950°C for 30 s. Thereafter, a second 300 nm polysilicon layer (poly-II) was deposited by an LPCVD system at 620°C and doped to a sheet resistance of 30-40 $\Omega/\square$  by the same POCl<sub>3</sub> process as that for poly-I. After definition of the poly-II, all samples were covered with a 300 nm oxide as a passivation layer by plasma enhanced chemical vapor deposition. Contact holes were opened and aluminum was deposited and patterned to form final capacitor structures. Finally, all devices were sintered at  $400^{\circ}$ C for 30 min in an N<sub>2</sub> ambient. A cross-sectional view of the interpoly-oxynitride dielectrics is shown in Fig. 1.

The EOT of the interpoly-oxynitride was determined by the high frequency  $(100 \text{ kHz})$  capacitance-voltage  $(C-V)$  in the strong accumulation region using a Keithley 590 and 595. Moreover, the physical thickness was estimated by transmission electron microscopy (TEM). The electrical properties and reliabilities were measured using an HP 4156B semiconductor parameter analyzer.

## **Results and Discussion**

Figure 2a, b, and c show the TEM images of a 50 Å interpolynitride film of the control sample (without annealing) and the oxynitride dielectrics with RTN<sub>2</sub>O annealed at 950°C for 30 s and N<sub>2</sub>O plasma annealed at 50 W for 5 min, respectively. A small increment in the interpoly-oxynitride thickness was observed after  $RTN<sub>2</sub>O$  or N2O plasma annealing. The annealing can oxidize the nitride films to form oxynitride dielectrics; meanwhile, the oxygen atoms may be incorporated in the nitride/polysilicon interface by various annealing methods, improving the reliability characteristics of the interpolyoxynitride dielectrics. Additionally, from the TEM picture of the



**Figure 1.** Cross-sectional view of the ultrathin interpolysilicon-oxynitride film under high density  $N_2O$  plasma and  $RTN_2O$  annealing.

<sup>z</sup> E-mail: tflei@cc.nctu.edu.tw



**Figure 2.** TEM images of the interpoly-oxynitride films for the (a) control

interpoly-oxynitride sample with  $N_2O$  plasma annealing shown in Fig. 2c, the thickness can be estimated to be 80 Å, and the dielectric constant of the oxynitride was nearly 6.24, which value can be derived from the electrical thickness of 49 Å obtained from the high frequency C-V characteristics. Figure 3a shows the positive currentdensity potential (J-E) characteristics of the ultrathin interpolynitride film of the control sample  $(As)$  and the interpoly-oxynitride

sample; (b)  $RTN<sub>2</sub>O$  annealed sample; and (c) high density  $N<sub>2</sub>O$  plasma-

annealed sample.

dielectrics with  $RTN_2O$  annealed at 950°C for 30s (RTA) and  $N_2O$ plasma annealed at 50 W for 5 min (PLA). The characteristics of all samples with similar EOTs, between 42 and 43 Å, were compared. The RTA sample exhibited the lowest leakage current owing to the local improvement of the nitride/poly-I interface by the  $RTN<sub>2</sub>O$  annealing.  $RTN<sub>2</sub>O$  annealing has been reported to suppress the leakage current of CVD nitride films by forming an interfacial oxide at the nitride/silicon interface.16 Consequently, for the interpoly-nitride dielectric with  $RTN_2O$  annealing, an  $Si_3N_4/SiO_xN_y$  structure may be formed by incorporating the high concentration of oxygen at the nitride/poly-I interface. The fact that the electron barrier of  $SiO<sub>x</sub>N<sub>y</sub>$ films is higher than that of  $Si<sub>3</sub>N<sub>4</sub>$  dielectrics may be responsible for the low leakage current. The negative J-E characteristics shown in Fig. 3b, on the contrary, the interpoly-oxynitride dielectric annealed by the  $N<sub>2</sub>O$  plasma has the lowest leakage current. This result indicates that annealing effects of the  $N_2O$  plasma on the interpolyoxynitride dielectrics are superior to those of  $RTN<sub>2</sub>O$ , due to the incorporation of a high concentration of oxygen at the poly-II/nitride interface.

Figure 4 presents the Weibull plots of the breakdown electric field of the ultrathin interpoly-oxynitride dielectrics with nearly the same EOT in both polarities, respectively. The samples with annealing presented a higher breakdown electric field than the control sample under both positive  $(Fig. 4a)$  and negative bias  $(Fig. 4b)$ . In particularly, for the poly-II injection of the  $N_2O$  plasma-annealed sample, significant improvement of the breakdown electric field was observed (negative bias). This fact is attributable to the introduction of oxygen into both the poly-II/nitride interface and the bulk of the nitride film. Figure 5a is a plot of the time-dependent-dielectricbreakdown (TDDB) lifetime projection of the ultrathin interpolyoxynitride dielectrics with nearly the same EOT under poly-I injection (positive bias) as a function of electric field. After annealing, a large increase in the electric field over the projected 10-year lifetime was contemplated, due to the improvement of the dielectric near the nitride/poly-I interface. Under negative bias, as shown in Fig. 5b, the  $N<sub>2</sub>O$  plasma-annealed sample exhibited a fairly high electric field up to 7.25 MV/cm over the projected ten-year lifetime because of the superior quality of the interpoly-oxynitride dielectrics. The reduction of the leakage current may lead to fewer defects in the oxynitride film following the  $N_2O$  plasma annealing.

Figure 6 plots both polarities of the extrapolated electric field over the ten-year lifetime  $(E_{10y})$  and the effective barrier height  $(\phi_B)$  determined by using the Fowler-Nordheim (F-N) model of ultrathin interpoly-oxynitride dielectrics under various annealing processes with nearly the same EOT. The effective barrier height was obtained by plotting the J-E characteristics in the form of an F-N plot  $(J/E^2$  *vs.*  $1/E$ ).<sup>17</sup> Straight lines were obtained for all



**Figure 3.** Current density *vs.* electric field (J-E) characteristics of ultrathin interpoly-oxynitride films of the control sample (As) and the samples under  $RTN<sub>2</sub>O$  (RTA) and high density  $N<sub>2</sub>O$  plasma annealing  $(PLA)$  under  $(a)$  poly-II positive bias and  $(b)$  poly-II negative bias.



**Figure 4.** Weibull plots of the breakdown electric field of the ultrathin interpoly-oxynitride films of the As, RTA, and PLA samples under (a) poly-II positive bias and (b) poly-II negative bias.



**Figure 5.** TDDB lifetime projection of the ultra-thin interpoly-oxynitride dielectrics of the As, RTA, and PLA samples with nearly the same EOT as a function of electric field under (a) poly-II positive bias and (b) poly-II negative bias.



**Figure 6.** Extrapolated electric field over the ten-year lifetime  $(E_{10y})$  and the effective barrier height obtained using the Fowler-Nordheim (F-N) model of ultrathin interpoly-oxynitride films of the As, RTA, and PLA samples under (a) poly-II positive bias and (b) poly-II negative bias.



**Figure 7.** Electron trapping characteristics of the ultrathin interpolyoxynitride of the As, RTA, and PLA samples under (a) poly-II positive bias  $(J = 1$  mA/cm<sup>2</sup>) and (b) poly-II negative bias ( $J = -1$  mA/cm<sup>2</sup>).

samples, indicating that F-N tunneling was the major conducting mechanism. Transport due to F-N tunneling is specified by *J*  $= C_1 E^2 \exp(-\phi_B/E)$ , where *E* is the field, and  $C_1$  and  $\phi_B$  are constants for the effective mass and barrier height. Indeed, the effective barrier height and the extrapolated electric field over the ten-year lifetime increased after annealing, especially after high density  $N_2O$  plasma annealing. Not only poly-I but also poly-II injections exhibit the highest  $\phi_B$  and  $E_{10y}$  values for N<sub>2</sub>O plasmaannealing interpoly-oxynitride. This result is proven by Fig. 4, which shows the introduction of oxygen into both the polysilicon/ nitride interface and the bulk of the nitride film. This would increase the effective barrier height of the interpoly-oxynitride dielectric approaching that of silicon dioxide thin films. Figure 7 shows the electron trapping characteristics of both polarities for all samples under a constant current stress of 1 mA/cm<sup>2</sup>. The figure shows that the additional annealing of interpoly-oxynitride produced a smaller



Figure 8. Band diagrams of the interpoly-oxynitride dielectrics for the (a) RTA sample under poly-II positive bias, (b) PLA sample under poly-II positive bias, (c) RTA sample under poly-II negative bias, and (d) PLA sample under poly-II negative bias.

voltage shift than that of control sample. For poly-I injection, shown in Fig. 7a,  $N<sub>2</sub>O$  plasma annealing generated the smallest voltage shift, implying that the lowest charge was trapped near the nitride/ poly-I interface. Nevertheless, an early failure and larger trapping rate was observed for the RTA sample. This phenomenon can be explained by the band diagrams in Fig. 8a for the RTA sample and (b) for the PLA sample under poly-I injection. The  $Si<sub>3</sub>N<sub>4</sub>/SiO<sub>x</sub>N<sub>y</sub>$ structure was proposed above, and the large stress-induced-defects at the  $Si_3N_4/SiO_rN_v$  interface contributed to the early failure and larger trapping rate for the RTA sample. However, for the poly-II injection shown in Fig. 7b, the  $N_2O$  plasma-annealed sample had a larger trapping rate, which result is consistent with the fact that the some stress-induced-charge trapped at the  $SiO<sub>x</sub>N<sub>y</sub>/Si<sub>3</sub>N<sub>4</sub>$  interface under such annealing is detectable from the band diagram in Fig. 8d. Therefore, under  $N_2O$  plasma annealing, defects and traps were eliminated near the poly-I/oxynitride interface, while a few stressinduced-defects might have existed at the  $SiO<sub>x</sub>N<sub>y</sub>/Si<sub>3</sub>N<sub>4</sub>$  interface.

In conclusion, Table I summarizes data concerning an ultrathin (EOT  $\sim$  42 Å) and highly reliable interpoly-oxynitride film formed by additional annealing. For a similar oxide thickness, high density  $N<sub>2</sub>O$  plasma-annealed sample presents is more reliable than the RTN2O annealed sample.

#### **Conclusion**

This work examined the ultrathin  $(EOT = 42 \text{ Å})$  interpolyoxynitride films with high density  $N_2O$  plasma and  $RTN_2O$  annealing.  $N_2O$  plasma annealing led to the incorporation of a high concentration of oxygen into the poly-II/nitride interface and a reduction of the trap density. Accordingly the interpoly-oxynitride dielectrics were made more reliable with a lower gate leakage current, a higher breakdown electric field, a longer ten-year lifetime, and larger effective barrier height. The oxynitride is very suitable for use in the next generation EEPROM.

**Table I. Summary of the breakdown electric field**  $(E_{bd})$ **, effective barrier height**  $(\Phi_B)$  and the extrapolated electric field over the ten-year lifetime  $(E_{10y})$  of the ultrathin interpoly-oxynitride film **of the As, RTA, and PLA samples, respectively.**



# **Acknowledgments**

The authors thank the National Science Council of the Republic of China, Taiwan, for financially supporting this research under contract no. NSC92-2215-E009-022. The National Nano Device Laboratory, R.O.C., is also appreciated for their technical assistance.

*National Chiao-Tung University assisted in meeting the publication costs of this article.*

#### **References**

- 1. C. S. Lai, T. F. Lei, and C. L. Lee, *IEEE Trans. Electron Devices*, 43, 326 (1996).
- 2. L. Faraone, *IEEE Trans. Electron Devices*, 33, 1785 (1986).<br>3. S. L. Wu, T. Y. Lin, C. L. Lee, and T. F. Lei, *IEEE Electron Device Lett.*, **14**, 113
- $(1993).$
- 4. S. L. Wu, C. Y. Chen, T. Y. Lin, C. L. Lee, T. F. Lei, and M. S. Liang, *IEEE Trans. Electron Devices*, 44, 153 (1997).
- 5. C. L. Cha, E. F. Chor, H. Gong, A. Q. Zhang, and L. Chan, *Tech. Dig. Int.* Electron Devices Meet., **1997**, 82.<br>6. N. Matsuo and A. Sasaki, *IEEE Trans. Electron Devices*, **42**, 1340 (1995).
- 
- 7. S. Holland, *IEEE Trans. Nucl. Sci.*, **42**, 423 (1995).
- 8. J. W. Lee, C. L. Lee, T. F. Lei, and C. S. Lai, *IEEE Trans. Electron Devices,* **48**, 743 (2001).
- 9. C. H. Kao, C. S. Lai, and C. L. Lee, *IEEE Electron Device Lett.*, 44, 526 (1997). 10. C. H. Kao, C. S. Lai, and C. L. Lee, *IEEE Trans. Electron Devices,* **45**, 1927
- $(1998).$ 11. W. L. Yang, T. S. Chao, C. M. Cheng, T. M. Pan, and T. F. Lei, *IEEE Trans. Electron Devices*, 48, 1304 (2001).
- 12. L. Faraone, R. D. Vibronek, and J. T. Mcginn, *IEEE Trans. Electron Devices,* **32**, 577 (1985).
- 13. H. Sato, H. Kato, Y. Ohki, S. S. Kwang, and T. Noma, in *International Symposium on Electrical Insulating Materials*, ISEIM 2001, IEEJ Technical Committee on Dielectrics and Electrical Insulation, and IEEE Dielectrics and Electrical Insulation Society, p. 148 (2001).
- 14. T. Arakawa and H. Fukada, *Electron. Lett.*, **30**, 361 (1994).
- 15. T. M. Pan, T. F. Lei, W. L. Yang, C. M. Cheng, and T. S. Chao, *IEEE Electron Device Lett.*, 22, 68 (2001).
- 16. W. H. Lin, K. L. Pey, Z. Dong, S. Y.-M. Choi, M. S. Zhou, T. C. Ang, C. H. Ang, W. S. Lau, and J. H. Ye, *IEEE Electron Device Lett.*, **23**, 124 (2002).
- 17. P. Olivo, J. Sune, and B. Ricco, *IEEE Electron Device Lett.*, **12**, 620 (1991).